10-Gb/s Optical Receiver and VCSEL Driver in 0.13-μm CMOS Technology

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10-Gb/s Optical Receiver and VCSEL Driver in 0.13-μm CMOS Technology

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A 10-Gb/s optical receiver and VCSEL driver are designed and implemented in 0.13-μm CMOS technology. In optical communication system, the analog front-ends is the most critical component affecting the whole system speed and noise performance. Traditionally, Ⅲ-Ⅴ compound semiconductors such as GaAs, InP, and HEMT have been exploited to realize the analog front-ends due to their high-speed and

low-noise characteristics. However, deep-submicron CMOS technologies become more attractive due to its low cost and high integration capacity. And almost optical receivers and transmitters over 10-Gb/s operation exploited passive inductor to enhance the bandwidth, while the area of chipset became large [1]-[3]. In this thesis, we realize 10-Gb/s CMOS optical receiver and VCSEL driver without passive inductor.

Optical receiver includes transimpedance amplifier (TIA) and limiting amplifier (LA). The advanced common-gate (ACG) stage is exploited as the input configuration of TIA. The ACG input configuration can effectively isolate the large photodiode capacitance from the bandwidth determination, as providing virtual-ground input impedance. And limiting amplifier achieves wide bandwidth using the combination of active feedback and negative impedance compensation. We estimate p-i-n photodiode has 0.7-A/W responsivity and 0.25-pF parasitic capacitance. An optical receiver achieves 10-Gb/s operations with 6.6-GHz 3-dB bandwidth for 0.25-pF input parasitic capacitance, 96-dBΩ transimpedance gain, and 22-pA/sqrt(Hz) average input-referred noise current density that corresponds to -16.5-dBm sensitivity for 10^{-12} BER. The whole receiver chip occupies the area of 1.8 × 1.35 mm^2, and the power dissipation is 54-mW from a single 1.2-V

supply.

VCSEL driver consists of LVDS/CML compatible pre amplifier, and main driver. The designed transmitter drives VCSEL array, operating up to 10-Gb/s with bias control (5~20-mA) and modulation control (5~20-mApp) to obtain constant and reliable optical output power. The whole transmitter chip occupies the area of 2.05 × 0.83 mm^2, and dissipates 50-mW from a single 1.8-V supply.

Keywords: Optical Receiver, VCSEL Driver, Transimpedance Amplifier, Limiting Amplifier, Active Feedback, CMOS

Chapter Ⅰ

Introduction

1.1 Optical Communication

As the technology of communication systems has advanced in modern society, the amount of information transported has increased enormously. The technology of first the electronic era and then the microelectronic era led to the development of a number of analog and digital communication techniques that resulted in the installation and expansion of wireless and satellite links. Many researchers have found methods to exploit the available bandwidth and to expand its capacity for information to the point where fundamental constraints of noise, interference, power, cost, and other issues began to limit progress in electronic communication links. Research in how to overcome these limitations brought the next step in the evolution of communication systems, which is the use of optics as a replacement for electronics. The inherent advantages of optics, as compared with conventional electronics, have led a widespread replacement of copper cables for communication at data rates above Mbps and over kilometers. Wide bandwidth optical fibers allow high data rates and large data capacity with low transmission loss, which allows vastly increased distances

between repeaters. In addition, a natural immunity to EMI (electromagnetic interference) helps keep SNRs low and permits the use of optical communication systems in noisy environments. As a consequence of these advantages, optical communication systems have replaced conventional electronic communication systems in long-distance applications and gradually are coming into use in networks involving short-haul applications [4].

Today optical communication systems are used in many applications such as synchronous digital hierarchy (SDH), synchronous optical networks (SONET) systems, wavelength division multiplexing (WDM) network systems, local area networks (LANs), metropolitan area networks (MANs), fiber-to-the-curb/home/building/desktop/office (FTTX), and board-to-board interconnections, all of which use optical fiber for data conveyance.

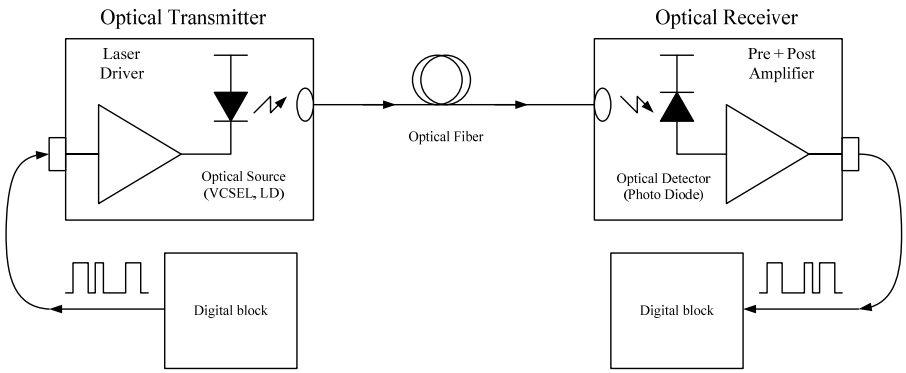


Figure 1.1 Overview of Optical Links

An optical communication system generally has three main parts: a transmitter, a transmission medium, and a receiver, as shown in Fig 1.1. This structure is similar to that of conventional electronic communication systems. The difference between two systems is that optical systems exploit optical fibers as a transmission medium instead of copper wires. The receiver consists of optical detectors such as p-i-n photodiode (PIN PD) or avalanche photodiode (APD), transimpedance amplifier (TIA), and limiting amplifier (LA). The transmitter consists of optical sources such as a laser diode (LD), a light emitting diode (LED), or a vertical cavity surface emitting laser (VCSEL) and their driver circuits [5], [6].

This dissertation will focus on the design and implementation of 10-Gb/s optical receiver and VCSEL driver in 0.13-μm standard CMOS technology. At first, backgrounds of optical receiver and VCSEL driver will be explained, and then the design issues and circuit details will be described. Details of dissertation outline are as follows.

In chapter Ⅱ, 10-Gb/s optical receiver design is discussed. Section 2.1 introduces basic background about optical receiver. In section 2.2, the design details of transimpedance amplifier and limiting amplifier are presented. And section 2.3 describes simulation results optical receiver.

Next, in chapter Ⅲ, 10-Gb/s VCSEL driver design is described. At first, basic background is introduced in section 3.1. And then, circuit details of VCSEL driver are described in section 3.2. In section 3.3, post layout simulation results of optical transmitter are discussed.

In chapter Ⅳ, IC fabrication and measurement are discussed. In section 4.1, IC fabrication and implementation methods are introduced, and then printed-circuit boards (PCBs) design is described in section 4.2. Measurement results of fabricated chipsets are discussed in section 4.3. At last, chapter Ⅴ summarizes results of 10-Gb/s optical receiver and VCSEL driver in CMOS 0.13-μm technology.

Chapter Ⅱ

10-Gb/s Optical Receiver Design

2.1 Background

The basic optical receiver consists of a photodiode and a transimpedance amplifier. The photodiode is a square law device, which means the detected electrical current depends on the power of the incident optical signal. TIA amplifies this electrical current with sufficient bandwidth, converting it to a voltage, while adding as little noise as possible. Generally, the TIA output signal is still not large enough to reach detectable logic levels (approximately 500-mVpp) so additional amplification is required in the form of a limiting amplifier (LA). The input signal of LA is amplified until it is saturated at the amplifier voltage rails. This has the effect of producing a reasonably constant output voltage swing for a wide range of input voltage levels. If the LA is DC coupled to the TIA, DC offset compensation is required to prevent the LA from saturating at one rail. The TIA and LA make up what is generally called the analog front-end of the optical receiver.

After the received signal has been boosted to detectable logic levels,

a decision circuit is used to remove the noise from the received signal. The decision circuit is timed by a clock recovery circuit which extracts a clock signal from the received data. It is important that the clock driving the retimer (flip-flop) has a well-defined phase relationship with the received data such that the signal is sampled at the optimum point during the bit period. Finally, the signal can be multiplexed down to multiple lower bit rate signals using a de-multiplexer (DEMUX). A block diagram of this typical optical receiver is shown in Fig 2.1 [7].

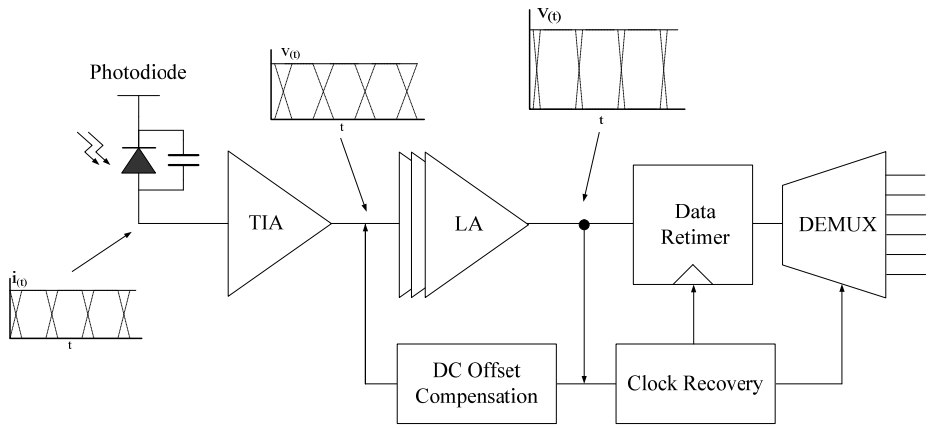


Figure 2.1 Block Diagram of Optical Receiver

2.1.1 Photodiode

The first element in an optical receiver is the photodiode. It is important to understand the main characteristics of this device, namely responsivity and noise, in order to be able to discuss and calculate the

performance of receiver. The photodetector together with the transimpedance amplifier largely determine the sensitivity of receiver. Fig 2.2 shows the conceptual diagram of p-i-n photodiode (PIN PD). We can write down the light-current relationship for a p-i-n diode knowing that the fraction η of all photons creates electrons. Each photon has the energy hc/λ and each electron carries the charge q, thus the electrical current (I_{PD}) can be expressed for a given amount of optical power (P) illuminating PIN PD:

$$I_{PD} = \eta \cdot \frac{\lambda q}{hc} \cdot P \tag{2.1}$$

To simplification we call the constant relating I_{PD} and P the *Responsivity* of the photodiode and use the symbol R for it :

$$I_{PD} = R \cdot P \quad \text{with} \quad R = \eta \cdot \frac{\lambda q}{hc} \tag{2.2}$$

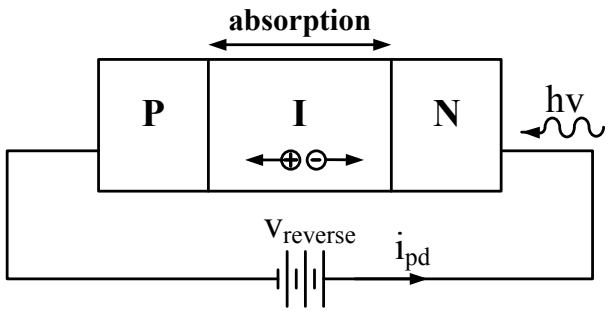


Figure 2.2 p-i-n Photodiode

Fig 2.3 shows the AC equivalent circuit for PIN PD. The value of parasitic components can be estimated to C_{PD}=*0.15~0.25-pF* and R_S=*20Ω* for 10-Gb/s operation. We can see that the output impedance of the p-i-n photodiode is mostly capacitive [8].

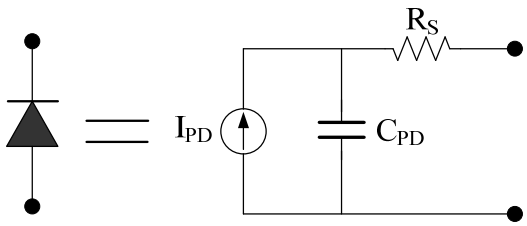


Figure 2.3 AC Equivalent Circuit for p-i-n Photodiode

2.1.2 Transimpedance Amplifier

2.1.2.1 TIA Specifications

Before looking into the implementation of TIAs, it is useful to discuss their main specifications: the transimpedance gain (Z_T), the bandwidth, the input-referred noise current.

Transimpedance Gain (Z_T)

The transimpedance gain (Z_T) is defined as the output voltage change, Δ*Vout*, per input current change, Δ*Iin* (See Fig 2.4):

$$Z_T = \frac{\Delta V_{out}}{\Delta I_{in}} \tag{2.3}$$

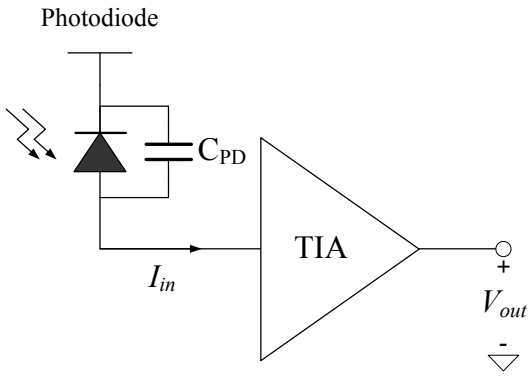


Figure 2.4 Input and Output Signals of a TIA

Thus, the higher the transresistance, the more output signal we get for a given input signal. The transimpedance is either specified in units of Ω or dBΩ. In the latter case, the value in dBΩ is calculated as $20log(Z_T/\Omega)$, for example, 1-kΩ corresponds to 60-dBΩ. In practice it is desirable to make the transimpedance of the TIA as high as possible because this relaxes the gain and noise requirements for the limiting amplifier. However, there is an upper limit to the transimpedance that can be achieved with the basic shunt-feedback topology. This limit depends on many factors including the bit rate and the technology used. For higher bit rates it is harder to get a high transimpedance with the required bandwidth. Therefore we typically see a lower Z_T for 10-Gb/s parts than for 2.5-Gb/s parts. Typical values for the single-ended transimpedance gain are $Z_T=1\sim2\text{-}\ k\Omega$ for 2.5-Gb/s and $Z_T=0.5\sim1\text{-}k\Omega$ for 10-Gb/s [9].

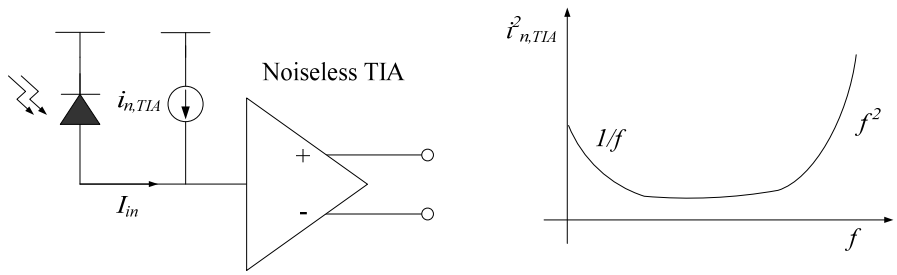
Bandwidth ($BW_{3\text{-}dB}$)

The TIA bandwidth, $BW_{3\text{-}dB}$, is defined as the frequency at which the amplitude response of $Z_T(f)$ dropped by 3-dB below its passband value. This bandwidth is therefore also called the 3-dB bandwidth to distinguish it from the noise bandwidth. The 3-dB bandwidth of the TIA is determined by the tradeoffs between inter-symbol interference (ISI) and noise. If we make 3-dB bandwidth wide, the TIA adds very little distortion to the signal. But at the same time a wideband TIA produces a lot of noise and this noise reduces the total receiver sensitivity. Alternatively, if we choose a narrow bandwidth the noise is reduced which is good. But now we have distortions, called ISI in the output signal. ISI also reduces the sensitivity because the worst-case output signal is reduced. We can conclude that there must be an optimum TIA bandwidth for which we get the best sensitivity. As rule of thumb this 3-dB bandwidth is $BW_{3\text{-}dB}=0.6 \sim 0.7 \cdot R_B$, where R_B is the desired bit rate, and NRZ signal is assumed.

Input-Referred Noise Current

The input-referred noise current is one of the most critical TIA parameter. Often the noise of the TIA dominates all other noise sources (e.g. photodiode, main amplifier, etc.) and therefore determines the

sensitivity of the whole receiver. Fig 2.5(a) shows a noiseless TIA with an equivalent noise current source, $i_{n,TIA}$, at the input. This current source is chosen such that, together with the noiseless TIA, it produces the same noise at the output as the real noisy TIA. The *Input-Referred Noise Current Spectrum*, $I^2_{n,TIA}(f)$, has the typical frequency dependence shown in Fig 2.5(b). Since this spectrum is not *white* it is not sufficient to specify a value at a single frequency. For a meaningful comparison of the TIA noise performance it is necessary to look at the



(a) (b)

Figure 2.5 (a) Input-referred noise current, and (b) typical power spectrum

whole spectrum up to about ($2 \times BW_{3\text{-dB}}$). Furthermore, the sensitivity of the TIA depends on a *combination* of the noise spectrum and the frequency response $|Z_T(f)|$.

The *Input-Referred RMS Noise Current*, or *Total Input-Referred*

Noise Current, $i_{n,TIA}^{rms}(f)$, is determined by integrating the *output-referred* noise spectrum up at least 2 × $BW_{3\text{-}dB}$ and dividing it by the passband transimpedance value. Written in the squared form, we have:

$$\overline{i_{n,TIA}^2} = \frac{1}{|Z_T|^2} \int |Z_T(f)|^2 \cdot I_{n,TIA}^2(f)\, df \tag{2.4}$$

where $|Z_T(f)|$ is the frequency response of the transimpedance. The total input-referred noise current directly determines the sensitivity of the TIA:

$$i_S^{pp} = 2Q \cdot I_{n,TIA}^{rms} \tag{2.5}$$

where Q is the quality factor for desired bit error rates (BERs). The *Averaged Input-Referred Noise Current Density* is defined as the input-referred rms noise current, $i_{n,TIA}^{rms}$, divided by the square-root of the 3-dB bandwidth. Again, it is important that the averaging is carried out over the *output-referred* noise spectrum rather than the input-referred noise spectrum, $I_{n,TIA}^2$.

2.1.2.2 TIA Topologies

Generally there are two types of TIA topologies, open loop TIAs

and feedback TIAs. The goal when designing a TIA, is to provide a low input impedance in order to meet the bandwidth requirements, while also providing low noise and high gain. The characteristics and performance of these two topologies will be discussed below.

Open Loop TIAs

Open loop TIAs generally use common gate topology since this device is capable of providing a low input impedance. A typical common gate TIA is shown in Fig 2.6. The transistor M_1 is the common gate transistor with a resistive load R_D, while current source I_D provides a bias current. Since all of the photodiode current passes through the load resistance, R_D, the transimpedance gain is equal to R_D. The input resistance of this amplifier is given:

$$R_{in} \approx \frac{r_{01} + R_D}{1 + g_{m1} r_{01}} \approx \frac{1}{g_{m1}} \tag{2.6}$$

where r_0 is the drain to source resistance, g_{m1} is the transconductance. This equation assumes that internal resistance of current source, I_D, is sufficient large.

This is an important result because the bandwidth is independent of the transimpedance gain set by R_D. In reality, if R_D is increased too much, the output pole formed with the parasitic output capacitance of the common gate transistor will determine the bandwidth.

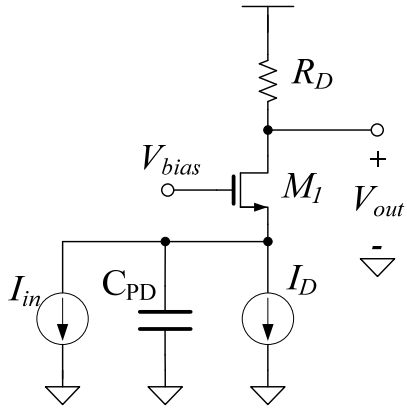


Figure 2.6 Common-Gate TIA

The unfortunate downside of this TIA is that the noise current produced by the load resistance R_D and the bias current source I_D are directly referred to the input with a unity factor. The noise contributions from these two sources have trade-off with each other. The load resistor can be increased in order to reduce its noise contribution. In order to maintain the proper biasing conditions, the bias current would need to be reduced which would increase the noise contribution of I_D. If the bias current is maintained, the supply voltage would need to be increased. In order to reduce the noise contribution from the bias current source, the bias current can be increased. Again, to maintain the bias conditions, the load resistor would need to be decreased, which would increase the noise contribution from the load resistor. If the load resistor is kept the same, the supply voltage would again need to be increased to maintain the transistor in saturation. Improving the noise

performance of this device comes at the cost of increased power consumption. As the supply voltage is increased, the power consumption increases quickly for a small improvement in the noise performance.

Feedback TIA

A more popular TIA topology is the shunt-shunt feedback structure shown in Fig 2.7. An ideal inverting voltage amplifier is shown with a feedback resistance, R_F. The impedance gain of this circuit given in the following equation:

$$Z_T = \frac{A}{A+1} \cdot \frac{R_F}{1 + jw\frac{R_F C_{PD}}{A+1}} \tag{2.7}$$

where A is the open loop voltage gain of the amplifier.

We can see that if the voltage gain, A, of the amplifier is sufficiently high, the transimpedance is approximately equal to R_F in the amplifier's passband. Assuming that the dominant pole at the input, the bandwidth of this circuit will be given by the following expression:

$$f_{3-dB} \approx \frac{A+1}{2\pi C_{PD} R_F} \tag{2.8}$$

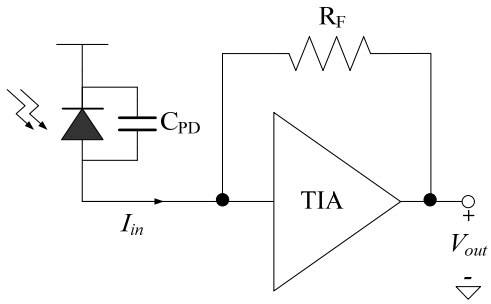


Figure 2.7 Feedback TIA

The bandwidth of the TIA is greater than that of a simple resistive network by a factor of A+1. The noise of the feedback resistor R_F is directly referred to the input with a unity factor, while the noise from the voltage amplifier is divided by a factor of R_F. This is similar to the load resistor in the common gate amplifier, but in this case R_F doesn't carry bias current and therefore can be increased without increasing the supply voltage.

2.1.3 Limiting Amplifier

The job of the limiting amplifier (LA) is to amplify the small input signal Vin from the TIA to a level which is sufficient for the reliable operation of the clock and data recovery (CDR) circuit. The required level for the output signal Vout is typically several hundreds mV peak-to-peak. Almost all LAs feature differential inputs as well as differential outputs, as shown in Fig 2.8. The LA is also known as *Post Amplifier* since it follows the TIA.

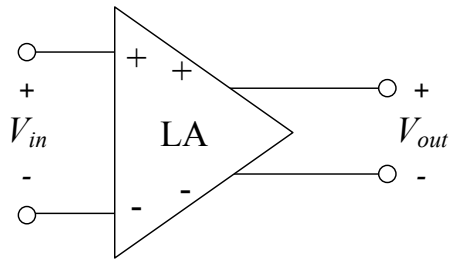


Figure 2.8 Input and Output Signals of a fully differential LA

For small signals, most amplifiers have a fairly linear transfer function. For large signals, however, nonlinear effect become apparent. Specifically, if the output amplitude approaches the power-supply voltage, severe distortions in the form of clipping set in. The DC transfer function of a LA is shown in Fig 2.9. The linear and the limiting regimes can be distinguished clearly. No special amplifier design is required to obtain the limiting characteristics of a LA, it happens naturally because of the finite power-supply voltage and other signal swing constraints. However, we need to make sure that the limiting happens in a controlled way, i.e., pulse-width distortions, jitter, and delay variations when the LA transitions from the linear to the limiting regime must be minimized.

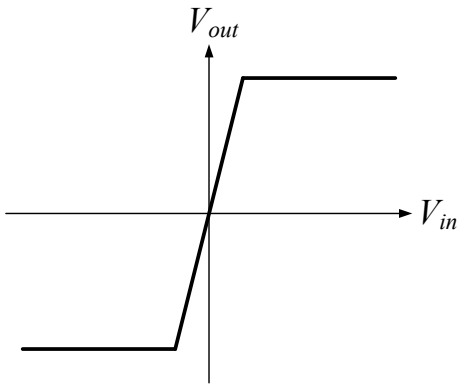


Figure 2.9 DC Transfer Characteristic of a LA

2.2 10-Gb/s Optical Receiver Analog Front-End Design

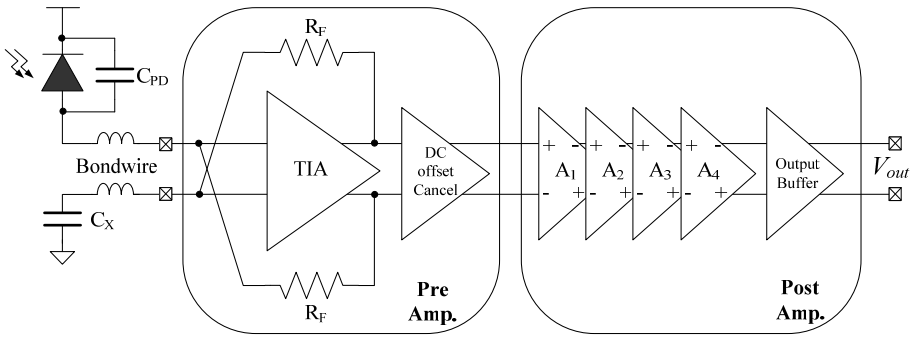


Figure 2.10 The Proposed Block Diagram of 10-Gb/s Optical Receiver

Fig 2.10 illustrates the block diagram of the proposed 10-Gb/s optical receiver, where all building blocks are designed to be differential so that the common-mode noises, such as power supply noise or substrate coupling noise, would be effectively reduced. Pre amplifier consists of the advanced common-gate (AGC) input stage, the voltage-gain stage with feedback resistance (R_F), and DC-offset cancellation stage. One input of the pre amplifier is connected to a p-i-n photodiode (PIN PD) and the other is connected to an off-chip capacitor (C_X) of which value is selected to be same as that of the photodiode. For 10-Gb/s operations, a photodiode with 0.7-A/W responsivity and 0.25-pF parasitic capacitance is utilized. Post amplifier consists of four active feedback gain stages with negative impedance compensation (NIC) and open drain output buffer.

2.2.1 TIA Input Configuration

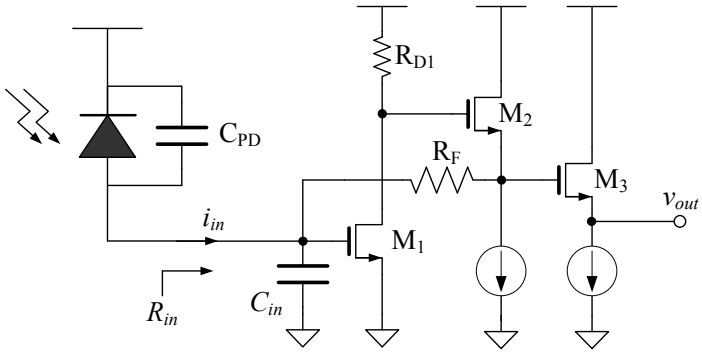


Figure 2.11 Conventional Common-Source TIA

Fig 2.11 shows the conventional common-source TIA. It suffers from serious design tradeoffs between the transimpedance gain (Z_T) , 3-dB bandwidth ($BW_{3\text{-}dB}$), and photodiode parasitic capacitance (C_{PD}). The bandwidth and transimpedance gain of the common-source TIA is given by:

$$Z_T = \frac{A}{A+1} \cdot R_F \approx R_F \tag{2.11}$$

$$BW_{3-dB} \approx \frac{A+1}{2\pi R_F (C_{PD} + C_{in})} \tag{2.12}$$

where A is the open-loop voltage gain of TIA, R_F is the feedback resistance, and C_{in} is the input parasitic capacitance including the ESD protection diode pad parasitic capacitance and the gate capacitance of M_1. For a given C_{PD}, R_F is directly proportional to Z_T, while is

inversely proportional to $BW_{3\text{-}dB}$. Therefore, it is very challenging to obtain both high Z_T and wide $BW_{3\text{-}dB}$ for a large C_{PD} in the design of common-source TIA. We can conclude that the input configuration is necessary for high speed application.

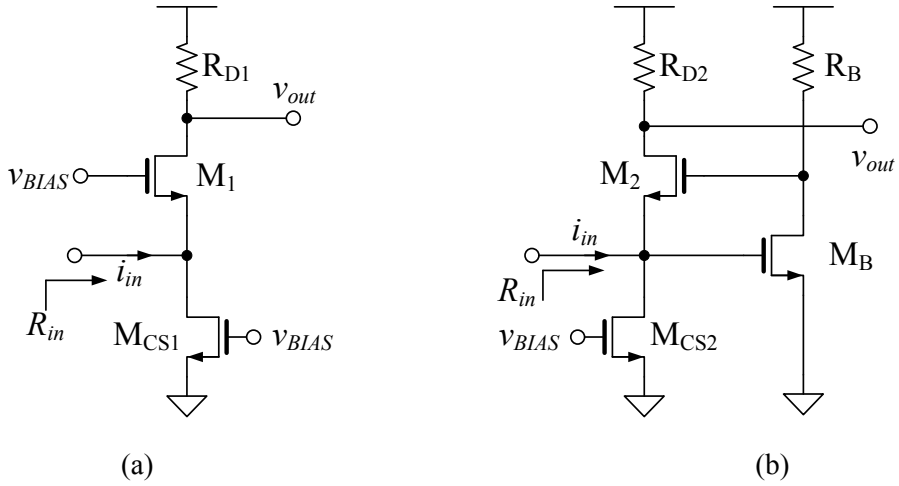


Figure 2.12 (a) Common-Gate and (b) Advanced Common-Gate Input Configuration

The common-gate input stage, shown in Fig 2.12(a), presents a small input resistance ($\sim 1/g_{m1}$). Therefore, the input pole can move to a higher frequency and thus the dominant pole of the circuit is now located at the other node, not input node. Hence, either a wider bandwidth or a larger transimpedance gain can be more easily achieved than conventional common-source TIA. The bandwidth of common-gate configuration is:

$$BW_{3-dB} \approx \frac{g_{m1}}{2\pi(C_{PD}+C_{in})} \tag{2.13}$$

Unfortunately, there are two limitations of the common-gate TIA in short channel CMOS technology. First, the device transconductance (g_{m1}) is not sufficiently large, then this input configuration cannot totally isolate the large photodiode capacitance from the bandwidth determination. Second, drain to source resistance of M_{CS1}, $r_{o,Mcs1}$, is not sufficient. Thus, the small-signal input current (i_{in}) can exhibit the leakage to the current source (M_{CS1}) [10].

Therefore, the advanced common-gate (ACG) input configuration, shown in Fig 2.12(b), is adopted in this thesis [11]. The ACG input configuration enhances the input resistance significantly due to the local feedback mechanism, so the ACG TIA can achieve better isolation of the photodiode capacitance than other configurations. The input resistance and 3-dB bandwidth of ACG stage is:

$$R_{in} = \frac{1}{(1+g_{mB}R_B)g_{m2}} \tag{2.14}$$

$$BW_{3-dB} \approx \frac{(1+g_{mB}R_B)g_{m2}}{2\pi(C_{PD}+C_{in})} \tag{2.15}$$

where $(1+g_{mB}R_B)$ is the voltage gain of the local feedback stage. The 3-dB bandwidth of ACG TIA can improve by factor of $(1+g_{mB}R_B)$ than

common-gate configuration. For example, if we set g_{mB} = 20-mA/V and R_B = 500-Ω, then we can achieve higher input pole than common-gate TIA by factor of 11.

2.2.2 TIA Gain Stage and DC Offset Cancellation

The gain stage of TIA is shown in Fig 2.13, which is based on Cherry-Hooper architecture with active feedback. Let C_1 and C_2, respectively, represent the parasitic capacitance at the drain node of M_1 and M_3, G_{m1} and G_{m2} denote the transconductance of the differential pair $(M_1 – M_2)$ and $(M_3 – M_4)$, and G_{mF} be the transconductance of the active feedback stage $(M_{F1} – M_{F2})$. Such an arrangement employs a transconductance stage G_{mF} to return a fraction of the output to the input of G_{m2}. Unlike the conventional Cherry-Hooper amplifier, active feedback does not resistively load the transimpedance stage. The conversion gain of the gain stage can be derived as:

$$\frac{v_{out}}{v_{in}} \approx \frac{A_v \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.16}$$

where

$$A_v = \frac{G_{m1} G_{m2} R_1 R_2}{1 + G_{m2} G_{mF} R_1 R_2} \tag{2.17}$$

$$\zeta = \frac{1}{2} \frac{R_1 C_1 + R_2 C_2}{\sqrt{R_1 R_2 C_1 C_2 (1 + G_{mF} G_{m2} R_1 R_2)}} \tag{2.18}$$

$$\omega_n = \sqrt{\frac{1 + G_{mF} G_{m2} R_1 R_2}{R_1 R_2 C_1 C_2}} \tag{2.19}$$

For a maximally Butterworth response, the 3-dB bandwidth of the gain stage is about ω_n. In addition, the active feedback can increase the GBW of the gain stage beyond the technology f_T [12].

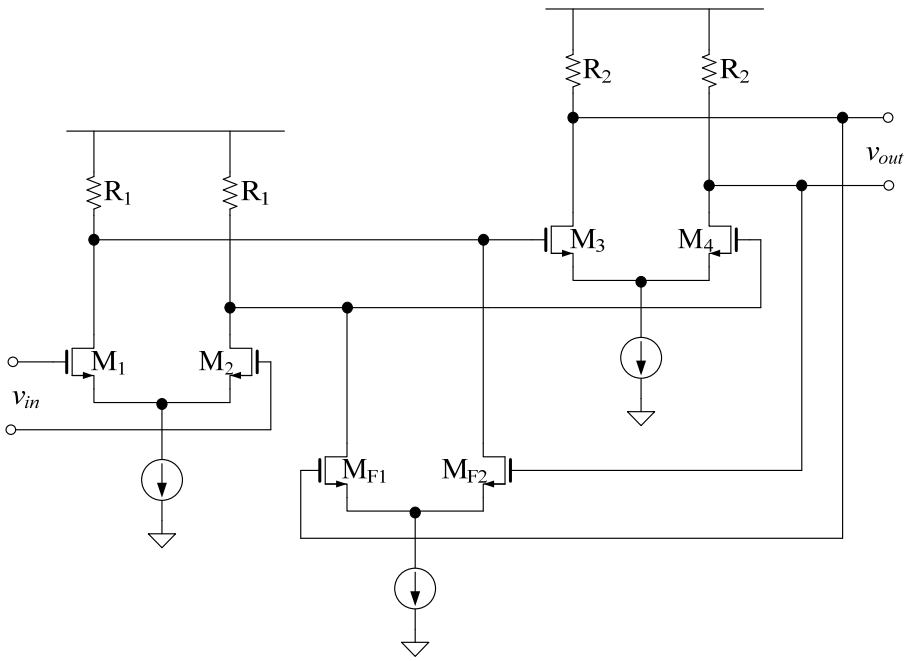


Figure 2.13 TIA Gain Stage

Transimpedance amplifier has inherently pseudo differential structure, as shown in Fig. 2.10. Therefore, symmetric differential signals may have dc offset errors. These errors gradually become large as passing the stages, thus dc-offset cancellation stage is required. Fig.

2.14 shows schematic of DC offset cancellation circuit using f_T doubler topology. The DC levels of differential input signals are extracted by on-chip passive low pass filter (LPF), and mixed at output node. The input parasitic capacitance, look into the gate of M2, is seen to the half of gate capacitance of M2, by using f_T doubler topology. Therefore, this stage can effectively eliminate dc-offset errors without the discrepancy of bandwidth [13].

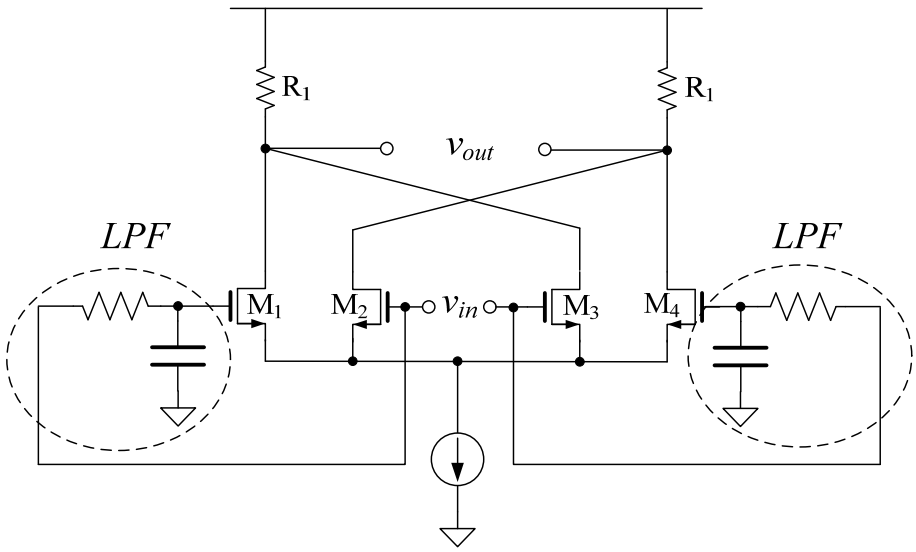


Figure 2.14 DC Offset Cancellation Circuit with on-chip passive LPF

2.2.3 Limiting Amplifier Gain Stage and Output Buffer

The gain stage of LA is shown in Fig 2.15, which is basically equal to the gain stage of TIA. The active feedback between two

transconductance stages can enhance the total bandwidth of limiting amplifier (see section 2.2.2). However, intermediate node (X) between two common-source stages very capacitive, since this node exhibits three active device (M_1, M_{F2}, and M_5). To compensate this parasitic capacitance, negative capacitance compensation is added [14]. Negative capacitance (Z_C) is given by:

$$Z_C = -\frac{1}{sC}\frac{g_m + s(C_{gs} + 2C)}{g_m - sC_{gs}} \approx -\frac{1}{sC}\frac{g_m + s(C_{gs} + 2C)}{g_m}, \; s << f_T \qquad (2.20)$$

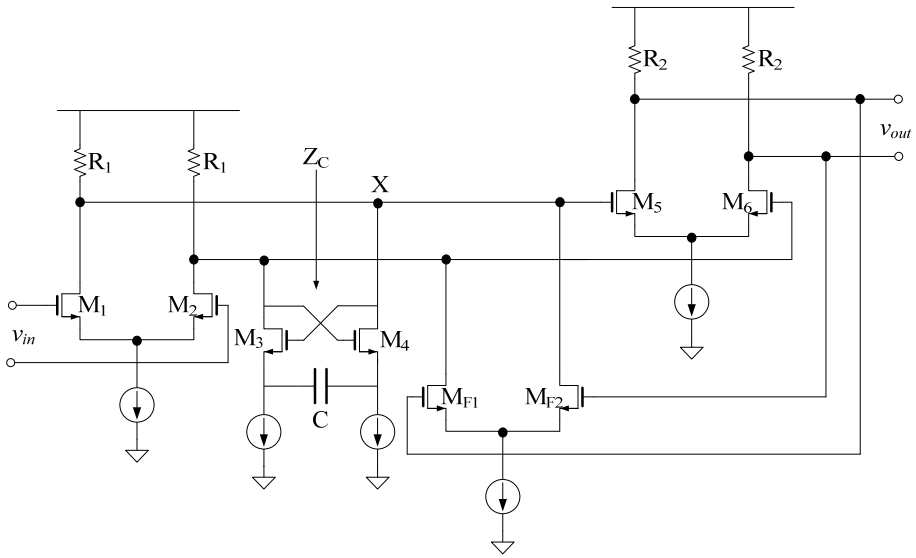


Figure 2.15 Schematic of Limiting Amplifier Gain Stage

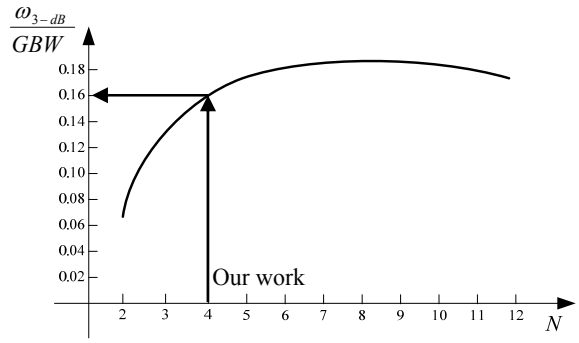


Figure 2.16 Normalized bandwidth versus N for A_{tot} = 40-dB

Fig 2.16 illustrates normalized bandwidth as a function of the number of stage of LA for desired total voltage gain, 40-dB. The maximum bandwidth appears at N=10, approximately. However, as N goes from 5 to 10, the bandwidth increases by less than 15%. Furthermore, with N=10, the gain per stage is small, making the noise contributed by all of the stages significant. For these reasons, we set the number of LA gain stage to four [15].

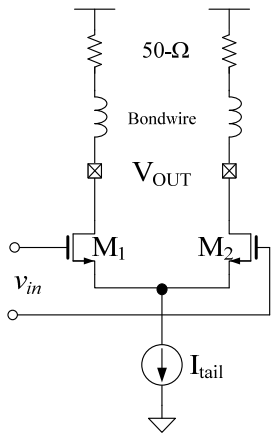


Figure 2.17 Open-Drain Output Buffer

As shown in Fig 2.17, output buffer employing the open-drain differential pair configuration drive the off-chip 50-Ω terminations and help the measurements of the output voltage and eye pattern. And tail current value determine the output voltage swing, (V_{DD}-$50 \cdot I_{tail}$). We set the differential output swing to 600-mV for CDR to operate properly.

2.3 Post-Layout Simulation Results

Post-layout simulations were conducted for the designed optical receiver by using the model parameter of a standard 0.13-μm CMOS technology. The total parasitic capacitance at the input is estimated ~0.3-pF including photodiode parasitic capacitance (0.25-pF), bonding pad capacitance (25-fF), and the gate capacitance of input transistor. Fig 2.18 illustrates frequency response of optical receiver, exhibiting 6.6-GHz bandwidth for 10-Gb/s operation and 96-dBΩ transimpedance gain. The bandwidth is optimized to 60~70 % of bit rate, considering tradeoff between noise and ISI.

Fig 2.19 shows *Input-Referred Noise Current Density*. The average Input-Referred Noise Current Density is ~22-pA/sqrt(Hz), which corresponds to input sensitivity of -16.5-dBm for 10^{-12} BER and 0.7-A/W responsivity.

The eye patterns according to received optical power are presented

in Fig 2.20. Optical receiver maintains its output voltage to 600-mVpp (differential) against received optical power variation from -18-dBm to -1.5-dBm. Input dynamic range is ~40-dB, and the power dissipation is 54-mW from a single 1.2-V supply.

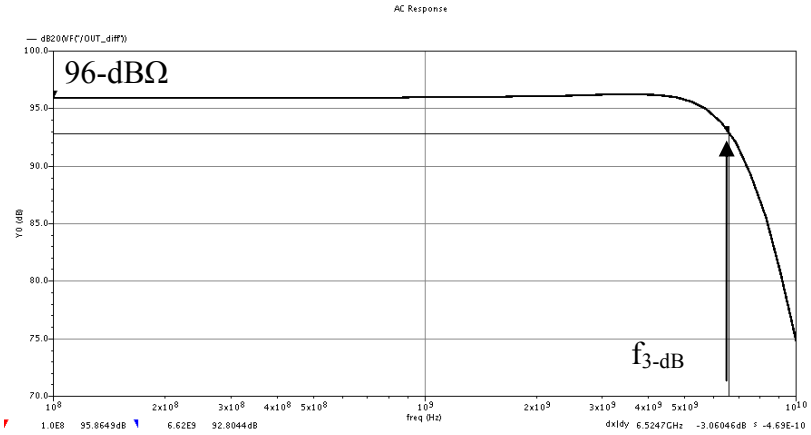


Figure 2.18 Frequency Response of Optical Receiver

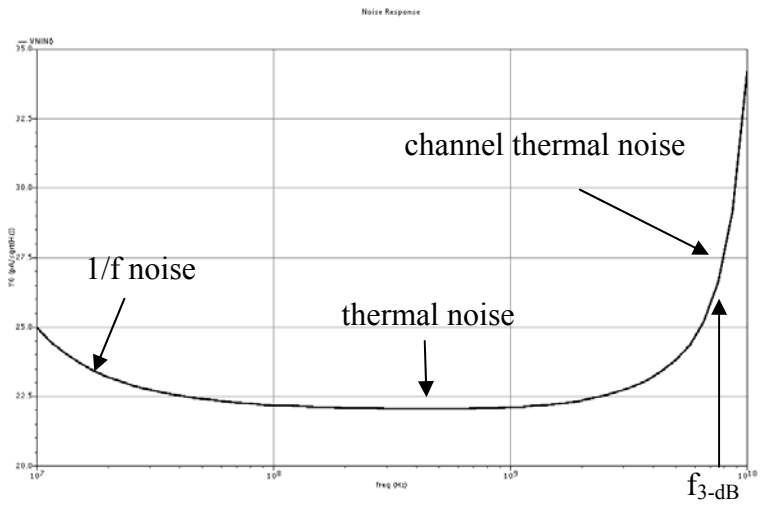
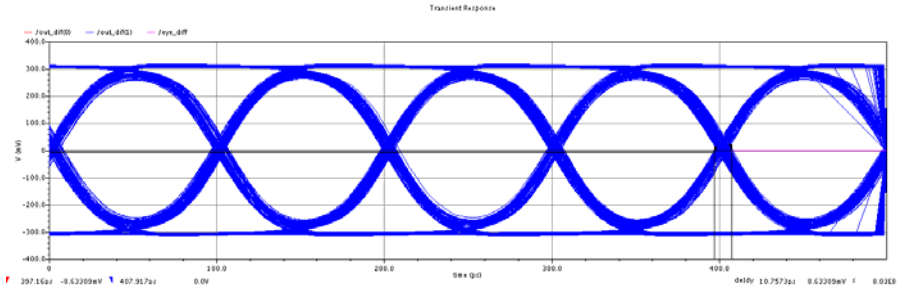
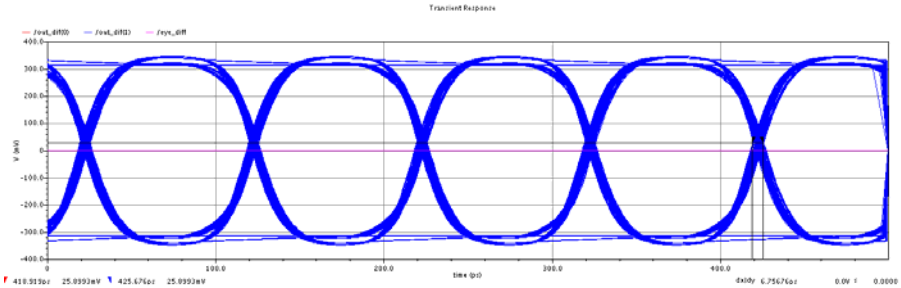


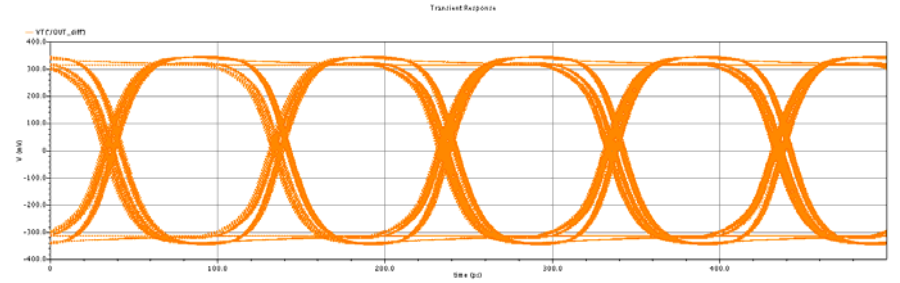
Figure 2.19 Input-Referred Noise Current Spectrum



(a)



(b)



(c)

Figure 2.20 Eye Patterns According to Received Optical Power @10-Gb/s, (a) -18.45-dBm (10-uA), (b) -8.45-dBm (100-uA), (c) -1.5-dBm (500-uA)

CHAPTER Ⅲ

Design of 10-Gb/s VCSEL Driver

3.1 Background

3.1.1 VCSEL

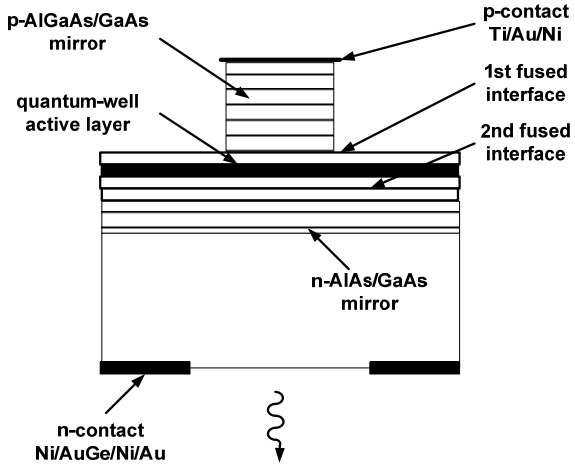


Figure 3.1 Structure of VCSEL

The Vertical-Cavity Surface-Emitting Laser (VCSEL) is a SLM laser like the DFB/DBR laser, however, its line width is not as narrow. The distinguishing feature of a VCSEL is that it emits the light perpendicular to the wafer plane. The VCSEL consists of a very short vertical cavity (about 1-μm) with Bragg mirrors at the bottom and the top, as shown in Fig 3.1. The advantage of VCSEL is that they can be fabricated, tested, and packaged more easily and at a lower cost. However, the very short gain medium requires mirrors with a very high

reflectivity to make the net gain larger than one. Currently, VCSELs are commercially available only at short wavelengths (850-nm band) where fiber loss is appreciably high. Their application is mostly in data communication systems using multi-mode fiber (MMF).

The static relationship between the laser current I_L and the light output P_{out}, the so-called L/I Curve, is shown schematically in Fig 3.2. Up to the so-called *Threshold Current*, I_{TH} , the laser outputs only a small amount of incoherent light (like a LED). In this regime the optical gain isn't large enough to sustain lasing. Above the threshold current the output power grows approximately linearly with the laser current as measured by the *Slope Efficiency*. Typical values for an edge-emitting InGaAsP MQW laser are I_{TH} = 5-mA, and a slope efficiency of 0.07-mW/mA. Thus for I_L = 25mA (= 10-mA + 15-mA) we obtain about 1-mW optical output power. VCSELs are characterized by a lower threshold current and a better slope efficiency, while LEDs have zero threshold current and a much lower slope efficiency.

The slope efficiency is determined by the *Differential Quantum Efficiency* (DQE) which specifies how efficiently electrons are converted into photons. Just like in the case of the photodiode, we have the situation that optical power is linearly related to electrical amplitude, which means that we have to be careful to distinguish between

electrical and optical dBs.

As indicated in Fig 3.2 the laser characteristics, in particular I_{TH}, are strongly temperature and age dependent. For example a laser that nominally requires 25-mA to output 1mW of optical power, may require in excess to 50-mA at 85 ◦C and near the end of life to output the same power. The temperature dependence of the threshold current is exponential and can be described by:

$$I_{TH}(T) = I_0 \cdot \exp(\frac{T}{T_0}) \tag{3.1}$$

where I_0 is a constant and T_0 is in the range of 50 − 70K for InGaAsP lasers. The temperature dependence of the laser's slope efficiency is less dramatic, a 30−40% reduction when heating the laser from 25 to 85 ◦C is typical.

Because of the strong temperature and age dependence of the laser's L/I curve all communication lasers have a built-in monitor photodiode which measures the optical output power at the back facet of the laser. The current from the photodiode closely tracks the optical power coupled into the fiber with little dependence on temperature and age, a tracking error of ±10% is typical. The monitor photodiode can be used to implement an *Automatic Power Control (APC).*

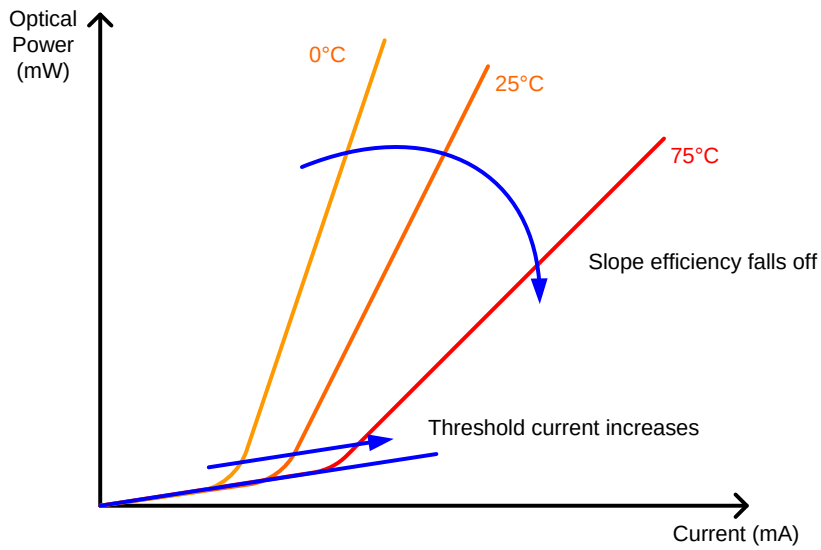


Figure 3.2 L-I Curves for a Semiconductor Laser

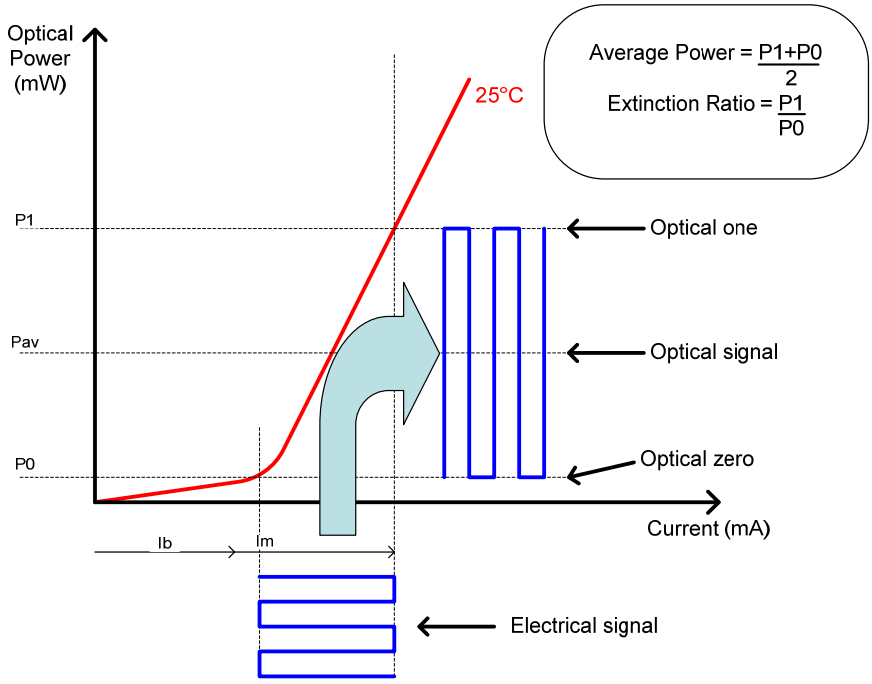


Figure 3.3 Average Optical Power and Extinction Ratio

3.2 Design of VCSEL Driver

3.2.1 Pre-Amplifier with LVDS/CML compatible

Pre Amplifier of VCSEL Driver has same structure to the gain stage of LA, as depicted in Fig 2.15. Pre amplifier consists of two gain stages to boost high frequency gain. And first amplifier has LVDS/CML compatible input configuration by adding mid tap control voltage (VT), as presented in Fig 3.4. In CML mode, allowable input swing is 150-mV to 1-V, so have wide dynamic range. For high speed operation, CML mode is rather than LVDS mode [16].

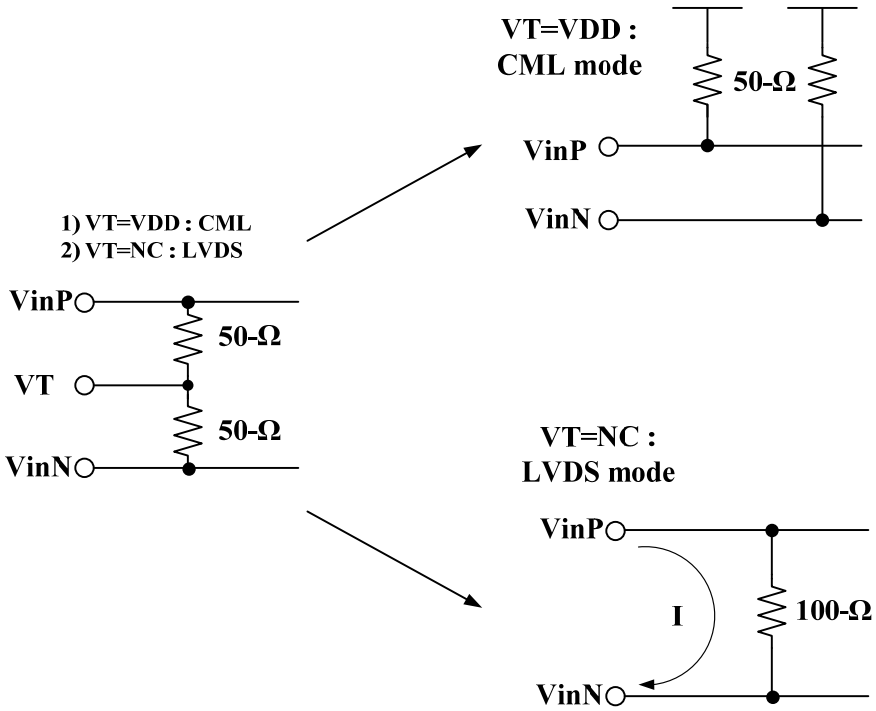


Figure 3.4 CML/LVDS Compatible Input Configurations

3.2.3 Open-Drain Output Driver

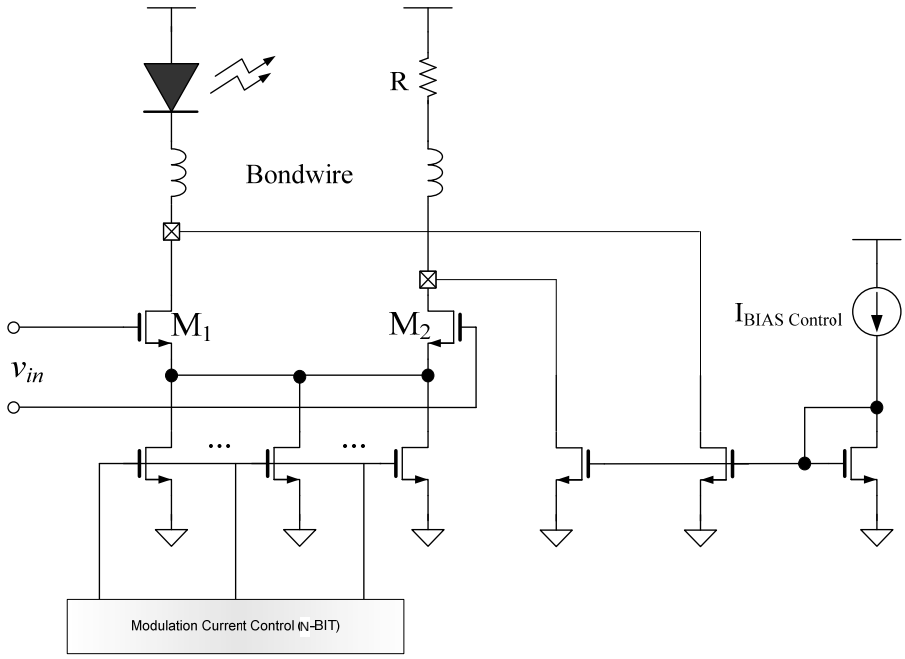


Figure 3.5 Output Driver with Bias and Modulation Control

Fig 3.5 shows the schematic of output driver. I_{MOD} represents the modulation current of VCSEL, corresponding to the optical output swing range, whereas I_{BIAS} is the bias current of VCSEL which corresponds to the average transmitted optical power. When the bias current is greater than the nominal threshold current, it guarantees that the VCSEL operates properly. Since the characteristics of VCSEL changes with time and temperature, I_{MOD} and I_{BIAS} can be controlled externally. Bias and modulation current are handled the maximum 15-mA and 20-mApp, respectively [17], [18].

3.3 Simulation Results

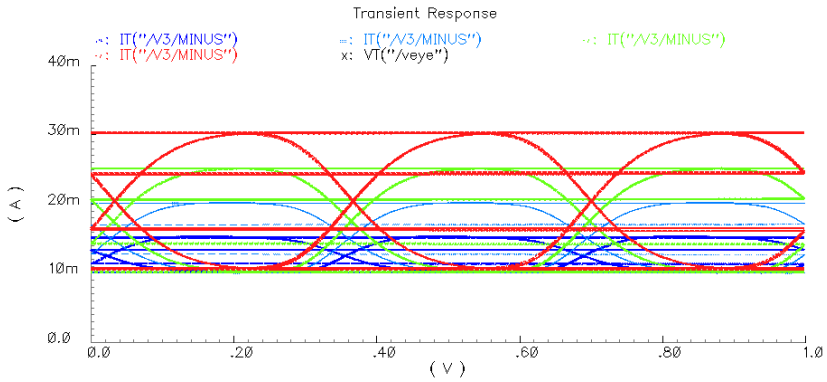


Figure 3.6 Eye Patterns with I_{MOD} Control

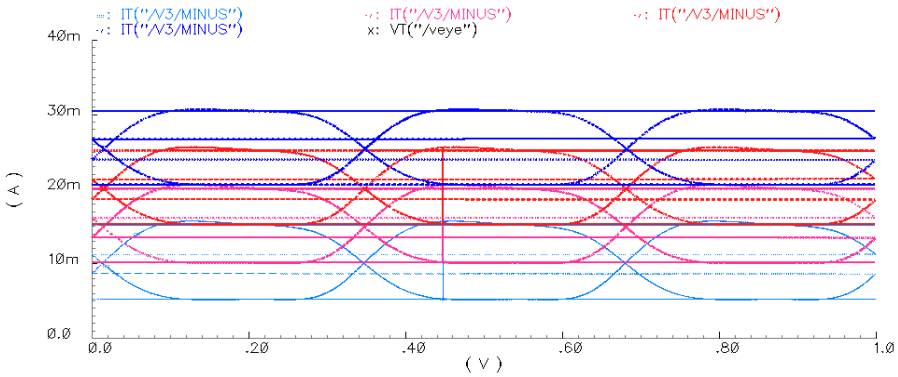


Figure 3.7 Eye Patterns with I_{BIAS} Control

Optical transmitter analog front-end consists of LVDS/CML compatible pre amplifier and main driver. The designed transmitter drives VCSEL, operating up to 10-Gb/s with bias control (5~20-mA) and modulation control (5~20-mApp) to obtain constant and reliable optical output power against age and temperature effect, as presented in Fig 3.6 and Fig 3.7 [19].

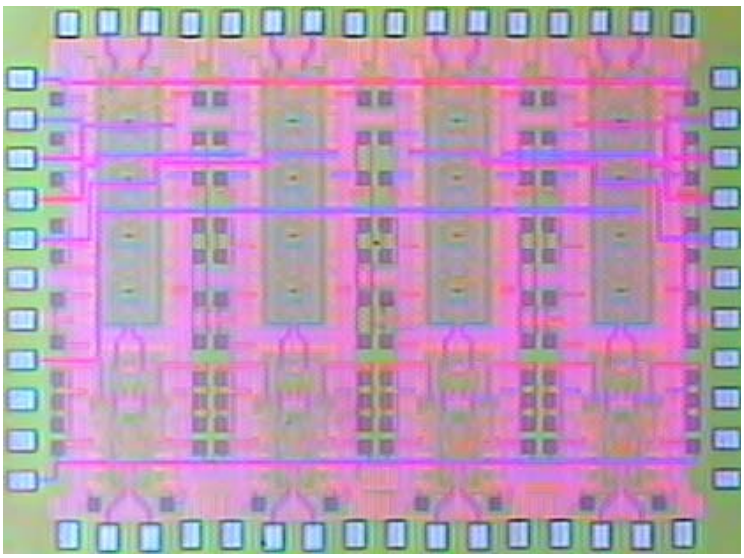
CHAPTER Ⅳ

IC Fabrication and Experiment Results

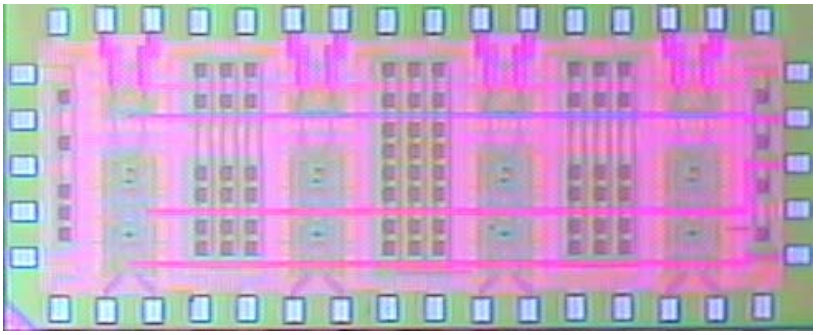
4.1 IC Fabrication

10-Gb/s optical receiver and VCSEL driver were fabricated using a TSMC 0.13-μm mixed signal / RF process. This CMOS process has a silicide block, thick gate oxide (3.3V), deep N-well, thick top metal, and MiM capacitor options.

Fig. 4.1 shows the microphotograph of fabricated optical receiver and VCSEL driver. Optical receiver and VCSEL driver occupies the area of 1.8 x 1.35 mm^2 and 2.05 x 0.83 mm^2, respectively.



(a)



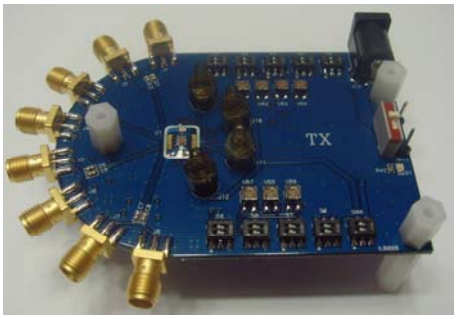
(b)

Figure 4.1 Microphotographs of Fabricated 10-Gb/s (a) Optical Receiver and (b) VCSEL Driver

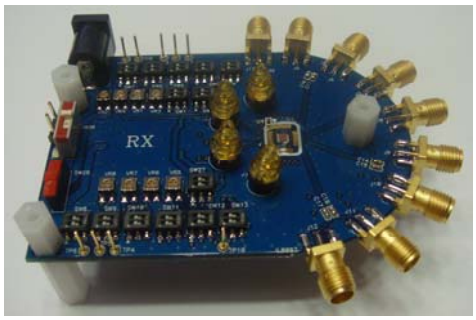
4.2 Experiment Results

4.2.1 Printed Circuit Board Design

Fig. 4.2 is a picture of the fabricated FR4 printed circuit boards (PCBs) of optical receiver and VCSEL driver. We exploit commercial TO-CAN type p-i-n photodiode and VCSEL, operating up to 10-Gb/s. The photodiode has parasitic capacitance of 0.25-pF and responsivity of 0.7-A/W, and requires reverse bias voltage of 3.3-V. VCSEL exhibits parasitic capacitance of 0.2-F and extinction ratio of ~9-dB.



(a)



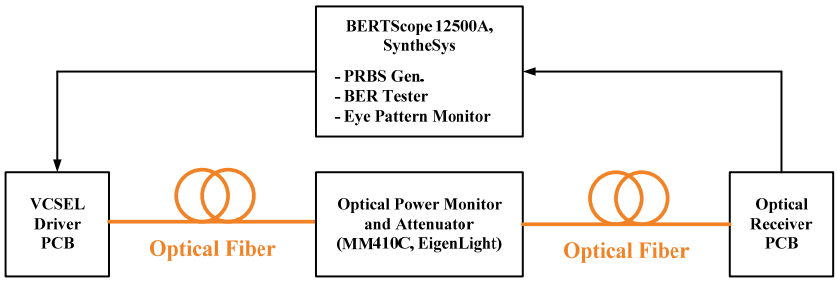
(b)

Figure 4.2 Evaluation Boards of (a) Optical Receiver and (b) VCSEL Driver

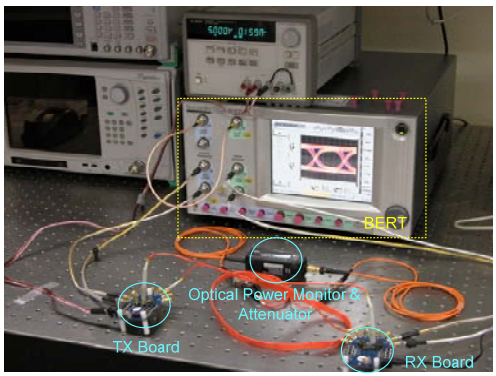
4.2.2 Test setup

Fig. 4.3 illustrates the block diagram and real picture of measurement setup for testing optical receiver and VCSEL driver. A BERTScope 12500A of SyntheSys generates differential modes of pseudo random bit streams (PRBS) and measures the probability of a received data error rate and eye patterns through full optical links. And

MM410C (optical power monitor and attenuator) can vary incident optical power to receiver board and help the measurement of BER. For optical measurements, 850-nm VCSEL diode and p-i-n photodiode are utilized as an optical source and detector, respectively. The VCSEL exhibits 9-dB extinction ratio and the photodiode yields the responsivity of 0.7-A/W at 850-nm with parasitic capacitance of 0.25-pF and parasitic resistance of 20-Ω.



(a)



(b)

Figure 4.3 Test Setup for Optical Links: (a) Block Diagram and (b) Real Picture

4.2.3 Measurement

Fig. 4.4 shows the measured optical eye patterns of the complete optical link at different data rates of 1.25-Gb/s, 2.5-Gb/s, 5-Gb/s, and 10-Gb/s 2^{31}-1 PRBS. The maximum single-ended voltage swing is measured to be 500-mVpp and the typical single-ended voltage swing under optimum bias condition is measured to be 300-mVpp, corresponding to the best jitter and BER performance. The peak-to-peak jitter is measured to be less than 32-psec, corresponding to 0.68-UI eye opening at 10-Gb/s operation.

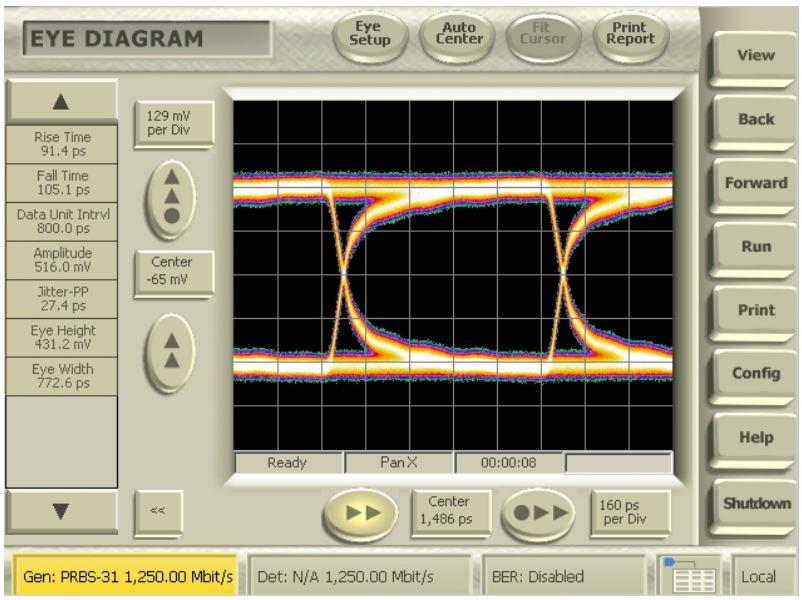
Fig. 4.5 shows the measured BER of receiver according to received optical power, which can be controlled by optical power attenuator (MM410C). The optical sensitivity through the complete optical link is measured to be -14-dBm for 10^{-12} BER with 10-Gb/s 2^{31}-1 PRBS. This 4-dB difference between measured and simulated values may be attributed to the coupling loss between VCSEL, optical fiber, and p-i-n photodiode, and the insertion loss from attenuator. The optical power attenuator (MM410C) exhibits insertion loss of 2-dB and total connector loss of 0.37-dB. Therefore, real sensitivity of receiver is expected to more than -16.5-dBm. Measurement results of optical link are summarized in Table 1.

The performance comparison of this paper, the prior art of

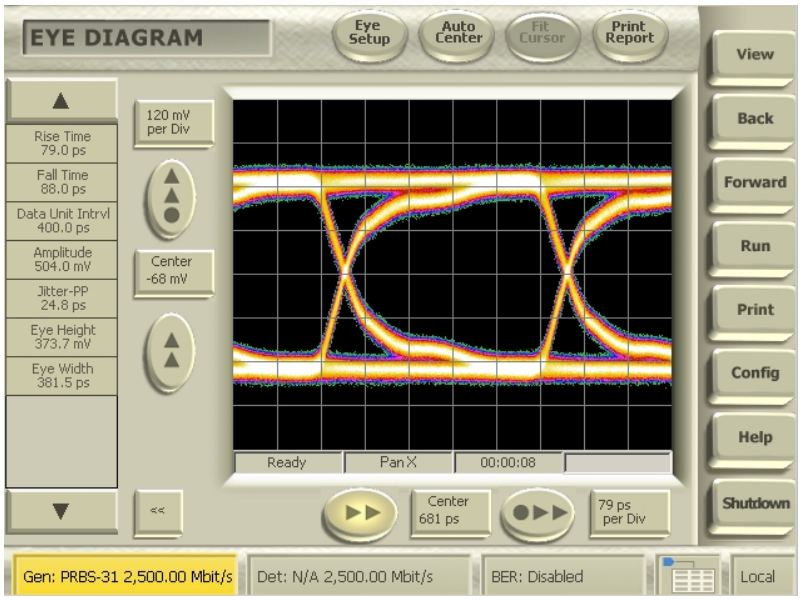
transimpedance amplifiers and limiting amplifiers [1]-[3] is summarized in Table 2. FOM of this table is defined as follows:

$$FOM = \frac{GBW}{f_T}\ (THz-\Omega/GHz) \tag{4.1}$$

where GBW is gain-bandwidth product and f_T is cut-off frequency of process. f_T is added for equitable comparison with previous works. Our work exhibits 4.55(THz-Ω/GHz) of FOM, which is better than other 10-Gb/s optical receiver chipset [1], [2]. Also, unlike [1] and [2], this work does not exploit passive inductor. Therefore, our chipset can occupy small area.



(a)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Eye Setup
Auto Center
Fit Cursor
Print Report
View
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Forward
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Config
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Rise Time 79.0 ps
Fall Time 88.0 ps
Data Unit Intrvl 400.0 ps
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120 mV per Div
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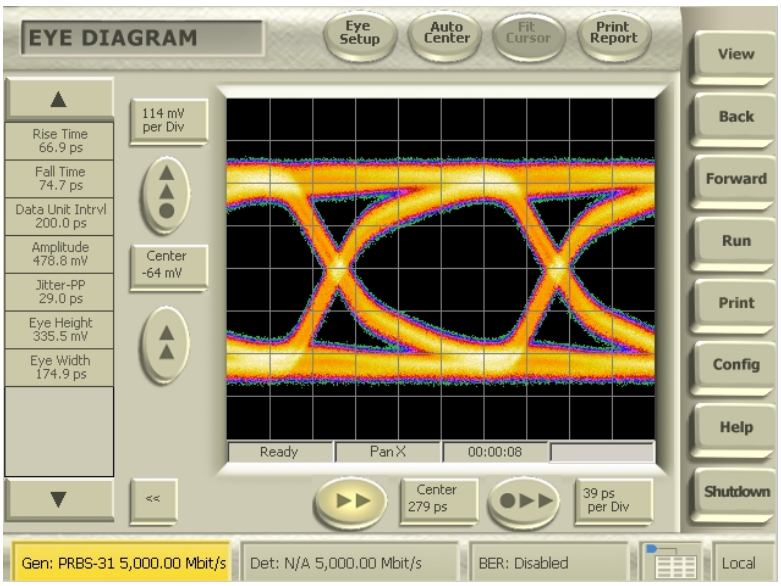
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Eye Setup
Auto Center
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Shutdown
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Fall Time 74.7 ps
Data Unit Intrvl 200.0 ps
Amplitude 478.8 mV
Jitter-PP 29.0 ps
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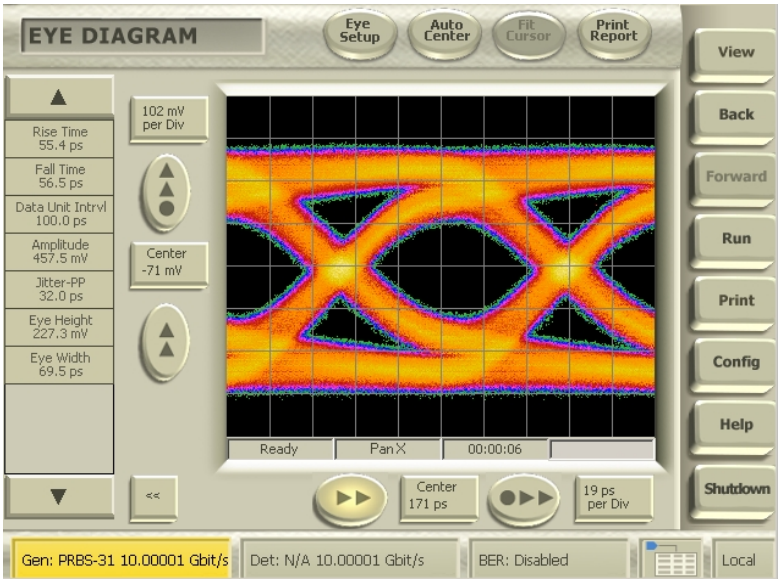

(d)

Figure 4.4 Eye Patterns of the Complete Optical Link at Various Data Rates: (a) 1.25-Gb/s, (b) 2.5-Gb/s, (c) 5-Gb/s, and (d) 10-Gb/s

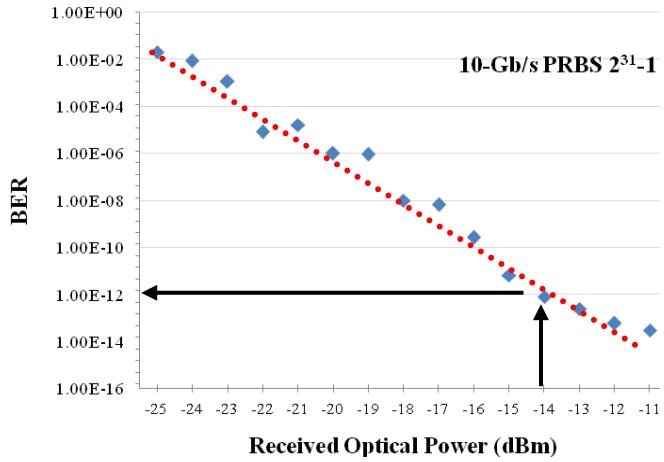

Figure 4.5 Measured Bit Error Rates according to the Received Optical Power for 10-Gb/s 2^{31}-1 PRBS

Table 1 Measurement Results of TX and RX

Parameter	Measurement Results	
	TX	RX
Process	0.13-μm CMOS	
Supply Voltage	1.8-V	1.2-V
Data Rates	Up to 10-Gb/s	Up to 10-Gb/s
Parasitic Capacitance	0.25-pF	0.2-pF
Transimpedance Gain	-	96-dBΩ
Sensitivity (10^{-12} BER)	-	-16.5-dBm[1)]
Peak-to-Peak Jitter	-	< 32-ps
Eye Opening	-	0.68-UI
Output Swing (single-ended)	20-mA_{pp} (Max.) 5-mA_{pp} (Min.)	500-mVpp (Max.) 300-mVpp (Typical)
Power Dissipation	50-mW	54-mW
Chip Size (mm^2)	2.05 × 0.83[2)]	1.8 × 1.35[2)]

1) Sensitivity of receiver is estimated considering the loss of optical attenuator (~2.5-dB), above mentioned.

2) Chip size occupies the area of 4-channel driver array and receiver array including ESD protection diode pads.

Table 2 Performance Comparison of Optical Receiver

Spec.	**This work**	[1] 07'VLSI	[2] 05'JSSC	[3] 06'TCS
Function	**TIA+LA**	TIA+LA	TIA+LA	TIA+LA
Power Dissipation	**54-mW (1.2-V)**	199-mW (1.8-V)	210-mW (1.8-V)	99-mW (3-V)
Process	**0.13-μm**	0.18-μm	0.18-μm	0.35-μm
#Inductors	**0**	7	9	0
Data Rate	**10-Gb/s**	10-Gb/s	10-Gb/s	2.5-Gb/s
Gain	**96-dBΩ**	90-dBΩ	87-dBΩ	96.5-dBΩ
FOM (THz-Ω/GHz)	**4.55**	4.14	2.83	4.9

CHAPTER Ⅴ

Conclusion

In this dissertation, 10-Gb/s optical receiver and VCSEL driver are designed and implemented in 0.13-μm CMOS technology.

Optical receiver includes transimpednace amplifier and limiting amplifier. For the efficient isolation from the photodiode capacitance, the advanced common-gate configuration is exploited as an input stage. To satisfy the requirements for limiting amplifier, such as high voltage gain, wide bandwidth, and wide input dynamic range, the active feedback amplifier with negative impedance compensation has been realized as a gain stage of LA.

VCSEL driver array consists of two stage pre amplifier with LVDS/CML compatible input configuration and main driver. For 10-Gb/s operation, the active feedback gain stage is exploited as a pre amplifier, too. To obtain constant and reliable optical output power, bias current and modulation current can be controlled.

The designed 10-Gb/s optical receiver and driver chipset provides high speed solution with low area and cost due to the absence of passive inductor. They can apply to long distance applications such as

SONET, LAN and MAN as well as short-haul applications, such as FTTx (curb, home, building, office, and desktop), board-to-board communication, chip-to-chip communication, and so on.

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국문요약

CMOS 0.13-μm 공정을 이용한
10-Gb/s 광 수신기와 VCSEL 구동 회로

본 논문에서는 10-Gb/s의 전송속도를 갖는 광 수신기와 VCSEL 구동회로를 CMOS 0.13-μm 공정으로 설계 및 구현하였다. 광 통신 시스템에서 아날로그 front-end단은 전체 시스템의 속도와 잡음특성에 영향을 주는 가장 중요한 요소이다. 따라서 이러한 회로들은 일반적으로 높은 속도와 낮은 잡음특성을 갖는 GaAs, InP, HEMT와 같은 화합물 반도체 공정으로 제작되었다. 그러나 매우 작은 채널길이를 갖는 CMOS 공정이 낮은 비용과 높은 집적도 때문에 화합물반도체를 대체할 공정으로 대두되고 있다. 또한 10-Gb/s 이상의 속도를 갖는 광 송수신기는 대역폭을 향상 시키기 위한 방법으로 큰 면적을 갖는 수동 인덕터 소자를 사용하는 것이 일반적이었다. 본 논문에서는, 10-Gb/s의 속도를 갖는 광 송신기와 수신기를 값싼 CMOS 공정으로 수동 인덕터 없이 구현함으로써 칩셋의 면적과 가격을 크

게 낮출 수 있다.

광 수신기는 Transimpedance amplifier (TIA)와 Limiting amplifier (LA) 로 구성된다. 향상된 공통 게이트 입력단 (ACG)은 매우 작은 입력 임피던스 특성을 나타내므로 광검출 소자의 큰 기생 커패시터를 회로내부와 효과적으로 격리시킬 수 있어서 대역폭을 크게 향상시킬 수 있다. LA의 증폭단은 능동 궤환회로와 부임피던스 기술을 이용하여 넓은 대역폭을 확보할 수 있었다. 본 논문에 사용된 광 검출기는 0.7-A/W의 responsivity, 0.25-pF의 기생 커패시터를 갖고 있다. 광 수신기는 10-Gb/s에서 동작할 수 있도록 6.6-GHz의 최적화된 대역폭을 갖도록 설계하였으며, 96-dBΩ의 변환이득을 갖는다. 또한 22-pA/sqrt(Hz)의 입력 잡음 전류 밀도를 갖고 있어서, -16.5-dBm의 광 파워로 10^{-12} BER을 만족시킬 수 있다. 전체 광 수신기는 1.8 × 1.35 mm^2 의 칩 사이즈를 가지며, 1.2-V의 공급전압을 사용하고 54-mW의 전력을 소모한다.

광 송신기는 CML과 LVDS 형식의 입력신호가 모두 가능한 전치증폭기와 VCSEL 구동회로로 구성된다. 설계된 광 송신기는 VCSEL을 구동하며 10-Gb/s의 속도로 동작한다. 또한 일정한 광 출력을 유지하기 위해 바이어스전류 (5~20-mA)와 변조전류 (5~20-mA)를 조절할 수 있다. 전체 칩 사이즈는 2.05 × 0.83 mm^2 이며, 1.8-V 공급전압에서 50-mW의 전력을 소모한

다.

본 연구에서 설계된 광 송신기와 광 수신기는 SONET, LAN, MAN 등으로 대표되는 기존의 장거리 광통신 시스템뿐만 아니라 FTTx (curb, home, building, office, desktop) 등의 저가형 광통신 시스템, 그리고 board-to-board, chip-to-chip 통신 등의 단거리 통신에 이르기까지 넓은 응용 분야에서 사용될 수 있을 것으로 기대된다.