Radiation Hardened Bandgap Reference Circuit with Radiation Effect Rejection by Using Reference Voltage Subtraction

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Radiation Hardened Bandgap Reference Circuit with Radiation Effect Rejection by Using Reference Voltage Subtraction

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Abstract

Radiation Hardened Bandgap Reference Circuit with Radiation Effect Rejection by Using Reference Voltage Subtraction

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This thesis is about the radiation hardened bandgap reference (BGR) circuit with radiation effect rejection by using reference voltage subtraction. The bandgap reference circuit is an essential circuit that supplies a constant voltage to the various sensors and circuit systems. Particularly, the thermocouple sensor interface with BGR is used to monitor and control the reactor and other equipment in the nuclear power plant for safe operation. However, cumulative damage is occurred when a semiconductor integrated circuit is used in a radiation environment, which changes the threshold voltage and increases the leakage

current. The change of the characteristics of semiconductor devices causes the operating point change of the BGR, resulting in tens of degree of error.

In previous studies, methods for minimizing radiation effects were proposed using Enclosed Layout Transistor (ELT). However, there are disadvantages such as difficulties in design and simulation using ELT structures and large area demand. Therefore, the standard 0.18 μm process was used in this thesis to implement radiation hardened by design (RHBD) BGR.

The proposed circuit utilizes the difference between two reference voltages with identical characteristics for temperature and radiation but different voltage level. The radiation characteristics are identical when two equal BGRs are irradiated by radiation in the uniform radiation field. If the supply voltage of the two BGRs is different, the output voltage changes due to the channel-length modulation effect in the saturation region, resulting in a decreased output reference voltage. This allows two circuits to having different output voltage level, while have the same temperature and radiation characteristics. Finally, the difference between two reference voltages is output through a voltage subtractor composed of OPAMP.

The experiment was conducted according to temperature and radiation changes to compare the output of the conventional BGR and the proposed BGR. The temperature experiment was conducted from 20°C to 110°C. As a result of the experiment, The maximum voltage variation of the proposed design shows 0.26 mV, while conventional circuit produces 26 mV, and the TC is 2.9 and 289 ppm/℃, respectively. Radiation testing was conducted for 20 hours at 100 krad per hour using a Co-60 source. The result of the radiation experiment shows that the conventional BGR shows the maximum radiation error of 16.7 mV and average error of 13 mV, while the proposed design shows 9.5 and 5.2 mV, respectively. Therefore, the proposed reference voltage supply was assessed to be 97.45 % more stable for temperature and 60 % more stable for radiation.

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1. Introduction

An analog-digital converter (ADC), a digital-analog converter (DAC), a temperature sensor, and a voltage regulator circuit requires high accurate and stable bias voltage to set the operating point. Therefore, the circuit performance is determined by the biasing circuit. Conventionally, a passive bias circuit composing the resistor are used. However, this biasing circuit is variated by external environment such as the temperature, process and supply voltage variation and so on. Today, the BGR is widely used instead of passive bias circuit [1]. It can generate the constant voltage regardless of external environment. The conventional BGR should provide the constant voltage to other circuits. Robert John Widlar, who was an American electronics engineer and a designer, demonstrated that proportional-to-absolute-temperature (PTAT) voltage was generated by scaling bipolar junction transistor (BJT) at 1971 [2]. Since then, the bandgap reference circuit is an essential block for various sensor and circuit systems. The bandgap reference circuit could produce constant voltage about 1.25

V to the circuit system [3]. This value is same about the silicon bandgap voltage. Therefore, this circuit is called as bandgap reference circuit.

Particularly, thermocouple sensors with BGR are widely installed in nuclear power plants (NPPs) to monitor and control reactors and other equipment for safe operation [4, 5]. Thermocouple sensor has the advantage of the low cost, wide measurement rage, stability, fast response and so on. Therefore, they are used in many industries [5, 6]. However, in the radiation field, the thermocouple sensor integrated circuit (IC) is affected by radiation. In the case of k-type thermocouple, output voltage is around 41.6 μV/℃. Therefore, a few mV errors at a BGR can result in tens of degree of error in temperature. For this reason, a reference voltage should supply a constant value to retain a sensor stable regardless of external environments.

The development of space, military, medical and nuclear industries has required the radiation harden device during tens of year. So, many technologies have been developed to resist against the radiation. A silicon-on-insulator (SOI) or a silicon-on sapphire (SOS) technologies increase inherent tolerance to the single event effect (SEE) [7]. In addition to, CMOS process scaling down reduce a total ionizing

dose (TID) effect due to electron tunneling effect. The hole induced by radiation is recombination with the electron moved from channel in the SiO_2-Si interface. Moreover, an ELT structure decreases the TID effect [7 - 11]. The ELT device has isolated gate structure that prevent to generate parasitic channel caused threshold voltage shift [12]. However, in the analog circuit aspect, the layout of ELT devices requires a wide area about three times larger than a standard metal-oxide-silicon field effect transistor (MOSFET) process. Moreover, it is difficult to develop an accuracy model for electrical response simulations [13]. The CMOS scaling down cause shallow trench isolation region (STI) to avoid the interference with adjacent devices. So, STI increase the leakage current when the CMOS is irradiated [7]. For this reason, it is necessary to research the RHBD analog circuit using standard MOSFET instead of the ELT structure against TID effect.

2. Background

2.1 Thermocouple Temperature Sensor

The thermocouple thermometer is widely used in various industry. It has the advantage of the low cost, wide measurement rage, stability, fast response and so on. It has been also utilized in NPPs to measure temperature for the NPPs safety due to these advantages. Thermocouples have various characteristics depending on the type of metal. In the case of k-type thermocouple, consisting of chromel and alumel, output voltage is around 41.6 μV/℃ and could measure from -200℃ to 1250℃ conventionally.

2.1.1 Seebeck Effect

The critical principle of the thermocouple is Seebeck effect. It is discovered at the 1821 by Seebeck who is Germany physicist. If one side is connected to the hot junction, and the other is connected to the cold junction as known as a reference junction, a voltage difference is generated by the different temperature between two different metals [6, 14]. This phenomenon is caused by moving free electron in the two metals. Free electrons move from high temperature region to low temperature. Moreover, electrons are trapped at the low temperature region due to shorter mean free path than high temperature region. At that time, the thermal potential is generated as called as electromotive force as shown equation (1).

$$V_T = S \times (T_H - T_C) \tag{1}$$

where S is Seebeck coefficient difference of two metals, and T_H and T_C are the temperature difference between the two metals.

2.1.2 Cold Junction Compensation

The temperature can be measured by using equation (1) when the reference junction temperature is constant, which is known as cold junction compensation (CJC). There are several methods to compensate cold junction. First, the traditional method is to use the $0\,℃$ water-bath as shown figure 2.1. So, $S \cdot T_C = 0$, the output of thermocouple is defined by high temperature as shown equation (2). However, it is not commonly used in these days because the water bath is relatively bulky to use in practical sites [15].

$$V_T = S \times T_H \tag{2}$$

Second method is to correct using software. It is simple and fast method but less precise. Another approach is to utilize hardware compensation such as a CMOS integrated circuit. The bandgap reference circuit is generally used as CJC circuit because it can produce constant voltage. Therefore, the output of thermocouple is defined as shown equation (3).

$$V_{output} = V_T + V_{REF} = S \times T_H \qquad\qquad (3)$$

(a)   (b)
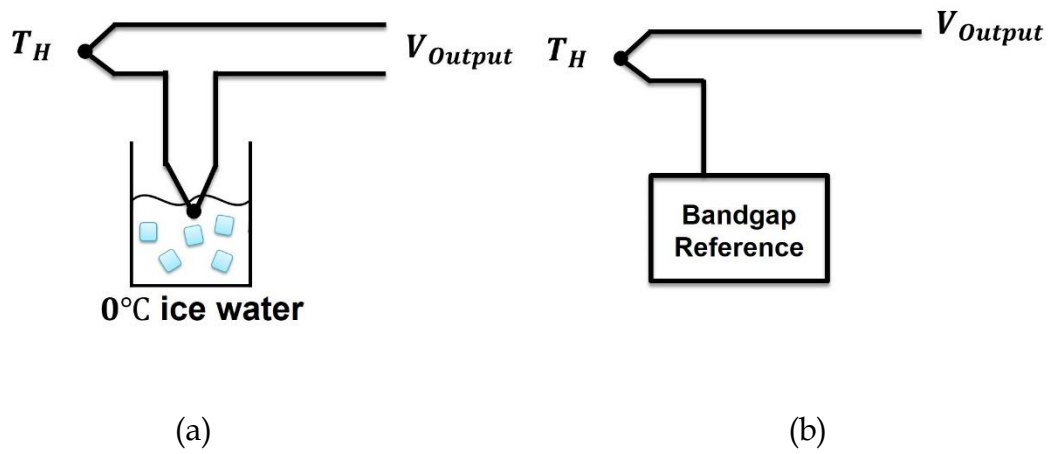
Figure 2.1 Cold junction compensation method by using (a) ice water and (b) the bandgap reference circuit.

2.1.3 Thermocouple Temperature Sensor Interface

Figure 2.2 shows a thermocouple sensor system, which consists of a k-type thermocouple, CJC circuit, and OPAMP. The k-type thermocouple is composed of chromel (positive lead) and alumel (negative lead). On the negative side, a BGR for the CJC supplies constant voltage, while the positive side is connected to an OPAMP to amplify the voltage difference. Therefore, the voltage putting the temperature sensor can be measured and calculated the target temperature using equation (3).
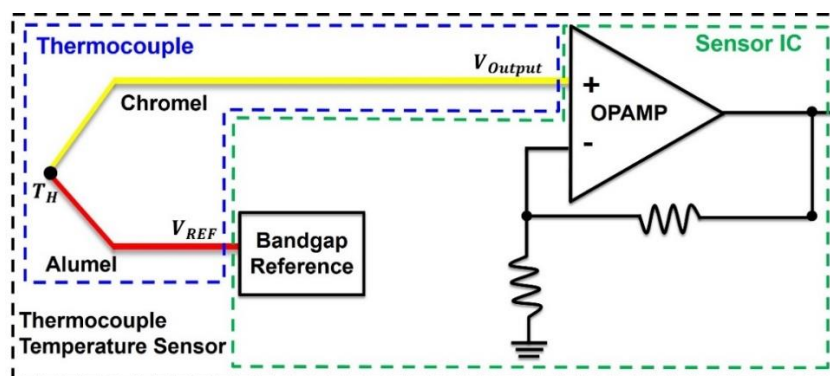
Figure 2.2 Thermocouple sensor interface block diagram. It consists of two part. One is the thermocouple and the other is sensor IC consisting of the BGR and OPAMP.

2.2 Bandgap Reference Circuit

2.2.1 Principle of Conventional BGR

The BGR is the circuit that generates the constant output voltage to the other circuits regardless of supply voltage, temperature and process variation. To maintain the output voltage constantly independence to supply voltage, beta-multiplier circuit is introduced later. The principle of conventional BGR is to add PTAT voltage and complementary-to-absolute-temperature (CTAT) to maintain the reference voltage regardless of temperature as shown in figure 2.3. The most important thing is to match property between the PTAT voltage and CTAT voltage. Conventionally, the base-emitter voltage has a temperature coefficient (TC) about -2.2 mV/℃ in the BJT device [16].

(a)

(b)
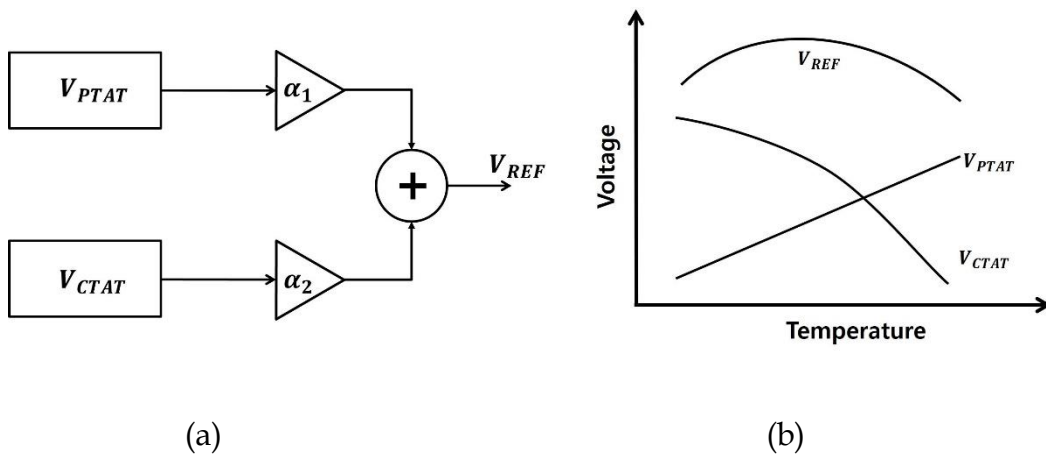
Figure 2.3 (a) Bandgap reference circuit diagram. Weighted factor is multiplied to PTAT and CTAT voltage (b) Reference voltage curve.

2.2.1.1 Current Bias Circuit

The current bias circuit is widely used to generate constant current to many analog circuits such as operational amplifier (OPAMP), BGR and voltage regulator. The conventional method to generate reference current is to use the current source consisting of resistor as shown in figure 2.4 [1].
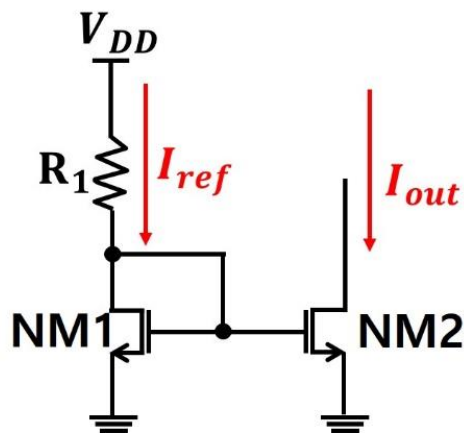
Figure 2.4 Conventional bias circuit consisting of resistor. Reference voltage flows through NM2 connecting to current mirror with NM1.

The output current is defined by reference current and the ratio of NM1 and NM2 like equation (4).

$$I_{out} = I_{ref} \times \frac{(W/L)_2}{(W/L)_1} \tag{4}$$

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_m} \times \frac{(W/L)_2}{(W/L)_1} \tag{5}$$

However, this structure is vulnerable to supply voltage variation due to ΔV_{DD} term at equation (5). The PTAT current and CTAT current should be independent to the supply voltage. So, the circuit without the resistor is designed as shown in figure 2.5. This circuit is coupled each gate voltage. Therefore, it has independence about supply voltage as shown in equation (6). But if I_{ref} is not defined, the output current has indeterminate solution. Therefore, the reference current should be defied.

$$I_{out} = K \times I_{ref} \tag{6}$$
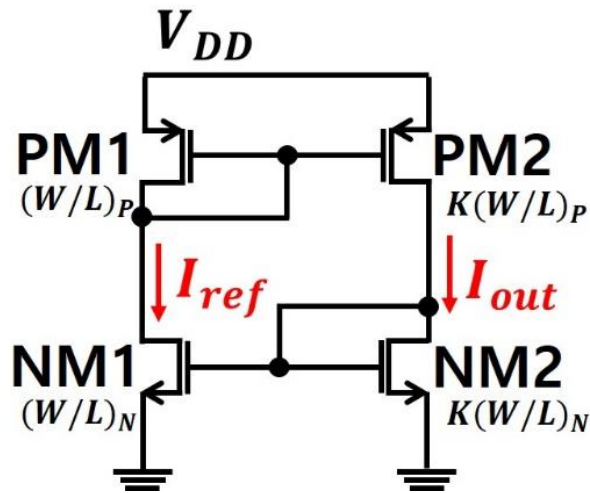
Figure 2.5 Bias circuit independent to supply voltage by self-biasing.

Figure 2.6 shows the bias circuit having defined reference current independent about the supply voltage as known as beta multiplier.

$$I_{out} = \frac{2}{\mu_N C_{ox}(W/L)_N} \times \frac{1}{R_1^2} (1 - \frac{1}{\sqrt{K}})^2 \tag{7}$$

Therefore, the current mirror circuit using the beta multiplier is supply independent current source as shown equation (7). The output current is defined

by R_1 and the ratio of transistor size K. In this case, $\mu_N C_{ox}(W/L)_N$ term is called

as beta in equation (7). So, this structure is known as beta multiplier.
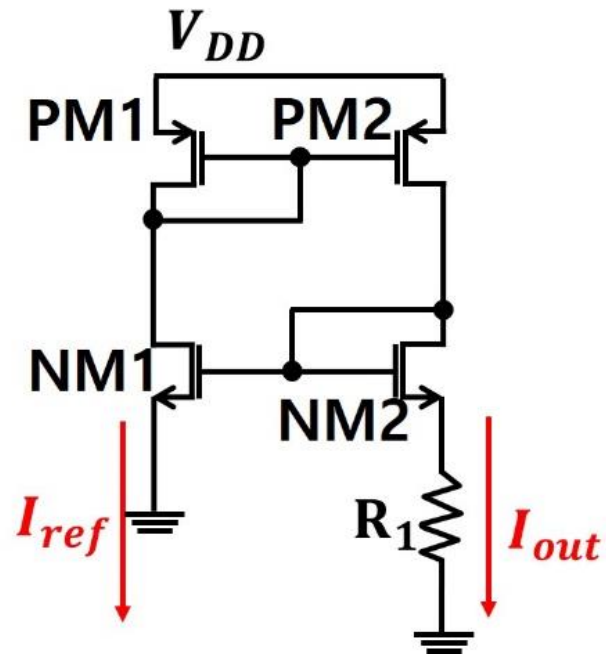
Figure 2.6 Beta multiplier circuit schematic. Resistor determines output current.

2.2.1.2 Complementary to Absolute Temperature

The CTAT voltage is generated at the semiconductor devices such as MOSFET, BJT and PN junction diode. The conventional BGR uses the BJT devices to generate the CTAT voltage. However, the BGR using the BJT is inefficiency about the area and power consumption. Recently, the BGR using CMOS diode is widely used instead of BJT. Conventionally, the MOSFET diode connection or the parasitic BJT in the CMOS is used instead of conventional BJT as shown in figure 2.7 [17]. In this thesis, the BGR is consist of the NMOS diode in figure 2.7.

(a)   (b)
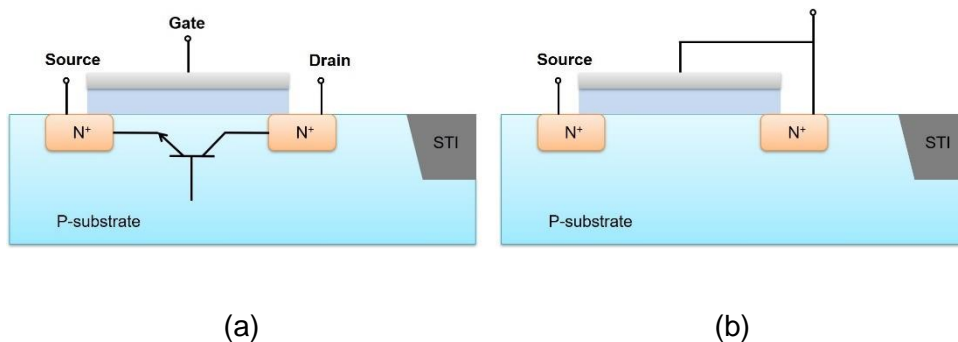
Figure 2.7 (a) Parasitic BJT in standard CMOS process and (b) NMOS diode connection.

At the BJT, the collector current is defined as shown equation (8) in the BJT.

Therefore, collector current is an inverse proportional to the absolute temperature.

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) = I_S \exp\left(\frac{qV_{BE}}{kT}\right) \tag{8}$$

$$V_T = \frac{kT}{q} \tag{9}$$

Moreover, the base-emitter voltage is calculated applying same method. The

V_{BE} is defined as shown as equation (10).

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{10}$$

$$I_S = b T^{4+m} \exp\left(\frac{-E_g}{kT}\right) \tag{11}$$

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m}\exp\left(\frac{-E_g}{kT}\right) + b T^{4+m}\exp\left(\frac{-E_g}{kT}\right)\frac{E_g}{kT^2} \tag{12}$$

$$\frac{V_T}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T \tag{13}$$

To calculate the voltage change rate for the temperature, equation (10) is

differentiated for the temperature.

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} \tag{14}$$

where I_S is saturation current, b is proportional constant, and E_g is silicon bandgap energy. Therefore, the equation (15) is calculated by using the equation (13) and (14).

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T}\ln\left(\frac{I_C}{I_S}\right) - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}V_T = \frac{V_{BE}-(4+m)V_T-E_g/q}{T} \tag{15}$$

$\frac{\partial V_{BE}}{\partial T}$ is defined the temperature coefficient of the base-emitter voltage depending on the V_{BE} and the temperature.

At the MOSFET case, they has the CTAT characteristic when that is operated in the weak inversion region [17 – 19]. The drain current is defined as equation (16) in subthreshold region. Therefore, gate-source voltage is defined as equation (17).

$$I_D = \frac{W}{L}I_0 exp\frac{(V_{GS}-V_{th})}{\eta V_T} \tag{16}$$

$$V_{GS} = \eta V_T \ln\left(\frac{I_D}{I_0}\frac{L}{W}\right) + V_{th} \qquad (17)$$

$$I_0 = \mu C_{ox}(\eta - 1)V_T^2 \qquad (18)$$

$$V_{th} = V_{th0} - kT = -\frac{E_g}{2q} + \varphi_b + \frac{\sqrt{4\varepsilon_{si}qN_a\varphi_b}}{C_{ox}} \qquad (19)$$

$$\frac{\partial V_{th}}{\partial T} = -(2\eta - 1)\frac{K_B}{q}\left\{ln\left(\frac{\sqrt{N_cN_v}}{N_a}\right) + \frac{3}{2}\right\} + \frac{\eta-1}{q}\frac{dE_g}{dT} \qquad (20)$$

$$V_{GS}(T) = V_{GS}(T_0) + K_G\left(\frac{T}{T_0} - 1\right) \qquad (21)$$

where η is subthreshold slope factor, φ_b is the difference between fermi level and intrinsic level, N_a is doping concentration of the channel, and ε_{si} is the silicon permittivity. Therefore, V_{GS} decreases with temperature.

2.2.1.3 Proportional to Absolute Temperature

Figure 2.8 shows the PTAT current generation principle. The BJT Q1 and Q2 has different current density by differing the BJT size. When the current density is difference, the ΔV_{BE} is defined equation (18).

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \tag{18}$$

$$= V_T ln\frac{nI_o}{I_s} - V_T ln\frac{I_o}{I_s} \tag{19}$$

$$= V_T \ln(n) \tag{20}$$

<div align="center">(a)   (b)</div>
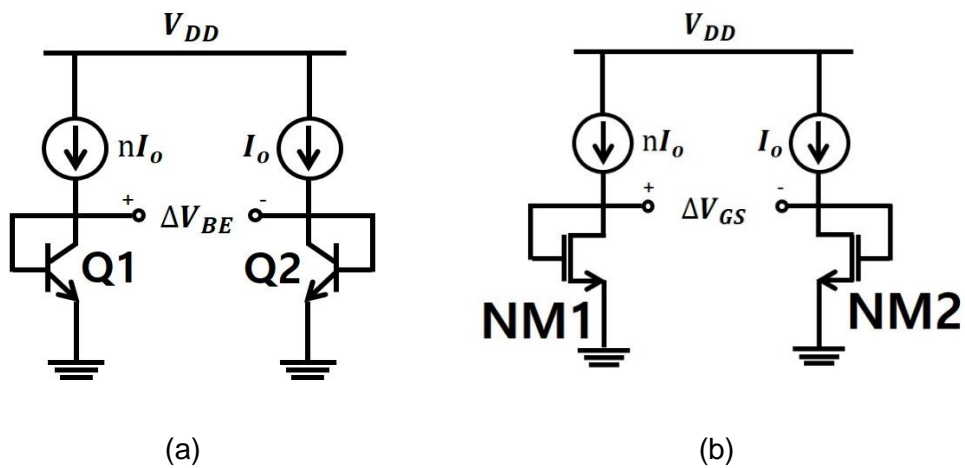
Figure 2.8 (a) PTAT current generation at the BJT case and (b) the MOSFET case.

At the MOSFET devices, identical principle is applied such as BJT case.

$$\Delta V_{GS} = V_{GS1} - V_{GS2} \tag{21}$$

$$= \eta V_T \ln\left(\frac{I_{D1}}{I_0}\frac{L_1}{W_1}\right) - \eta V_T \ln\left(\frac{I_{D2}}{I_0}\frac{L_2}{W_2}\right) \tag{22}$$

$$= \eta V_T \ln\left(\frac{I_{D1}}{I_{D2}}\frac{L_1}{W_1}\frac{W_2}{L_2}\right) \tag{23}$$

Therefore, the PTAT current is generated by scaling the MOSFET NM1 and NM2 size.

2.2.2 Operation Principle of Conventional BGR

Figure 2.9 shows the fully CMOS conventional BGR schematic. The conventional BGR consists of three part. First part is beta multiplier generating the constant current independent to supply voltage variation. The beta multiplier should be operated in the saturation region to maintain the reference voltage. The second part makes the PTAT current by scaling MOSFET size. Therefore, generated current is defined by equation (6), which N is ratio of two MOSFET (NM3 and NM4) size. This current flows into third part due to the current mirror PM3. In this part, the NM3 and NM4 is operated in the weak inversion region. Finally, the output of conventional BGR is defined by equation (7). In this equation, the former is PTAT voltage, while the latter is the CTAT voltage.

$$I_{PTAT} = \frac{1}{R_1} \times \ln{(N)} \tag{6}$$

$$V_{ref} = \frac{R_2}{R_1} \times \ln(N) + V_{NM5} \tag{7}$$
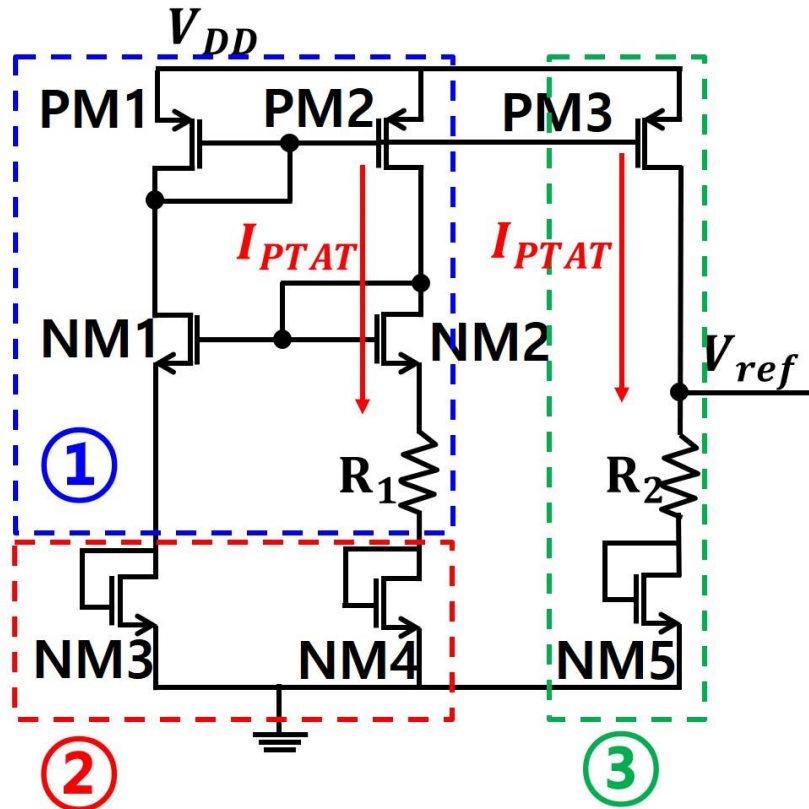
Figure 2.9 Conventional BGR structure consisting beta multiplier, NMOS diode connection stage to make PTAT property and output stage.

2.3 Radiation Effect on Semiconductor Devices

Two types of effects can occur in semiconductor devices exposed by radiation: single event effects (SEE) and cumulative effects. The SEE is a temporary effect that can flip over digital bits in data storage such as D Flip Flop (DFF) and static random-access memory (SRAM) in high-energy radiation fields like space. However, a cumulative effect such as total ionizing dose (TID), is considered for analog circuit system [20].
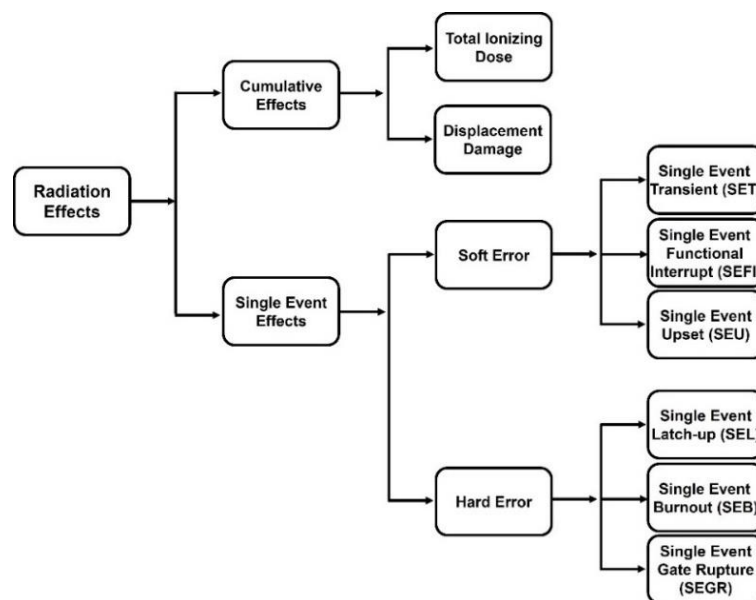
Figure 2.10 Categorization of Radiation effects on the semiconductor

2.3.1 Total Ionizing Dose Effect

The permanent damage is generated when the semiconductor is irradiated by radiation for a long time. This cumulative and long-term effect is known as total ionizing dose (TID). It is primarily generated at the insulate layer such as silicon oxide layer and shallow trench isolation region. When incident radiation penetrates the oxide region of the MOSFET, it generates electron-hole pairs (EHP). Some carriers are promptly recombined or escaped from the dielectric, but the other carriers, especially holes, can be trapped in the insulator region and SiO2-Si interface because the hole mobility is relatively slower than the electron [7-11]. This cumulative damage causes performance degradation to CMOS devices in terms of threshold voltage, leakage current, and noise. TID effect unit is defined by ionization energy, Grays (1 J/kg, *Gy*) or *rad (*1 ergs/g) [20]

$$1 \ Gy = 100 \ rad \tag{10}$$
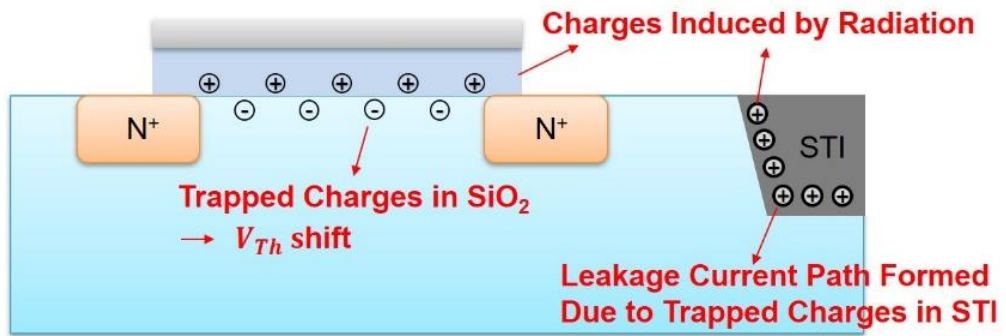
Figure 2.11 TID effect on the standard NMOS structure. Threshold voltage shift and leakage current path are made by trapped charge

2.3.1.1 Threshold Voltage Shift

The threshold voltage is defined as a voltage when the transistor starts to operate. The hole induced by radiation is trapped in the oxide layer or SiO_2-Si interface and changes the threshold voltage of MOSFET. The most trapped hole is in the SiO_2-Si interface when the positive voltage is applied at the NMOS. Although the source-drain potential difference is zero, channel is slightly formed by trapped hole in the SiO_2-Si interface. Therefore, the threshold voltage decreases at the N type MOSFET [21].

In case of PMOS, it has difference mechanism comparing to the NMOS. The interface trapped holes pull the electrons located in the substrate and push the channel charges which consist of hole. Therefore, the threshold voltage increases along the number of holes. Mathematically, the threshold voltage shift generated by the oxide trapped charges is defined as shown equation (11).

$$\Delta V_{ot} = -\frac{1}{\varepsilon_{ox}} \int_0^{x_{ox}} x \rho_{ox}(x) dx \qquad (11)$$

where ε_{ox} is the dielectric constant, x_{ox} is the oxide thickness, ρ_{ox} is the volume density of charge in the oxide, and x is the position in the oxide. The threshold voltage shift induced by trapped holes at the SiO₂-Si interface is shown equation (12).

$$\Delta V_{it} = -\frac{Q_{int}}{C_{ox}} \tag{12}$$

where Q_{int} is the charge of trapped hole in the SiO₂-Si interface. Therefore, the total threshold voltage shift is calculated as the sum of equations (11) and (12) as shown in equation (13).

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} = -\frac{1}{\varepsilon_{ox}} \int_0^{x_{ox}} x\rho_{ox}(x)dx - \frac{Q_{int}}{C_{ox}} \tag{13}$$
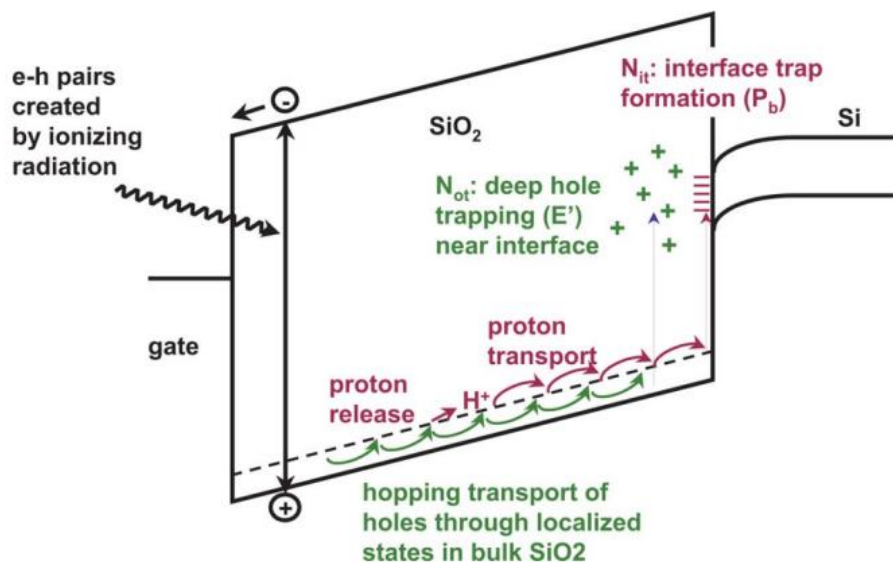
Figure 2.12 MOS energy band diagram and total ionization effect [22]. Trapped charges in SiO2 are moved to interface area when gate voltage applied and generate TID effect.

2.3.1.2 Leakage Current

In the modern CMOS process, shallow trench isolation (STI) technique is widely used to prevent to interact with neighboring MOSFET. However, in the extremely environment, holes induced by radiation are trapped in STI region. the trapped holes pull the electron at the non-channel area and form the parasitic channel in the NMOS as shown figure 2.13. The leakage current cause the degradation of the circuitry system such as BGR output variation. Particularly NMOS devices is more vulnerable than PMOS. Since, the MOSFET scaling down reduce the number of trapped hole and the parasitic channel consisting of hole is not formed due to the rebelling force against the trapped charge in STI [22-24].
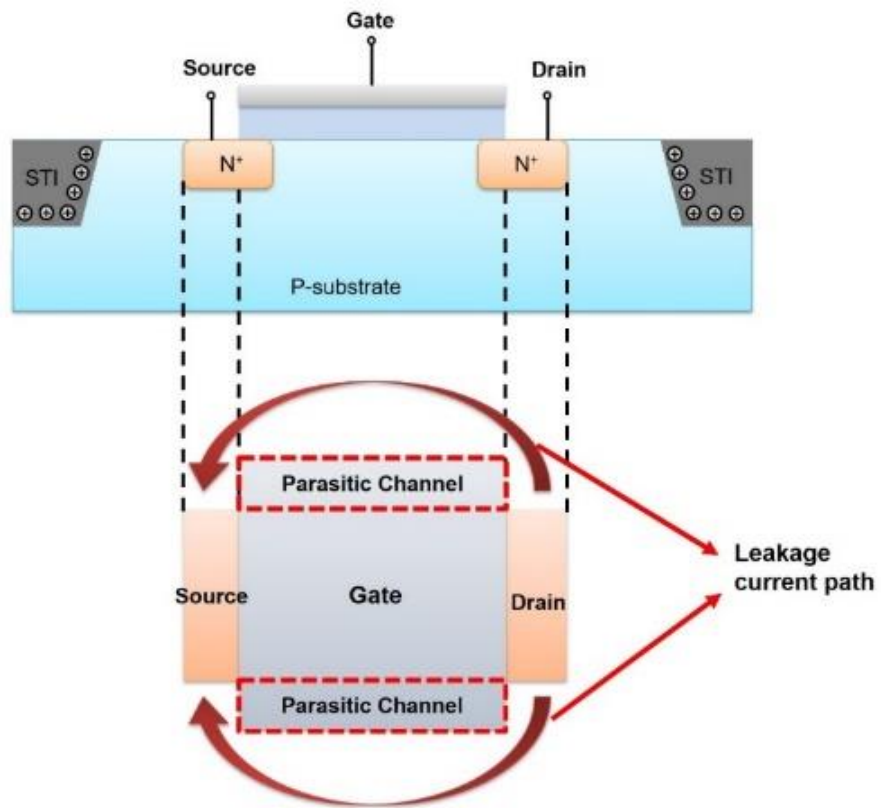
Figure 2.13 Leakage current path induced by radiation. Trapped charges at the STI region form parasitic channel flowing leakage current.

2.3.2 Single Event Effects

High energy radiations such as alpha ray, proton beam have a significant effect on the digital system including the DFF, SRAM, Analog Digital Converter (ADC) and Digital Analog Converter (DAC). The high energy particle generates EHP while losing the energy about 3.6 eV per one pair. The most EHP is promptly recombined but some pair is collected at the reverse biased PN junction in MOSFET. The collected EHP generates the errors such as bit flip, glitches and current spike. Figure 2.13 visualizes the SEE mechanism [20]. The SEE is divided into two types: a soft error and a hard error.

The soft error is temporary effect to reverse bit while it could maintain the circuit operating. Sigle Event Transient (SET), Single Event Functional Interrupt (SEFI) and Sing Event Upset (SEU) are included in the soft error. The SEU is the phenomenon that could change the digital logic from ground level (0) to high level (1) by transferring the energy of particles. The SET is mainly occurred in the analog-digital mixed system and disturbs data processing by propagating the

signal induced by single event. Except SEU and SET, all kind of general error is called as the SEFI [25].

The semiconductor devices could be broken down, since the large current which the high energy heavy ion generates flowed at the circuit. Therefore, the hard errors including Single Event Latch-up (SEL), Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) is classified as permanent effect [26].
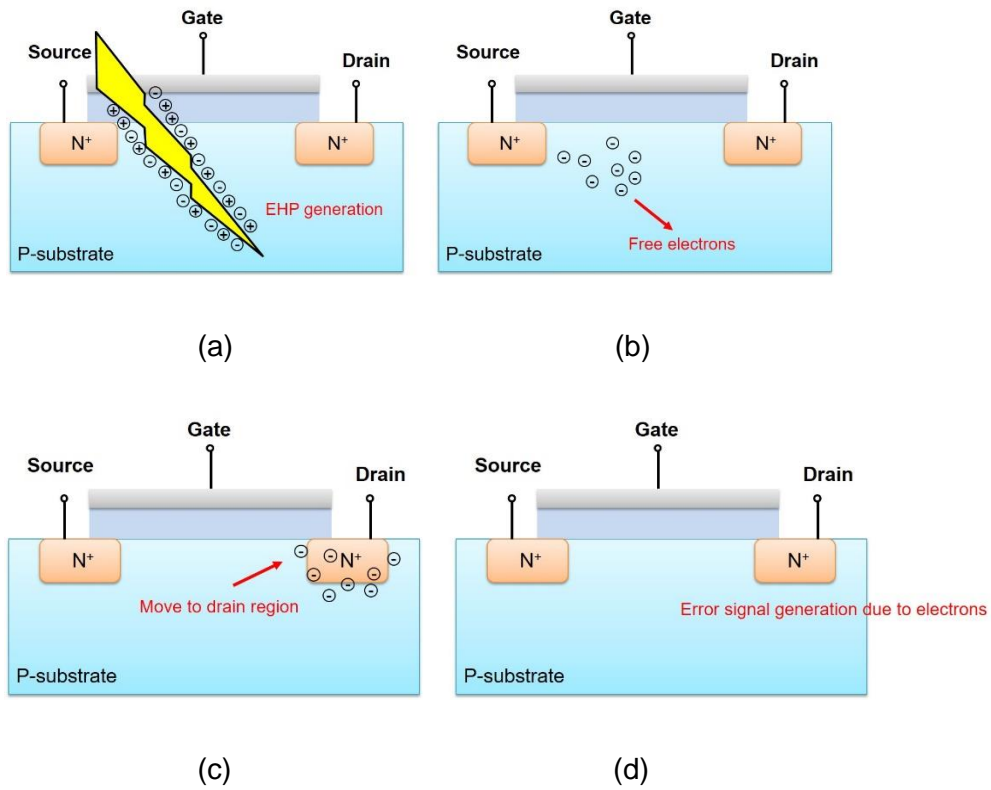
Figure 2.14 Single event effect induced by heavy ion mechanism. (a) Electron-hole pairs are generated by radiation. (b) Free electrons float the P-substrate and (c) move to drain region. (d) Collected electron at the drain generate a various error such as bit flip, glitches and current spike.

2.3.3 Radiation Effect on the BGR

The bandgap reference circuit is affected by radiation. The MOSFET process technology is developed to have radiation tolerance. The SOI technique highly increase the resistant of SEE. However, the TID effect could be still discussed due to parasitic channel induced by radiation at the field oxide. The TID effect changes the semiconductor characteristics such as threshold voltage and leakage current. Therefore, the circuit operating point is changed by accumulation effect. Moreover, the leakage current increase cause the PTAT current increase. So, the reference voltage increase too. However, radiation effect is difficult to exactly anticipate because it depends on the MOSFET process and radiation type. Figure 2.15 shows the radiation experiment results on the BGR circuits from previous researches [7, 10, 11]..
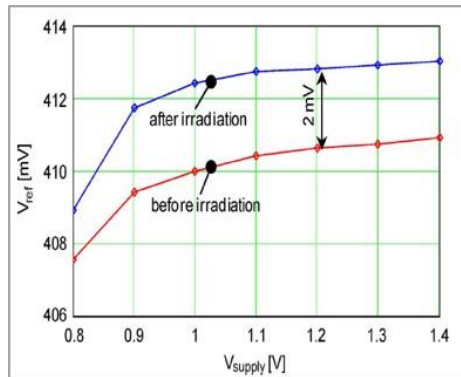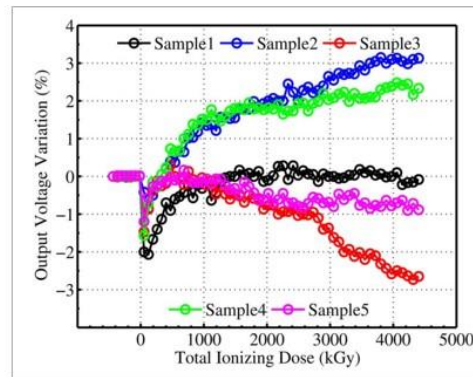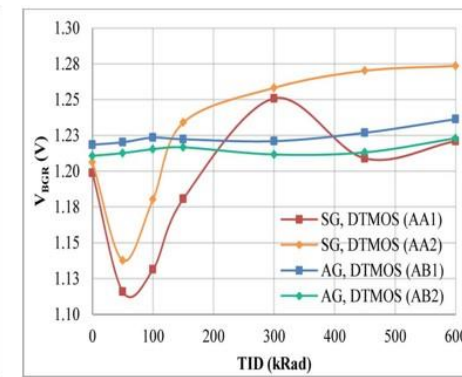
Figure 2.15 Radiation effect on the BGR circuit. (a) Radiation hardened BGR made by Gromov. It is irradiated by x-ray up to 40 Mrad [7]. (b) Ying Cao BGR is irradiated up to 450 Mrad [10]. (c) These BGR is designed by M. McCue and irradiated by gamma ray up to 600 krad [11].

3. Proposed

3.1 Principle of Proposed BGR

The proposed radiation hardened by design (RHBD) BGR is to exploit the difference between two output reference voltages, equation (14) and (15), from the identical temperature and radiation characteristics, as shown in figure 3.1 (top). The concept is realized by utilizing two similar BGR circuits in terms of CMOS size, structure, and resistor values. If a supply voltage applied to one BGR circuit is decreased, the PTAT current on the PM3 decreases either due to the channel-length modulation effect in the saturation region, resulting in a decreased output reference voltage. Thus, these circuits are supplied by different supply voltages for generating different output reference voltages.

$$V_{ref(1)} = \frac{R_2}{R_1} \times I_{ref(1)} + V_{NM5(1)} \qquad (14)$$

$$V_{ref(2)} = \frac{R_2}{R_1} \times I_{ref(2)} + V_{NM5(2)} \qquad (15)$$

Since the two BGRs with the same TC and TID effects, the variation induced by temperature and radiation can be minimized by subtracting the two internal reference voltages, as shown in figure 3.1 (bottom). The final reference voltage of the proposed circuit is calculated as the difference between the reference voltages of two identical BGR circuits such as equation (16).

$$V_{REF} = \frac{R_2}{R_1}\left(I_{ref(1)} - I_{ref(2)}\right) + \left(V_{NM5(1)} - V_{NM5(2)}\right) + \left(\Delta V_{rad(1)} - \Delta V_{rad(2)}\right) \quad (16)$$
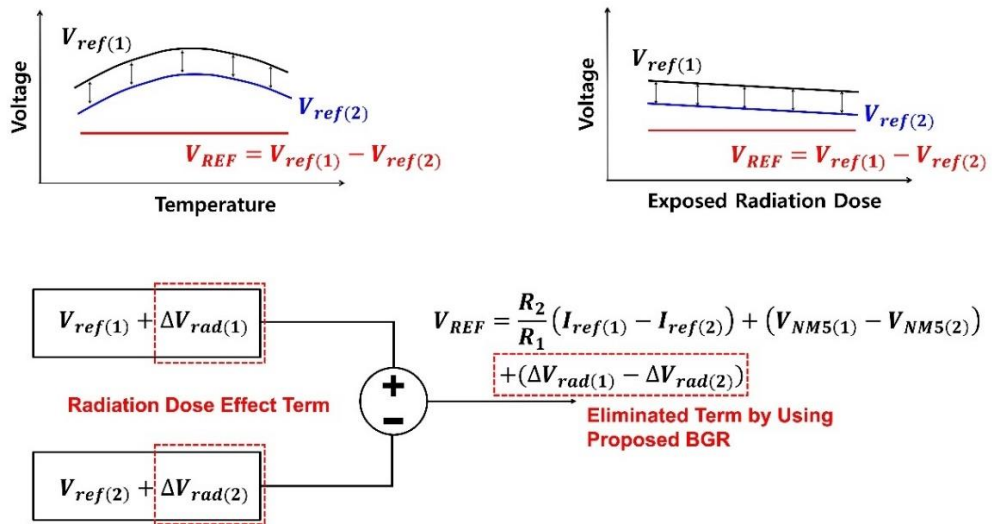
Fig. 3.1 Concept of proposed bandgap reference by subtracting temperature and radiation variations.

Figure 3.1 Concept of proposed bandgap reference by subtracting temperature and radiation variations. Figure 3.2 describes an entire architecture of the proposed BGR. Two conventional reference circuits applied by different supply voltages, 2.8 and 1.5 V, respectively, are designed involving startup circuits. The output of each BGR is connected to a source-follower buffer to match the impedance of the BGR circuit with the input impedance of the subtractor. As I said at chapter 2.3.1, PMOS is generally insensitive to the TID effect than NMOS. Since, the parasitic channel consisting of hole is not formed. Therefore, the source follower is designed by using PMOS. The two reference voltages, 736 and 693 mV, respectively, are subtracted by the subtractor, consisting of a two-stage OPAMP and a feedback resistor. Table 3-1 shows the OPAMP specifications. Consequently, the proposed circuit generates a stable final reference voltage of 275 mV, regardless of the temperature and radiation variations. Figure 3.3 shows the whole circuit was designed in a 0.18 μm standard CMOS process.

Table 3-1. OPAMP specifications

Supply voltage	3.3 V
DC gain	72.5 dB
Bandwidth (UBGW)	149 MHz
Bandwidth (3dB)	35 kHz
Phase margin	63.5°
Slew rate	160 V/μs
CMRR	62 dB

$$V_{REF} = \frac{R_5}{R_4}\{\frac{R_2}{R_1}\left(I_{ref(1)} - I_{ref(2)}\right) + \left(V_{NM5(1)} - V_{NM5(2)}\right)\}$$
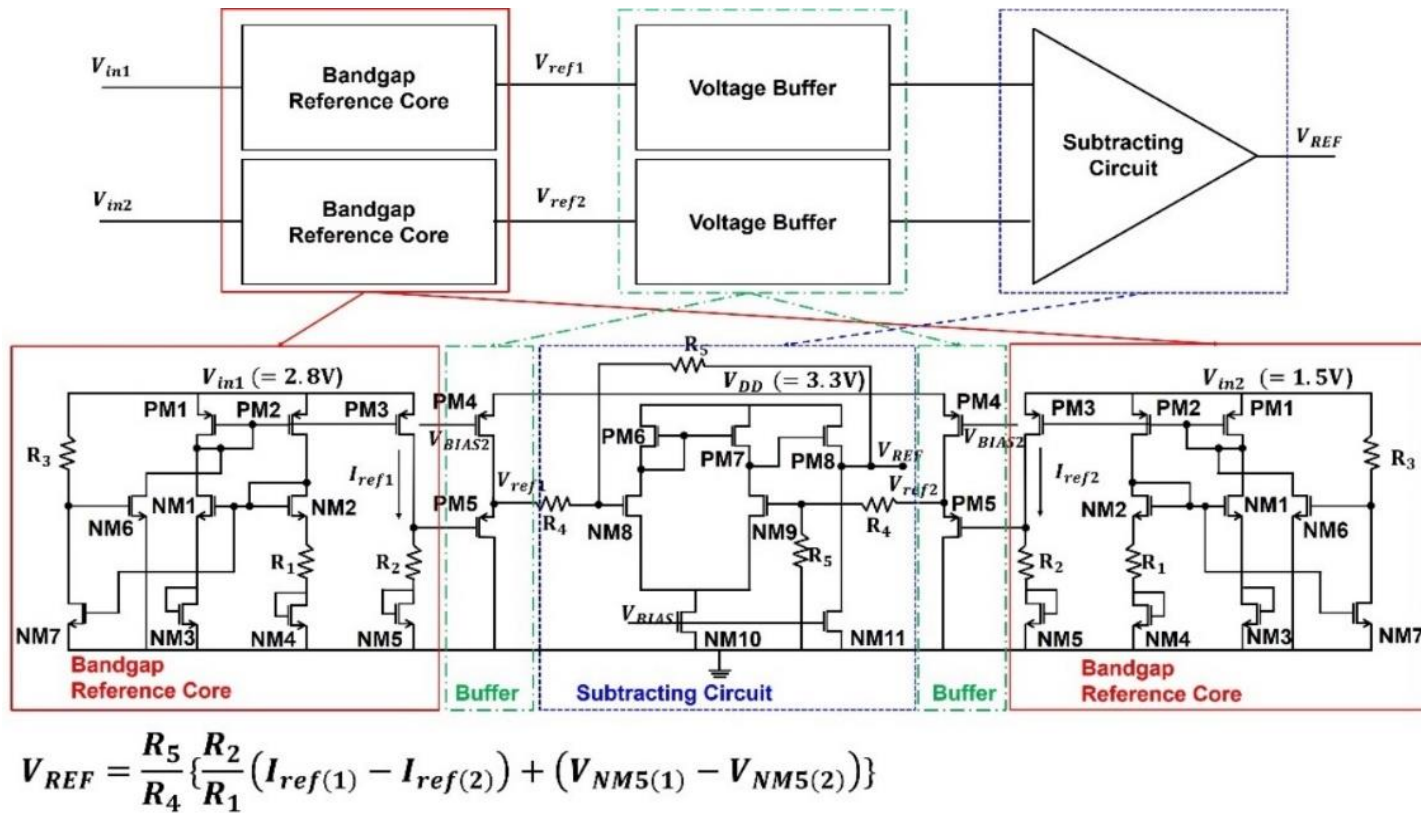
Figure 3.2 Architecture of proposed RHBD BGR block diagram and detailed schematic. It consists of the three parts: voltage subtractor, buffer, and bandgap reference core.

Chip Detail		
Parameter	Conventional	Proposed
CMOS Technology	Standard 180 nm	
Temperature Range (℃)	20 – 110	
Supply Voltage (V)	2.8	2.8 / 1.5
Power Consumption (μW)	414	1716
Reference Voltage (V)	0.736	0.275
Temperature Coefficient (PPM/℃)	289	2.9
△V *(due to radiation)*	13mV @2Mrad(SiO$_2$)	5.2mV @2Mrad(SiO$_2$)
Core Size (mm^2)	0.012	0.035
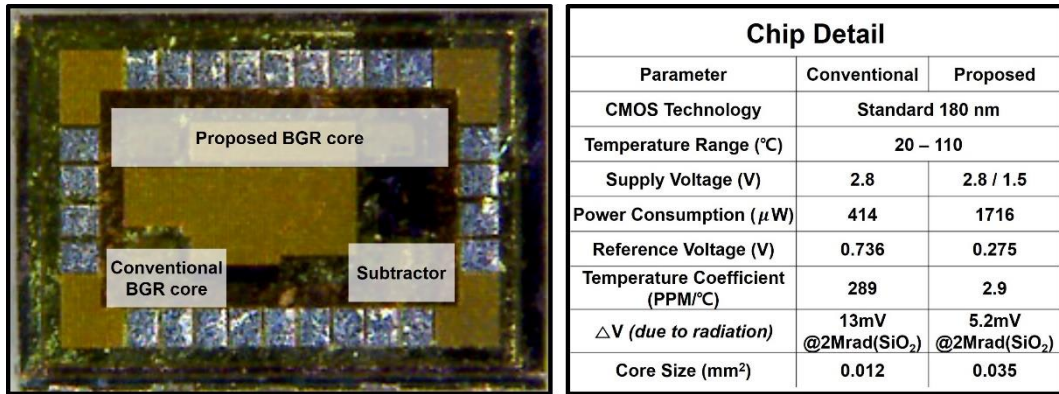
Figure 3.3 Architecture of proposed RHBD BGR block diagram and detailed schematic.

4. Experiment Results of Proposed BGR

4.1 Temperature Experiment

Figure 4.1 shows the temperature test environment. The experiment was conducted at the rate of 1℃/min from 20℃ to 110℃ in a temperature chamber. The output temperature on the display of chamber is measured by thermometer on the top side. Therefore, the plate temperature is not the same the output temperature. So, the design under test (DUT) was suspended in the air so as not to heat by hot plate of chamber during the test. Figure 4.2 presents the temperature experiment result

By the experiment result, the maximum voltage variation of the proposed design shows 0.26 mV, while conventional circuit produces 26 mV, and the TC is 2.9 and 289 ppm/℃, respectively. The temperature test result shows that the proposed structure is more stable about 97.45 % than that of the conventional design.

Figure 4.1 Temperature experiment setup.
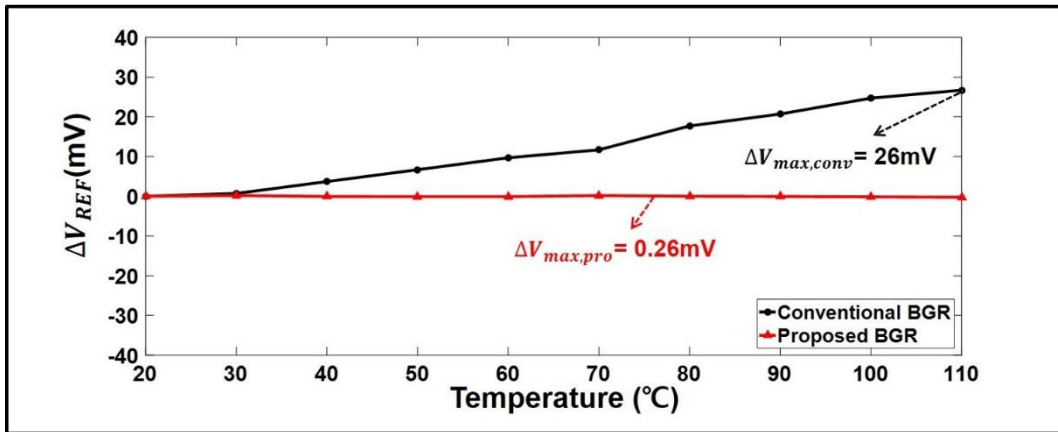
Figure 4.2 Output reference voltage changes of conventional and proposed BGRs versus temperature.

4.2 Irradiation Experiment

The irradiation test was carried out via a Cobalt-60 source with high-level activity of 490 kCi at the Korea atomic energy research institute, as shown in figure 4.3. The BGR chips were exposed by radiation up to 2 Mrad (SiO2) for 20h. The DUT board was faced toward the Cobalt-60 source; the other measurement instruments were located beyond a 30 cm thick wall to prevent radiation effects to the equipment.

Figure 4.4 shows the irradiation test result. The conventional BGR shows the maximum radiation error of 16.7 mV and average error of 13 mV, while the proposed design shows 9.5 and 5.2 mV, respectively. The final reference voltage shows the slight fluctuation with the irradiation dose increase even after the radiation effects are canceled by the proposed technique because the two conventional BGRs can be influenced by the TID effects differently due to the device mismatches of process, voltage, and temperature (PVT) variations. Nevertheless, the test result shows that the proposed circuit is less susceptible than the conventional BGR regarding radiation effects.

Figure 4.3 Irradiation experiment setup.
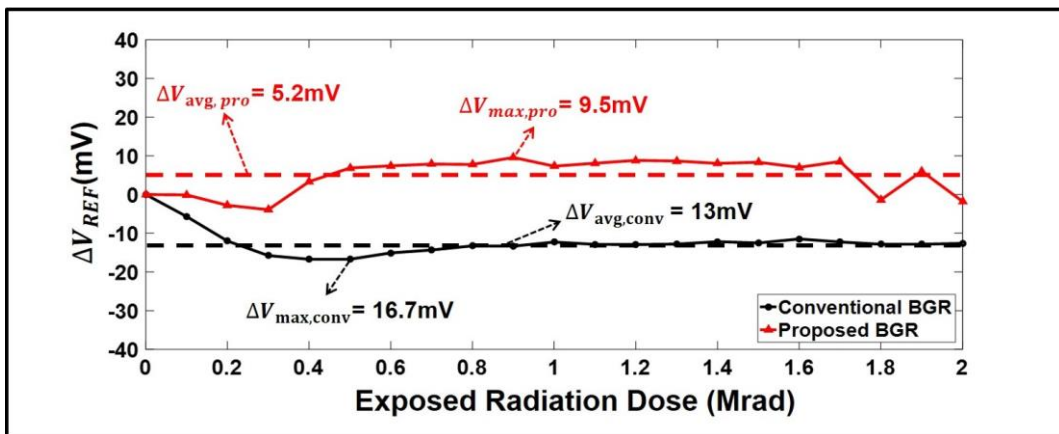
Figure 4.4 Output reference voltage changes of conventional and proposed BGRs versus irradiation dose.

4.3 Behavioral Verification Experiment as CJC circuit

Figure 4.5 shows an experiment result of the proposed BGR circuit coupling with a thermocouple for a temperature range of 30℃ to 420℃. The output voltage was recorded for 2 min at each temperature every 30℃.

As a test result, the thermocouple output indicates 274.3 mV at 30℃ and 291.4 mV at 420℃. The total voltage shift shows about 17.1 mV, and the thermal electromotive force is calculated about 43.8 μm/℃ for the temperature change of 390℃. It shows that the proposed BGR is verified as a CJC circuit with the proper linearity of the thermocouple.
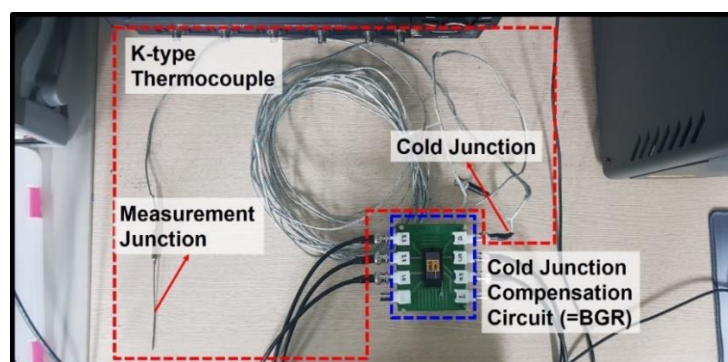
Figure 4.5 Thermocouple experiment environment.
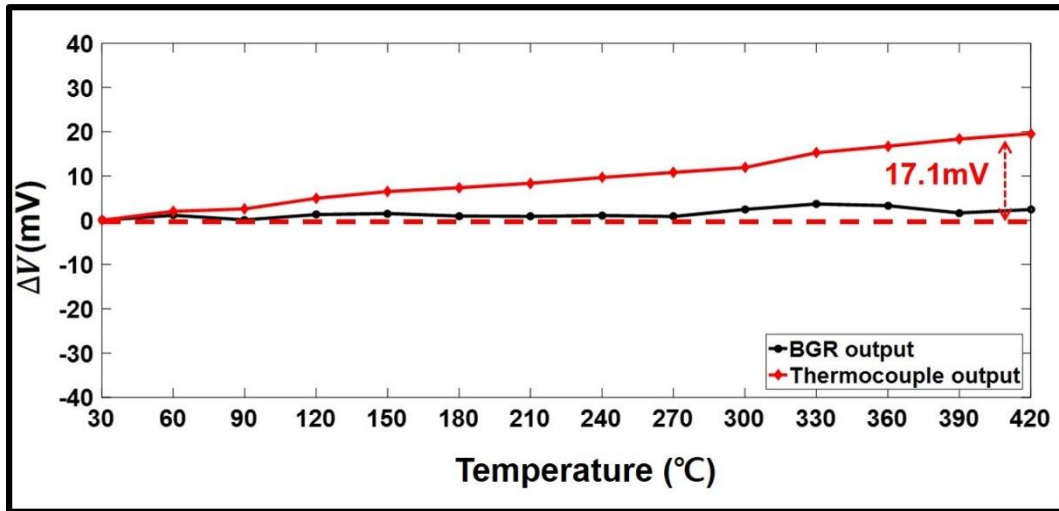
Figure 4.6 Output voltage changes of proposed BGR and thermocouple

4.4 Multi-chip measurement method

The multi-chip test should be conducted to analyze the BGR properties distribution about the temperature, the supply voltage and the radiation at least 15 chips. So, this part introduces the multi-chip measurement experiment method.

4.4.1 Multi-chip measurement device

Multi-chip measurement device is introduced in this paper. Conventional BGR and proposed BGR are involved in the one chip. So, when use fifteen chip total output is thirty that is too many to measure using the oscilloscope. Fig. 4.7 shows the multi-chip measurement device block diagram. The PCB outputs connect with measurement device that is controlled by Labview program. The device switches the output data step by step. So, the BGR outputs sequentially input to the oscilloscope. The oscilloscope measures the voltage level and transfer these data to the PC. Fig. 4.8 represented the multi-chip measurement device.

Figure 4.7 Multi-chip measurement device block diagram. PCB is provided the supply voltage from power supply. PCB outputs sequentially input to the Oscilloscope going through the multi-chip measurement device.
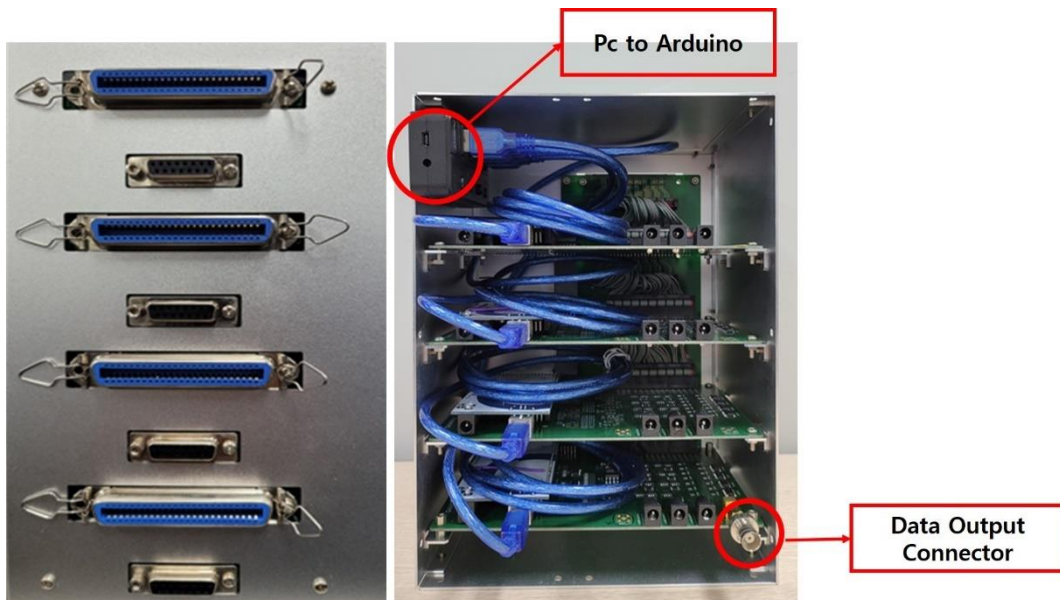
Figure 4.8 Multi-chip measurement device. Arduino boards is controlled by Labview program and then the input data output in serial order.

5. Conclusion
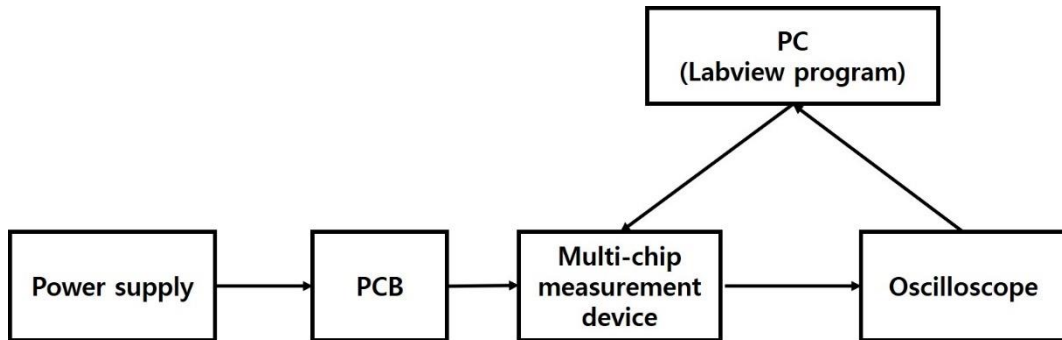
This thesis presents the RHBD BGR design technique by using two conventional BGR circuits. The BGR circuit is used in a various radiation environment such as nuclear power plant, military, medical, and space industry. Particularly, the thermocouple sensor interface with BGR is widely used in nuclear power plant to monitor if the reactor temperature is too high or low. However, the BGR output voltage is variated by radiation effect including TID effect. Therefore, the temperature could be accurately measured and it threatens the safety of nuclear power plant. Therefore, this thesis is conducted to maintain reference voltage in the radiation field and present the RHBD BGR topology and experiment result.

The previous researches demonstrated the ELT structure has radiation tolerance. However, these devices are difficult to design and simulation and require large area. Therefore, the proposed design is implemented by standard 0.18 μm process which is different to previous researches that are used ELT structure. The key idea of RHBD BGR is to remove the error induced by radiation by subtracting

reference voltages of two identical BGRs, resulting in supplying the constant output voltage. Prior to design, there are two problems. First, the radiation induced error should be identical. It was settled by utilizing two identical BGR. Second, the difference of two reference voltage is not zero. Therefore, they could have different output voltage level. This problem was resolved by differing the supply voltage. So, the two identical BGR has different output voltage due to channel length modulation effect.

The temperature and irradiation experiment was conducted to demonstrate to retain stable reference voltage level regardless of external environment. The result of the radiation experiment shows that the conventional BGR shows the maximum radiation error of 16.7 mV and average error of 13 mV, while the proposed design shows 9.5 and 5.2 mV, respectively. Therefore, the proposed reference voltage supply was assessed to be 97.45 % more stable for temperature and 60 % more stable for radiation.

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Abstract (in Korea)

기준전압 차이를 이용한 공통방사선 영향제거

내방사선 기준전압공급기

연세대학교 대학원

전기전자공학과

승 민 욱

본 논문은 기준전압 차이를 이용한 공통 방사선 영향을 제거하는 내방사선 기준전압공급기에 관한 것이다. 기준전압공급기는 다양한 센서 및 회로 시스템에서 일정한 전압을 공급해주는 필수적인 회로로 이를 이용한 thermocouple sensor interface는 원자력발전소 내 reactor 및 다른 장비를 모니터링하고 컨트롤 하기 위해서 사용

된다. 방사선환경에서 반도체집적회로 사용시 누적되는 손상이 발생하며, 이로 인해 문턱전압이 변하고 누설전류가 증가한다. 이를 총이온화선량 (TID)이라 하며, 반도체 소자의 특성 변화는 기준전압공급기 동작점을 변화시켜 결국 수 ~ 수 십 mV 출력전압 변동이 발생한다.

이전 연구들에서, 내방사선 기준전압공급기의 경우 Enclosed Layout Transistor (ELT)를 사용하여 방사선 영향을 최소화 하는 방법들을 제안하였다. 하지만 ELT 구조를 이용한 설계 및 시뮬레이션의 어려움과 대면적 요구 등 단점이 존재한다. 따라서 본 논문에서는 표준 0.18 ㎛ 공정을 이용하여 내방사선 기준전압공급기를 구현하였다.

제안하는 회로는 온도와 방사선에 대한 특성이 동일하고 출력전압이 다른 두 기준전압의 차이를 이용하였다. 완벽히 동일한 두 기준전압공급기는 방사선에 동일한 영향을 받는다. 따라서 방사선 특성을 동일화 할 수 있다. 두 기준전압공급기의 공급 전압을 다르게 하면, MOSFET 트랜지스터가 포화상태에서 동작할 때 channel length modulation effect가 유도되어 출력전압이 변하게 된다. 이를 이용하여 온도와 방사선에 대한 변화 특성이 같고 출력전압이 다른 두 회로를 만들 수 있다. 최종적으로 OPAMP로 구성된 voltage subtractor를 통해 두 기준전압 차이가 출력된다.

실험을 통해 온도와 방사선 변화에 따라 전통적인 기준전압공급기와 제안된 기준

전압공급기 출력 변화를 확인 하였다. 온도 실험은 20℃부터 110℃까지 진행 되었고, 실험 결과 일반적인 기준전압공급기는 26 mV의 변화가, 제안된 기준전압공급기는 0.26 mV 변화가 발생하였다. 방사선 실험은 Co-60 선원을 이용하여 시간당 100 krad 로 20시간 동안 조사하였다. 실험 결과 기존의 기준전압공급기는 최대 16.7 mV 평균 13 mV 변화가, 제안된 기준전압공급기에서는 최대 9.5 mV 평균 5.2 mV 변화가 발생하였다. 따라서 제안된 기준전압공급기가 온도에 대해서 97.45 % 그리고 방사선에 대해서 60 % 더 안정적인 것으로 평가되었다.