2025 68th International Midwest Symposium on Circuits and Systems

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August 10-13, 2025, Lansing, MI, USA

Track 1	Track 2	Track 3	Track 4
08:30-10:15 Banquet Room 1-6 Plenary Session MonKey00 *Opening Remarks & Keynote (Monday)*			
10:15-10:30 Event Session MonBr00 *Morning Break (Monday)*			
10:30-12:00 Room #201 Regular Session MonLecA01 *ADCs and DACs*	10:30-12:00 Room #204 Regular Session MonLecA02 *Neural Networks and Neuromorphic Systems I*	10:30-12:00 Room #101 Regular Session MonLecA03 *Digital Integrated Circuits and Systems I*	10:30-12:00 Room #103 Regular Session MonLecA04 *Wireline and Optical Communication Circuits and System*
12:00-13:30 Banquet Room 1-6 Event Session MonLun00 *Conference Lunch (Monday)*			
13:30-14:45 Room #201 Special Session MonLecB01 *Integrated Photonics Capabilities and Applications for Analog and Digital Circuits and Systems*	13:30-14:45 Room #204 Special Session MonLecB02 *Circuits and Systems for Intelligent Health Monitoring Using Machine Learning*	13:30-14:45 Room #101 Special Session MonLecB03 *Undergraduate Research in Circuits and Systems*	13:30-14:45 Room #103 Special Session MonLecB04 *Next-Generation AI Hardware Using Deep and Spiking Neural Networks for Efficient Edge Processing I*
14:45-16:00 Banquet Room 7-8 Poster Session MonPos00 *Circuits and Systems for AI and Edge Computing*			
16:00-18:30 Banquet Room 1-6 Event Session MonSIF00 *Student-Industry Forum (SIF)*			

MonLecA04 Room #103

Wireline and Optical Communication Circuits and System Regular Session

Chair: Musah, Tawfiq The Ohio State University

Co-Chair: Chatterjee, Baibhab University of Florida

10:30-10:45, Paper MonLecA04.1

PDF *A 40-Gb/s PAM-4 VCSEL Driver with Reconfigurable 3-Tap Fractionally Spaced FFE*

Kim, Dong-Hyeon	Univ. of Yonsei
Kim, Kihun	Univ. of Yonsei
Kim, Jun-Seo	Univ. of Yonsei
Park, Jae-Koo	Univ. of Yonsei
Rho, Dae-Won	Univ. of Yonsei
Lee, Jae-Ho	Univ. of Yonsei
Yang, Seung-Jae	Univ. of Yonsei
Choi, Woo-Young	Univ. of Yonsei

10:45-11:00, Paper MonLecA04.2

PDF *A Modular Cascaded Tap Equalizer for Chromatic Dispersion Equalization in Coherent Optical Receivers*

Cao, Yuang	The Ohio State University
Musah, Tawfiq	The Ohio State University

A 40-Gb/s PAM-4 VCSEL Driver With Reconfigurable 3-Tap Fractionally Spaced FFE

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***Abstract*—This work presents a 40-Gb/s four-level pulse amplitude modulation (PAM-4) driver implemented in 28-nm CMOS technology for a vertical-cavity surface-emitting laser (VCSEL). The reconfigurable 3-tap fractionally spaced feed-forward equalizer (FFE) compensates for the limited modulation bandwidth of a VCSEL. A thermometer encoder and a voltage-mode push-pull output driver with adjustable strength are employed to minimize the VCSEL optical response nonlinearity. The implemented driver achieves the energy efficiency of 3.7 pJ/bit and the bandwidth efficiency of 3.3 bit/Hz at 40-Gb/s PAM-4 signaling.**

Keywords— Vertical-cavity surface emitting laser (VCSEL), Transmitter (TX), Fractionally spaced feed-forward equalizer (FFE), Four-level pulse amplitude modulation (PAM-4), Optical transmitter.

I. INTRODUCTION

The demand for faster, cost-effective, and energy-efficient interconnect solutions is increasing for deep learning and cloud computing applications in data centers [1]. However, as data rates increase, signal quality deteriorates significantly in electrical interconnects due to channel losses. Therefore, optical links with negligible frequency-dependent loss are increasingly being deployed not only for long-distance communications but also for short-distance interconnects [2]. In particular, optical interconnects based on the vertical-cavity surface-emitting laser (VCSEL) have replaced many mid-range electrical interconnects (tens of meters) [3]. The high-bandwidth VCSEL is significantly more expensive than a standard electrical transmitter. Consequently, an approach that uses electrical equalization to compensate for the limited bandwidth of a lower-cost VCSEL can be of significant interest. When used as a data modulator, the VCSEL has two drawbacks. First, the VCSEL's light output power-current characteristic is nonlinear. This is because the larger modulation current causes a self-heating effect within the VCSEL, resulting in a reduction in differential gain [4]. This can generate unequal spacing between the amplitude level spacing in PAM-4 signaling and deteriorate the ratio of level mismatch (RLM). Second, the VCSEL electro-optical modulation response depends on the bias current. As the bias current increases, the modulation bandwidth increases, and the amount of the relaxation oscillation is reduced. As the current flowing into the VCSEL for the bottom sub-eye is smaller with the lower modulating bandwidth, more elaborate bandwidth compensation is required for the VCSEL. In addition, the optical pulse response of the VCSEL has a shorter rise time than the fall time due to the charge storage effect of the PN junction within the VCSEL [5], which can deteriorate the timing margin.

In our VCSEL driver, the RLM control is realized. In addition, the output driver's push-pull strengths are tuned to mitigate asymmetric transition times. The proposed reconfigurable 3-tap fractionally spaced feed-forward equalizer (FFE) effectively compensates for the insufficient bandwidth of a VCSEL with 14.7-GHz modulation bandwidth and achieves 40-Gb/s PAM-4 modulation.

II. VCSEL DRIVER

A. Architecture

Fig. 1 shows the schematic of the proposed VCSEL driver. By employing a quadrature clock to serialize data, the VCSEL driver operates at half the clock speed compared to the half-rate method, reducing clock path power consumption. For testing purposes, a 2^{31}-1 pseudorandom binary sequence (PRBS-31) pattern is generated on the chip using the internal pattern generator and distributed to 16 parallel data streams. The binary-to-thermometer encoders convert the data streams, enabling independent control of the amplitude levels in PAM-4 signaling. A retimer is employed to increase the timing margin of the 8:4 multiplexer (MUX). A data selector is used to implement the reconfigurable fractionally spaced FFE. The data selector chooses one of the pre-cursor, main, or post-cursor data to feed into the 8:4 MUX for serialization. Finally, a 4:1 MUX serializes the fastest data stream, which is then transferred to the output driver. A voltage-mode (VM) output driver supplies the modulation current and the bias current to the VCSEL. A quadrature clock generator produces four-phase I/Q/IB/QB clock signals. The quadrature error correction (QEC) and duty-cycle correction (DCC) calibrate clock phase errors and clock duty cycle errors, respectively.

B. Reconfigurable 3-Tap Fractionally Spaced FFE

Fig. 2 presents a simplified block diagram of the reconfigurable 3-tap fractionally spaced FFE. The input signal x(t) is preceded and delayed by intervals of $\alpha_1 T$ and $\alpha_2 T$, where α_1 and α_2 are the fractional coefficients, and T is the unit interval of the input data. The coefficients β_1, β_2, and β_3 are the tap weights. The data selector distributes data to each tap according to the assignment shown in Table I. This reconfigurable tap configuration provides flexibility to adjust which cursor is

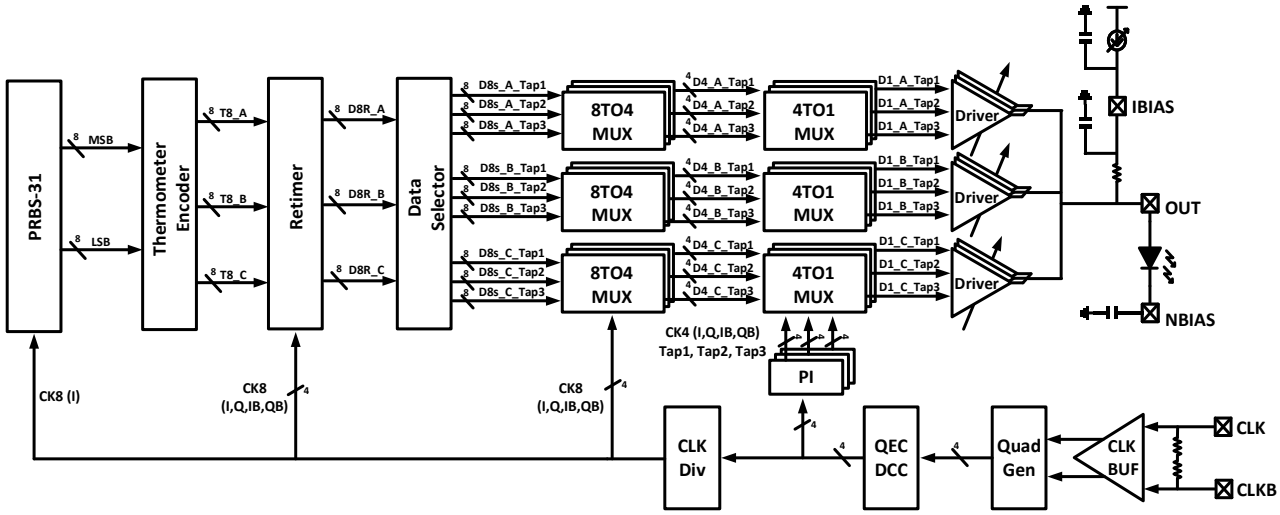


Fig. 1. Schematic of a proposed VCSEL driver.

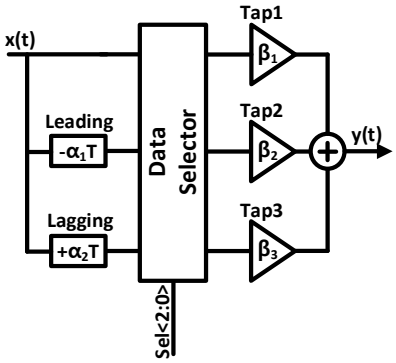


Fig. 2. Block diagram of the reconfigurable 3-tap fractionally spaced FFE.

TABLE I
RECONFIGUABLE 3-TAP FFE SETTING

Sel <2:0>	Tap1	Tap2	Tap3	Cursor (Tap1, Tap2, Tap3)
000	x(t)	x(t)	x(t)	main, main, main
001	x(t)	x(t+α_1T)	0	main, pre, off
010	x(t)	x(t-α_2T)	0	main, post, off
011	x(t)	x(t)	x(t+α_1T)	main, main, pre
100	x(t)	x(t)	x(t-α_2T)	main, main, post
101	x(t)	x(t+α_1T)	x(t-α_2T)	main, pre, post

active, allowing the equalizer to address bias-dependent modulation response issues. If the main, pre, and post FFE cursors are all selected, the transfer function of the fractionally spaced FFE is given by

$$H(j\omega) = \frac{Y(j\omega)}{X(j\omega)} = \beta_1 + \beta_2 e^{+j\alpha_1 T\omega} + \beta_3 e^{-j\alpha_2 T\omega}. \quad (1)$$

The corresponding amplitude of the transfer function can be determined as

$$|H(j\omega)| = \sqrt{\begin{matrix}\beta_1^2 + \beta_2^2 + \beta_3^2 + 2\beta_2\beta_3 cos\{(\alpha_1+\alpha_2)T\omega\} \\ +2\beta_1\beta_2\, cos(\alpha_1 T\omega) + 2\beta_1\beta_3\, cos(\alpha_2 T\omega)\end{matrix}}. \quad (2)$$

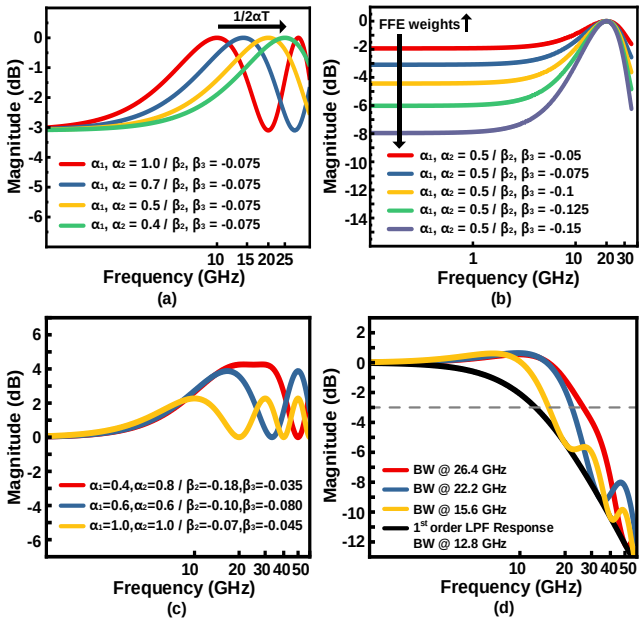


Fig. 3. The frequency responses of (a) fractionally spaced FFE with various fractional coefficients, (b) fractionally spaced FFE with various FFE tap weights, (c) fractionally spaced FFE with various fractional coefficients, and (d) fractionally spaced FFE passing through a 1st order low-pass filter.

The frequency responses of the fractionally spaced FFE for several selected combinations of fractional coefficients and FFE tap weights are shown in Fig. 3. For these simulations, the sum of the absolute values of the FFE tap weights is set to one, and the unit interval, T is set to 50 ps. As can be seen in Fig. 3(a), when α_1T equals α_2T and both β_2 and β_3 are negative, the magnitude response reaches a local maximum at 1/2αT. As the fractional coefficients decrease, the peaking frequency increases. For example, when the pre- and post-fractional coefficients are 0.5, the peak occurs at twice the Nyquist frequency, and the peaking frequency is twice as high as that for fractional coefficients of 1. As a result, the fractionally spaced FFE can compensate for the bandwidth limitation beyond the Nyquist frequency. However, to compensate for the greater insertion loss at higher frequencies when using lower fractional coefficients, larger FFE weights are required. This

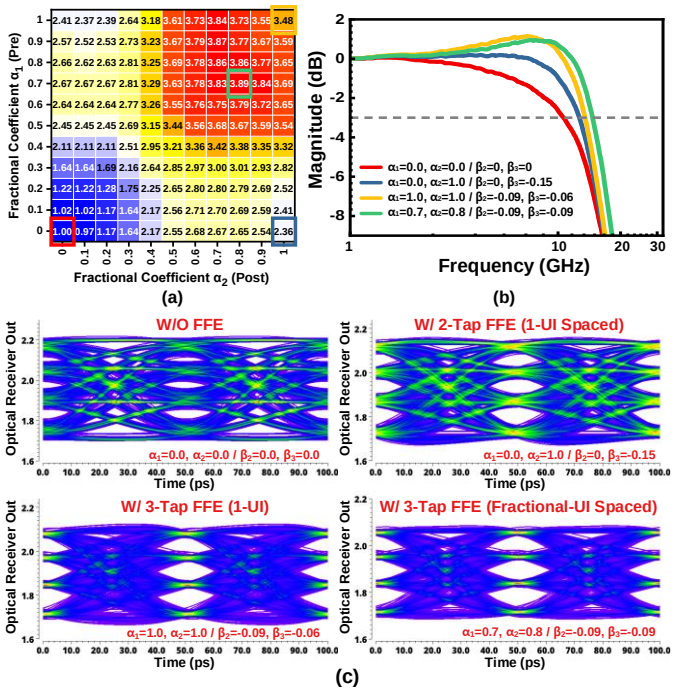


Fig. 4. Co-simulation results of (a) normalized PAM-4 eye-opening at 40-Gb/s with 7mA bias current, (b) the frequency response of optical link corresponding to the color-coded boxes of (a), (c) the 40-Gb/s eye-diagrams of optical receiver corresponding to the color-coded boxes of (a).

requirement reduces the magnitude at DC, which should be carefully considered, as can be seen in Fig. 3(b). Fig. 3(c) and (d) illustrate the frequency response of FFE for various fractional coefficients. The 3-tap fractionally spaced FFE can effectively compensate for a wide range of the bandwidth limitation. For example, when α_1 and α_2 are set to 0.4 and 0.8, respectively, the compensated frequency range is wider than when α_1 and α_2 are set to 0.6 and 0.6 as can be seen in Fig. 3(c). Fig. 3(d) shows the frequency response of the first-order low-pass filter and the compensated response derived from Fig. 3(c). The bandwidth extends to 15.6-GHz when both α_1 and α_2 are set to 1, as in conventional FFE. Furthermore, the bandwidth extends to 22.2-GHz when both α_1 and α_2 are set to 0.6, and further increases to 26.4-GHz when α_1 and α_2 are set to 0.4 and 0.8, respectively.

The 3-tap fractionally spaced FFE effect is evaluated together with the VCSEL and the optical receiver in co-simulation. The VCSEL used for our investigation is a commercial product, and its electro-optical 3-dB modulation bandwidth is 14.7-GHz at the bias current of 7 mA. The equivalent circuit for the VCSEL is achieved using piecewise linear RLC elements based on the measured optical characteristics [6]. The RLC parameter values depend on the bias current, allowing both small-signal and large-signal response simulation. The frequency response of a commercial optical receiver is reflected for co-simulation. Fig. 4 shows the simulation results for various combinations of FFE parameters. In Fig. 4(a), the normalized eye-opening areas are shown for varying α_1 and α_2 values for PAM-4 40-Gb/s modulation. For these results, the optimal β_2 and β_3 are used, which provide the best results from co-simulation. As shown in the figure, the

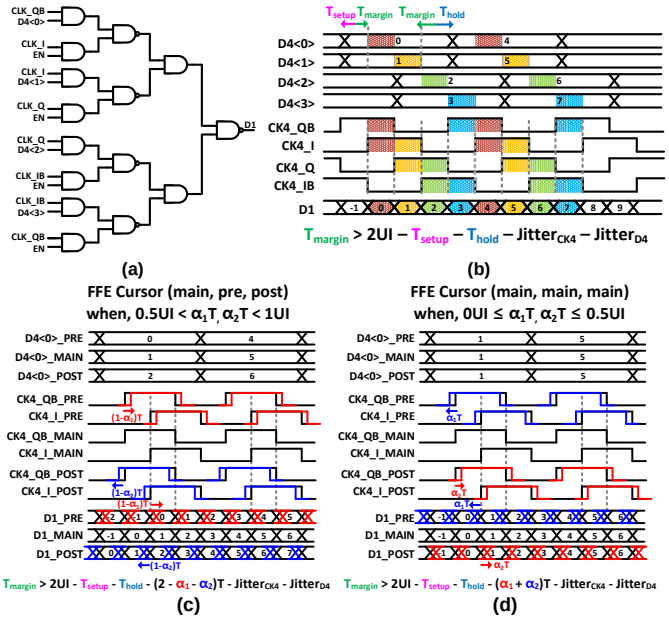


Fig. 5. (a) Schematic of 4:1 multiplexer. (b) Timing diagram of 4:1 multiplexer. (c) Timing diagram of the 0.5 UI to 1 UI fractionally spaced FFE configuration. (d) Timing diagram of the 0 UI to 0.5 UI fractionally spaced FFE configuration.

optimal values for α1 = 0.7 and α2 = 0.8 are achieved with a bias current of 7 mA. The eye-opening area is improved by a factor of 3.89 compared to the case without fractionally spaced FFE. Fig. 4(b) shows the frequency response of the co-simulated optical link and the frequency response compensated using FFE, corresponding to the four different cases, color-coded boxes in Fig. 4(a). The bandwidth is extended from 12.1-GHz to 13.5, 14.2, and 15.4-GHz in the following FFE order: 2-tap 1 UI space, 3-tap 1 UI space, and 3-tap fractional UI space. As previously explained, lower fractional coefficients result in peaking at higher frequencies, thus enabling a wider bandwidth. Consequently, a bandwidth of up to 15.4-GHz is achieved when α_1 and α_2 are 0.7 and 0.8, respectively. The wider bandwidth can be obtained with smaller fractional coefficients. However, excessively small fractional coefficients lead to poorer eye-opening, as shown in Fig. 4(a). To flatten the magnitude at high frequencies, larger FFE weights are required, resulting in a decrease in magnitude at DC, as illustrated in Fig. 3(b). Consequently, the output signal swing is reduced, resulting in a decreased eye opening. Since there is a trade-off between extended bandwidth and signal swing, it is necessary to carefully select optimal fractional coefficients and FFE weights. The optimal eye diagram of the optical receiver with the maximum eye opening was obtained when α_1 and α_2 were set to 0.7 and 0.8, respectively, and β_2 and β_3 were set to -0.09, as shown in Fig. 4(c).

C. 4:1MUX with Phase Interpolator

Fig. 5(a) illustrates the schematic of a 4:1 MUX. Unlike the current-mode (CM) logic 4:1 multiplexer, the NAND gate-based 4:1 multiplexer exhibits lower power consumption owing to the absence of static power dissipation. The 4:1 MUX uses the quadrature clock from PI and serializes four UI data as shown in Fig. 5(b). The PI controls the clock phase from 0° to 360°. The clock phase can be observed externally using the

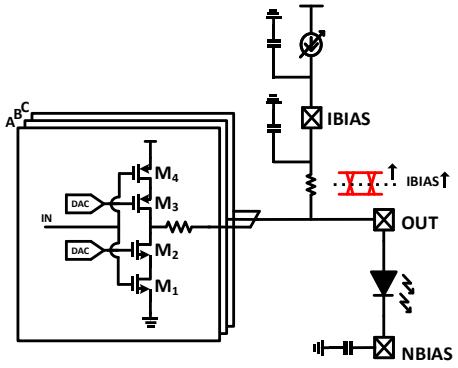


Fig. 6. Schematic of proposed VCSEL output driver.

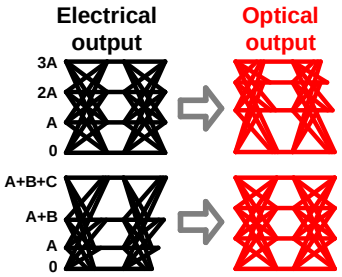


Fig. 7. Illustration of electrical output of VCSEL driver and optical output of VCSEL.

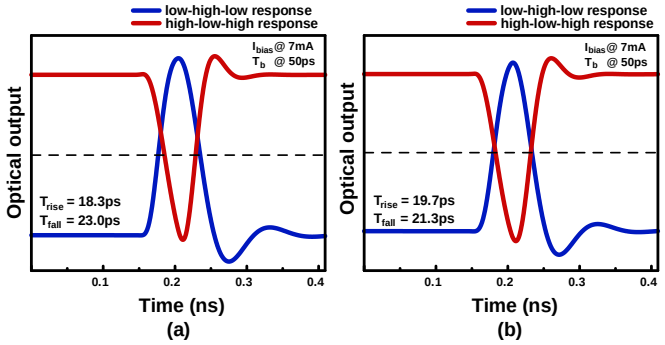


Fig.8. Simulated VCSEL optical pulse response. (a) without rise and fall time control. (b) with rise and fall time control.

position of the PI codes. The pre- and post-cursors required for the 3-tap fractionally spaced FFE are generated by adjusting the PI's clock phase and using the data selector. If α_1T and α_2T are between 0.5 UI and 1 UI, the pre-, main, and post-cursors are selected. Then, the clock phases used in the 4:1 MUXs to serialize the pre- and post-cursors are adjusted by (1 - α_1)T and (1 - α_2)T, respectively, as shown in Fig. 5(c). If α_1T and α_2T are between 0 UI and 0.5 UI, all cursors are assigned to the main data. Then, the clock phases used the 4:1 MUXs, which serialize the pre- and post-cursor, are adjusted by α_1T and α_2T, respectively, as shown in Fig. 5(d). By utilizing the reconfigurable FFE, an additional timing margin of 0.5 UI is ensured, allowing the fractional coefficient range to be extended from 0 to 1.

D. Output Driver

A current-mode output driver wastes half of the power consumption due to the dummy load, resulting in area overhead. However, a voltage-mode output driver exhibits low power

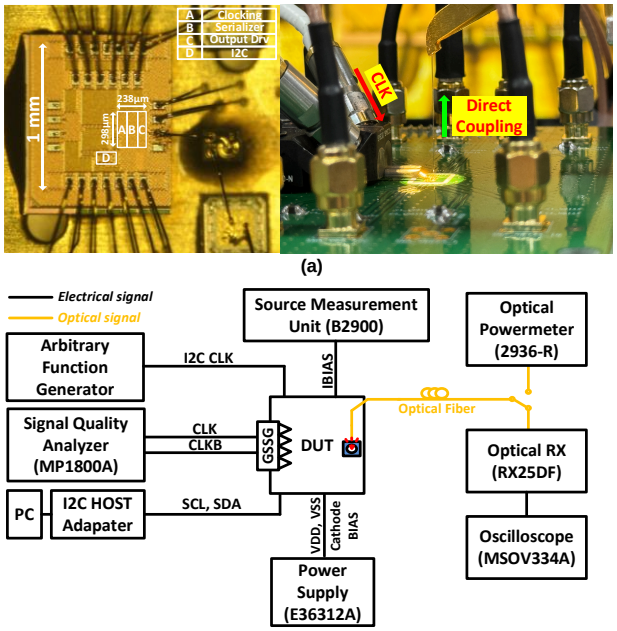


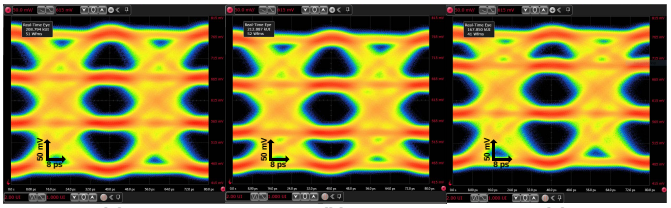
Fig. 9. (a) Die micrograph. (b) Measurement setup.

consumption due to its low supply voltage and the absence of static power dissipation, without incurring any area overhead [8]. Fig. 6 describes a voltage-mode output driver utilized in our design. The strengths of transistors M_2 and M_3 are controlled by the DAC. It enables adjusting the RLM of VCSEL's optical output, asymmetric transition time, and FFE tap weights by tuning the push-pull strength. The optical output is enhanced by intentionally distorting the A, B, and C strengths of the output drivers to compensate for the nonlinearity in the L-I characteristics of the VCSEL, as illustrated in Fig. 7. The asymmetric rise and fall times are mitigated by adjusting the push-pull strength, as shown in Fig. 8.

III. MEASUREMENT

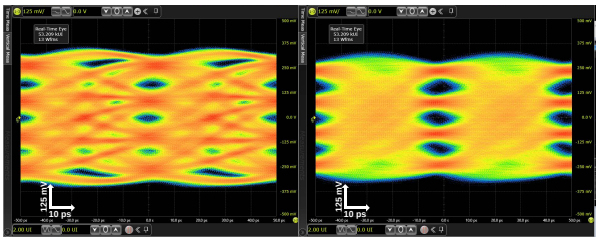
The proposed VCSEL driver is fabricated in 28-nm CMOS. The die micrograph and measurement setup are shown in Fig. 9. The VCSEL driver core area is 0.071 mm^2. For testing, a commercial VCSEL is bonded to a common cathode. Decoupling capacitors reduce the noise in the power supply at the VCSEL cathode and bias current nodes. The 850-nm multi-mode VCSEL bandwidth is 14.7-GHz at 7mA bias current. To convert the VCSEL's optical signal to the electrical signal, we use a commercial 850-nm optical receiver, which has a bandwidth of 21.5-GHz. The VCSEL is connected to the optical receiver using a cleaved multi-mode fiber and lightwave probe. To capture the optical eye diagrams, the optical receiver output is connected to a Keysight real-time oscilloscope.

Fig. 10 shows the measured electrical eye diagrams of a PRBS-31 pattern at 50-Gb/s PAM-4 with various amplitude level control settings. Fig. 10(a) displays the eye diagram when the sub-eye spacings are equal. Fig. 10(b) and (c) present eye diagrams where the bottom and top eye heights are reduced, respectively. The measured electrical signal swing voltage is 360 mV into a 50 Ω termination load. Fig. 11 shows the



(a) (b) (c)

Fig. 10. PAM-4 50-Gb/s electrical eye diagrams of (a) equally spaced eye, (b) narrowly spaced bottom eye, and (c) narrowly spaced top eye.



(a) (b)

Fig. 11. PAM-4 40-Gb/s optical eye diagrams. (a) without EQ and RLM control. (b) with EQ and RLM control.

measured optical eye diagrams of a PRBS-31 pattern at 40-Gb/s PAM-4. In this measurement, no equalization is applied at the receiver side. Fig. 11(a) shows the optical eye diagram without FFE and RLM control. Fig. 11(b) presents the optical eye diagram with FFE and RLM control. The selected cursors are the main, pre, and post cursors, with assigned tap weight DAC codes of 203/192/128, respectively. The fractional coefficients of the pre- and post-cursors are 0.75.

The total energy efficiency is 3.7 pJ/bit at 40-Gb/s. Excluding the clocking and serializer power, the energy efficiency of the pre-driver and output driver is 0.75 pJ/bit at 40-Gb/s. The optical link bandwidth can be calculated using the following equation [7], [8].

$$BW_{total}^{-2} = BW_{VCSEL}^{-2} + BW_{Opticalreceiver}^{-2}. \quad (3)$$

BW_{VCSEL} and $BW_{Opticalreceiver}$ are the bandwidths of the VCSEL and an optical receiver, respectively. Accordingly, the total bandwidth is 12.1-GHz in the measurement setup. The bandwidth efficiency is defined as the data rate divided by the total bandwidth and is recorded as 3.3 bit/Hz.

IV. Conclusion

A 40-Gb/s PAM-4 VCSEL driver in 28-nm CMOS technology is presented. The key techniques to mitigate the VCSEL's nonlinearity and limited bandwidth are discussed, including the reconfigurable 3-tap fractionally spaced FFE, RLM control using a thermometer encoder, and a push-pull output driver with adjustable strength. The achieved total energy and bandwidth efficiencies are 3.7 pJ/bit and 3.3 bit/Hz, respectively. Table Ⅱ summarizes the performance of the proposed work in comparison with state-of-the-art VCSEL drivers. This work presents the most bandwidth-efficient VCSEL driver for testing among those listed in Table II.

TABLE II

Performance Summary

	JSSC '21 [3]	JSSC '18 [8]	CICC '17 [9]	JSSC '24 [10]	This Work
Technology	28nm CMOS	14nm CMOS	28nm CMOS	12nm CMOS	28nm CMOS
Data Rate [Gb/s]	56	45	40	50	40
Signaling	NRZ	NRZ	NRZ	PAM-4	PAM-4
Data Sequence	PRBS-10	PRBS-7	PRBS-7	PRBS-9	PRBS-31
Equalization Technique	3-tap FFE, Shunt peaking	Fractional space 2-tap FFE	Complex zero	3-tap FFE	Fractional space 3-tap FFE
VCSEL BW [GHz]	28	18	19	23	14.7
O/E converter BW [GHz]	30	22	35	34	21.5
Core Area [mm^2]	0.024	0.088	0.033	0.086	0.071*
Energy Efficiency [pJ/bit]	1.28*	2.11	0.5	0.97	0.75 / 3.7*
Bandwidth Efficiency [bit/Hz]	2.7	3.2	2.4	2.6	3.3

*Including Serializer & Clocking Circuits

Acknowledgment

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