Design and Optimization of 3D-Stacked Backside-Illuminated SPADs

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Abstract

Edge breakdown in 3D-stacked backside-illuminated SPADs is prevented using a virtual guard ring implemented with an additional deep P-well implantation at the junction. The SPAD fabricated in 40 nm CIS technology demonstrates a uniform avalanche region, resolving the default structural limitations.

I. Introduction

Single-photon avalanche diodes (SPADs) are essential devices for emerging applications such as direct time-of-flight (dToF), LiDAR, 3D imaging, low-light imaging, fluorescence lifetime imaging microscopy (FLIM), etc. [1]–[10]. To maximize photon detection efficiency (PDE), adopting a non-isolated type SPAD structure is highly advantageous. However, this structure basically requires independent substrate biasing, necessitating physical isolation from the readout circuitry. To resolve this, recent designs have adopted 3D-stacking and backside illumination (BSI) technologies [2]–[9].

The 3D-stacked structure physically separates the SPAD from the logic circuits, allowing the entire P-epitaxial layer to be utilized safely. Additionally, the BSI structure improves PDE by removing optical blockages caused by metal routing layers. Although these architectural changes improve optical and integration performance, they do not resolve the fundamental physical limitations of the device junction, specifically the localized electric field crowding induced by the physical curvature at the junction edge. Therefore, precise control of the electric-field distribution in the device is necessary to prevent premature edge breakdown of the SPAD. In this paper, a virtual guard ring (VGR) structure using a selective deep P-well (DPW) layer is proposed to address this issue for 3D-stacked BSI SPADs.

II. Device Structures

A. Default SPAD Structure

A default non-isolated type SPAD structure consists of an N-well and P-epitaxial (NW/P-epi) junction without any guard-ring technique (Fig. 1a). Utilizing the P-epi, which has the lowest doping concentration, allows the depletion region to expand maximally. This widens the effective active area and significantly contributes to efficiency enhancement. However, at the periphery of the N-well, including the boundaries interfacing with the surrounding P-well (PW) or P-epi, the physical curvature naturally causes the concentration of the electric field. Due to this electric field crowding, premature edge breakdown occurs at approximately 44 V, as demonstrated by the measured current-voltage (I-V) characteristics (Fig. 2). This occurs before the central region reaches the critical electric field required for avalanche multiplication. When edge breakdown precedes planar breakdown, the applied excess bias V_{EX} cannot effectively extend the depletion region into the deep P-epi layer, thereby severely limiting the maximum achievable PDE. The light emission test (LET) result visually confirms this localized breakdown at the edge (Fig. 3a). This localized breakdown reduces the effective active area and inhibits uniform avalanche multiplication.

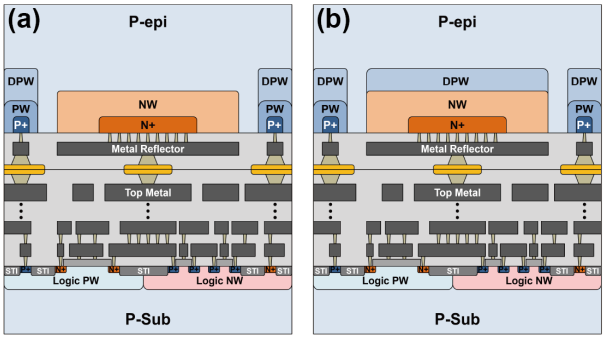

Fig. 1. Cross-sections of (a) the default SPAD structure and (b) the proposed VGR structure.

B. Proposed Virtual Guard Ring Structure

While maintaining the structural benefits of the non-isolated type SPAD structure, a VGR structure is proposed (Fig. 1b). A DPW layer is selectively implanted in the central region of the N-well to form an NW/DPW junction. This DPW layer locally increases the doping concentration compared to the lightly doped P-epi layer. According to avalanche breakdown physics, this higher doping concentration narrows the depletion width, causing the junction to reach the critical electric field at a significantly lower reverse bias voltage. The DPW layer is intentionally excluded at the edge of the N-well, maintaining a 0.5 μm gap. By omitting this highly doped layer at the edge, the local electric field is kept lower than that in the central region. This VGR mechanism ensures that the maximum electric field is distributed uniformly across the entire active area, allowing planar breakdown to occur prior to edge breakdown. Furthermore, in 3D-

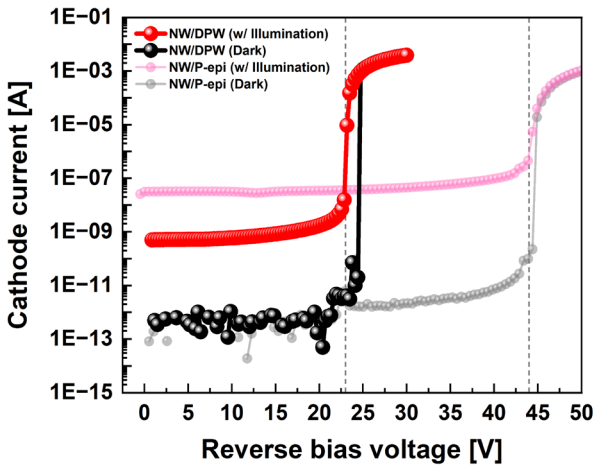

Fig. 2. Measured I-V characteristics of the default structure (NW/P-epi) and the proposed VGR structure (NW/DPW).

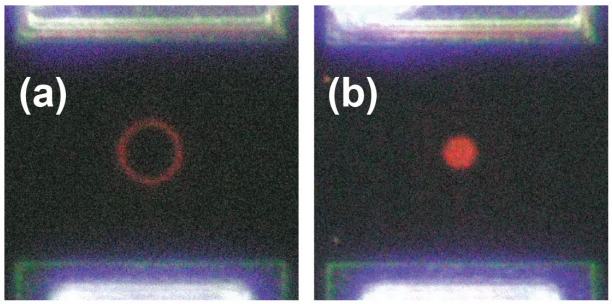

Fig. 3. LET results of (a) the default structure and (b) the proposed VGR structure at V_{EX} = 3 V.

stacked BSI technologies, miniaturizing the SPAD pitch is crucial for achieving high spatial resolution. Since a wide guard ring inevitably increases the SPAD pitch and degrades the fill factor (the ratio of the active area to the total SPAD size), the VGR width was aggressively scaled down to 0.5 µm to maximize the fill factor while maintaining reliable edge breakdown suppression.

III. Experimental Results

The proposed 3D-stacked BSI SPAD devices were fabricated in 40 nm CIS technology with a 10 µm active area diameter and 13um pitch. The measured I-V characteristics (Fig. 2) show that the structural modification effectively enhances the electric-field concentration at the planar junction, shifting the operating breakdown voltage to 23 V. The premature edge breakdown, which occurred at 44 V in the default NW/P-epi structure, is completely suppressed. Instead, a highly uniform light emission profile was observed across the entire active area, as confirmed by the LET result at V_{EX} = 3 V (Fig. 3b). This functional improvement was successfully verified with the fabricated 13 µm pitch SPAD.

IV. Conclusions

The selective implantation of a DPW layer functions as an effective virtual guard ring in 3D-stacked BSI SPADs. By enhancing the electric field at the main junction while maintaining a 0.5 µm gap at the edge, the breakdown voltage is reduced to 23 V. This structural modification successfully prevents the premature edge breakdown observed at 44 V in the default NW/P-epi structure. The resulting uniform avalanche multiplication demonstrates that the proposed structure fabricated in 40 nm CIS technology is suitable for reliable single-photon detection in next-generation imaging systems.

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