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(54) **Clock and data recovery device**

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EP 2 913 926 B1

Description

BACKGROUND

[0001] Embodiments of the inventive concepts described herein relate to a clock and data recovery device.

[0002] A clock and data recovery circuit is a device that restores a clock fit to a data rate from noisy data and samples data to restore it to refined data. The clock and data recovery circuit is an indispensable circuit in most data receivers. FIG. 1 is a block diagram schematically illustrating a conventional clock and data recovery device. In general, a clock and data recovery device consists of a phase detector 11, a charge pump unit 12, a loop filter unit 13, and a voltage controlled oscillator 14. Clock and data recovery architecture comprising a phase detector, charge pump circuit and voltage controlled oscillator is disclosed in US2013108001A1 and US2002126867A1. Among phase detectors, a linear phase detector determines whether either of data clock and an output clock of the voltage controlled oscillator precedes and how fast either of the data clock and the output clock is, whereas it has a disadvantage in that it is difficult to operate at high speed. Among the phase detectors, a bang-bang phase detector can operate at high speed, but it only determines whether either of data clock and an output clock of the voltage controlled oscillator precedes. That is, the bang-bang phase detector cannot determine how fast either of the data clock and the output clock is. A multi-level characteristic can be implemented using the bang-bang phase detector. However, as a number of level increases, a circuit area and power consumption increase.

[0003] On the other hand, production cost of a semiconductor circuit gradually decreases, but a cost needed to test the semiconductor circuit does not decrease. For example, a special comparator that operates at high speed and has high resolution is required to measure jitter of the semiconductor circuit. This causes an increase in a hardware cost and acts as a limitation in designing hardware. Also, a conventional jitter measurement device additionally necessitates a reference clock. For this reason, the conventional jitter measurement device is unsuitable in working together with a clock and data recovery device.

SUMMARY

[0004] Embodiments of the inventive concepts provide a clock and data recovery device and a phase detector having small-size and low-power consumption characteristics and capable of detecting a phase in a multi-level.

[0005] Embodiments of the inventive concepts provide a clock and data recovery device capable of measuring its jitter characteristic simply and efficiently.

[0006] According to an aspect of the present invention, there is provided a clock and data recovery device (100) comprising: a phase detector (110) configured to output a comparison signal; a charge pump unit (120) configured to adjust an amount of charges to be supplied according to the comparison signal; a loop filter unit (130) configured to accumulate the amount of charges to be supplied to output an adjustment signal; a voltage controlled oscillator (140) configured to generate an output clock signal variable according to the adjustment signal; and a modulation clock generation unit (150) configured to modulate the phase of the output clock signal to generate pairs of corresponding modulated clock signals among first modulated clock signals (Lclk) having a phase preceding a predetermined reference phase (Cclk) and second modulated clock signals (Rclk) having a phase lagging said reference phase (Cclk), and to provide the pairs of modulated clock signals sequentially to the phase detector(110), wherein the phase detector (110) is configured to receive the data clock signal and the pairs of modulated clock signals, and to compare phases of the data clock signal and each of the sequentially received pairs of modulated clock signals, to output the comparison signal.

[0007] The modulation clock generation unit may include a frequency divider configured to divide a frequency of the output clock signal to generate a frequency division clock signal; a bit generator configured to generate a bit signal in response to a clock edge of the frequency division clock signal; and a modulation clock output unit configured to sequentially output the pairs of modulated clock signals according to the bit signal.

[0008] The modulation clock generation unit may generate the sequential modulated clock signals with a linearly varying phase difference from the output clock signal.

[0009] The modulation clock generation unit may provide the phase detector with each pair of modulated clock signals during a predetermined time period, and the predetermined time period about each pair of modulated clock signals may be set according to the repetition rate of the pair of modulated clock signals the number of modulated clock signals, or both.

[0010] The phase detector may include a first phase comparison unit configured to sequentially compare a phase of the data clock signal and a phase of each modulated clock signal to output a first comparison signal.

[0011] The phase detector further may include a second phase comparison unit configured to compare a phase of the data clock signal and a phase of the output clock signal to output a second comparison signal. The charge pump unit may include a first charge pump configured to adjust the amount of charges to be supplied according to the first comparison signal; and a second charge pump configured to adjust the amount of charges to be supplied according to the second comparison signal.

[0012] The second phase comparison unit may include a first flip-flop configured to output the data clock signal in response to a first clock edge of the output clock signal; a second flip-flop configured to output an output value of

the first flip-flop in response to the first clock edge; a third flip-flop configured to output the data clock signal in response to a second clock edge of the output clock signal; a fourth flip-flop configured to output an output value of the third flip-flop in response to the first clock edge; a first XOR gate configured to compare the output value of the first flip-flop and an output value of the fourth flip-flop; and a second XOR gate configured to compare an output value of the second flip-flop and the output value of the fourth flip-flop.

[0013] The first phase comparison unit may include a fifth flip-flop configured to output the data clock signal in response to a first modulated clock signal sequentially input; a sixth flip-flop configured to output an output value of the fifth flip-flop in response to the first clock edge; a seventh flip-flop configured to output the data clock signal in response to a second modulated clock signal sequentially input; an eighth flip-flop configured to output an output value of the seventh flip-flop in response to the first clock edge; a third XOR gate configured to compare the output value of the first or fourth flip-flop and an output value of the sixth flip-flop; and a fourth XOR gate configured to compare the output value of the second or fourth flip-flop and an output value of the eighth flip-flop.

[0014] The first modulated clock signal may be a signal having a phase leading the output clock signal, and the second modulated clock signal may be a signal having a phase lagging the output clock signal.

[0015] The first comparison signal may include an output value of the first XOR gate and an output value of the second XOR gate, and the second comparison signal may include an output value of the third XOR gate and an output value of the fourth XOR gate.

[0016] The clock and data recovery device may further include a jitter measurement unit configured to compare cumulative values of the comparison signal to measure a jitter, each cumulative value corresponding to each of the modulated clock signals.

[0017] The jitter measurement unit may include a plurality of counters configured to measure cumulative values of the comparison signals, the cumulative value being measured for each of the modulated clock signals.

[0018] The jitter measurement unit may further include a selection circuit connected between the phase detector and the plurality of counters, the selection circuit being configured to select one of the plurality of counters in response to a modulated clock signal and connect the selected at least one counter to the phase detector.

[0019] The jitter measurement unit may further include a histogram analysis unit configured to analyze cumulative values measured by the plurality of counters in a histogram method to measure a jitter.

[0020] The phase detector may include a first phase comparison unit configured to sequentially receive modulated clock signals, modulated from a first clock signal to have different phases, and to compare phases of a data clock signal and each of the modulated clock signal sequentially input to output a first comparison signal.

[0021] The first phase comparison unit may sequentially receive the modulated clock signals modulated to have a linear phase difference from the first clock signal.

[0022] The first phase comparison unit may receive each of the modulated clock signals during the same time period and may output the first comparison signal.

[0023] The phase-locked loop circuit may further include a second phase comparison unit configured to compare phases of the data clock signal and the first clock signal to output a second comparison signal.

[0024] According to an exemplary embodiment of the inventive concept, there are provided a clock and data recovery device and a phase detector having a small-size and low-power consumption characteristics and capable of detecting a phase in a multi-level.

[0025] Also, according to an exemplary embodiment of the inventive concept, it is possible to measure a jitter characteristic of a clock and data recovery device simply and efficiently.

BRIEF DESCRIPTION OF THE FIGURES

[0026] The above and other objects and features will become apparent from the following description with reference to the following figures, wherein like reference numerals refer to like parts throughout the various figures unless otherwise specified.

FIG. 1 is a block diagram schematically illustrating a conventional clock and data recovery device;

FIG. 2 is a block diagram schematically illustrating a clock and data recovery device according to an exemplary embodiment of the inventive concept;

FIG. 3 is a diagram schematically illustrating modulated clock signals generated by a modulation clock generation unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept;

FIG. 4A is a detailed block diagram illustrating a clock and data recovery device according to an exemplary embodiment of the inventive concept;

FIG. 4B is a diagram illustrating modulated clock signals input to a first phase comparison unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept;

FIG. 5A is a timing diagram for describing a function of a modulation clock generation unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept.

FIG. 5B is an expanded diagram of a portion "A" of FIG. 5A;

FIG. 5C is an expanded diagram of a portion "B" of FIG. 5A;

FIG. 6 is a diagram for describing a function of a second phase comparison unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept;

FIG. 7 is a diagram for describing a function of a first

phase comparison unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept;

FIGS. 8A to 8D are diagrams for describing a function of a phase detector according to an exemplary embodiment of the inventive concept;

FIG. 9 is a detailed block diagram illustrating a phase detector of a clock and data recovery device according to an exemplary embodiment of the inventive concept;

FIGS. 10 and 11 are diagrams for describing an operation of a clock and data recovery device according to an exemplary embodiment of the inventive concept;

FIG. 12A is a block diagram schematically illustrating a clock and data recovery device according to another exemplary embodiment of the inventive concept;

FIG. 12B is a detailed block diagram illustrating a clock and data recovery device of FIG. 12A; and

FIGS. 13A to 13C and 14 are diagrams for describing a jitter measurement method of a clock and data recovery device of FIG. 12B.

DETAILED DESCRIPTION

[0027] Embodiments will be described in detail with reference to the accompanying drawings. The inventive concept, however, may be embodied in various different forms, and should not be construed as being limited only to the illustrated embodiments. Rather, these embodiments are provided as examples so that this disclosure will be thorough and complete, and will fully convey the concept of the inventive concept to those skilled in the art. Accordingly, known processes, elements, and techniques are not described with respect to some of the embodiments of the inventive concept. Unless otherwise noted, like reference numerals denote like elements throughout the attached drawings and written description, and thus descriptions will not be repeated. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity.

[0028] It will be understood that, although the terms "first", "second", "third", etc., may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the inventive concept.

[0029] Spatially relative terms, such as "beneath", "below", "lower", "under", "above", "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" or "under" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary terms "below" and "under" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0030] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the inventive concept. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. Also, the term "exemplary" is intended to refer to an example or illustration.

[0031] It will be understood that when an element or layer is referred to as being "on", "connected to", "coupled to", or "adjacent to" another element or layer, it can be directly on, connected, coupled, or adjacent to the other element or layer, or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to", "directly coupled to", or "immediately adjacent to" another element or layer, there are no intervening elements or layers present.

[0032] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this inventive concept belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and/or the present specification and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0033] A clock and data restoration device according to an exemplary embodiment of the inventive concept contains a phase detector which detects a phase of a data clock signal to output a comparison signal; a charge pump unit which adjusts the amount of charges to be supplied according to the comparison signal; a loop filter unit which accumulates the amount of charges to be supplied to output an adjustment signal; a voltage controlled

oscillator which generates a variable output clock signal according to the adjustment signal; and a modulation clock generation unit which generates modulated clock signals using an output clock signal to provide them to the phase detector. The phase detector sequentially receives the modulated clock signals that the modulation clock generation unit generates by modulating a phase of the output clock signal so as to have different phases. The phase detector compares phases of the sequentially input modulated clock signal and a data clock signal to output the comparison signal. According to an exemplary embodiment of the inventive concept, an area and power consumption of the phase detector are minimized, thereby making it possible to implement a phase detector having a multi-level phase detection characteristic.

[0034] FIG. 2 is a block diagram schematically illustrating a clock and data restoration device according to an exemplary embodiment of the inventive concept. A clock and data restoration device 100 may be implemented at a data receiver stage. The clock and data restoration device 100 receives a data clock signal from a data transmitter stage, restores a clock fit to a data rate of the data receiver stage from the data clock signal including noise, and restores noise-free and refined data through a sampling operation using the restored clock.

[0035] Referring to FIG. 2, the clock and data restoration device 100 according to an exemplary embodiment of the inventive concept contains a phase detector 110, a charge pump unit 120, a loop filter unit 130, a voltage controlled oscillator 140, and a modulation clock generation unit 150. The phase detector 110 receives the data clock signal and compares a phase of a data clock signal with a phase of a signal from the modulation clock generation unit 150 using an output clock signal from the voltage controlled oscillator 140 and modulated clock signals obtained by phase-modulating the output clock signal and outputs a comparison signal as a comparison result. The phase detector 110 sequentially receives the modulated clock signals that are modulated to have different phases using the output clock signal of the voltage controlled oscillator 140. The phase detector 110 compares phases of each of the modulated clock signals received sequentially and the data clock signal. A detailed structure, a detailed function, and an operation of the phase detector 110 will be described later.

[0036] The charge pump unit 120 adjusts the amount of charges to be supplied according to the comparison signal from the phase detector 110. The loop filter 130 accumulates the amount of charges adjusted by the charge pump unit 120 and outputs an adjustment signal. The voltage controlled oscillator 140 generates an output clock signal variable according to the adjustment signal from the loop filter unit 130. The modulation clock generation unit 150 modulates a phase of the output clock signal from the voltage controlled oscillator 140 to generate the modulated clock signals. The modulation clock generation unit 150 generates the modulated clock signals using the output clock signal so as to have different phases. The modulation clock generation unit 150 provides the phase detector 110 with the output clock signal and the modulated clock signals. The modulation clock generation unit 150 sequentially provides the modulated clock signals to the phase detector 110 by lapse of time.

[0037] FIG. 3 is a diagram schematically illustrating modulated clock signals generated from a modulation clock generation unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept. Referring to FIGS. 2 and 3, a modulation clock generation unit 150 generates modulated clock signals, including a first modulated clock signal(s) Lclk and a second modulated clock signal(s) Rclk, using an output clock signal from a voltage controlled oscillator 140. In FIG. 3, an embodiment of the inventive concept is exemplified as there are generated a total of 32 modulated clock signals including first sixteen modulated clock signals Lclk and second sixteen modulated clock signals Rclk. However, the inventive concept specified by the appended claims may not be limited thereto.

[0038] The modulation clock generation unit 150 generates the first modulated clock signals Lclk, which are modulated from an output clock signal of a voltage controlled oscillator 140 to have a phase preceding a predetermined reference phase Cclk, based on the output clock signal and generates the second modulated clock signals Rclk, which are modulated from the output clock signal to have a phase lagging the reference phase Cclk, based on the output clock signal. The reference phase Cclk may be a 180° phase of the output clock signal of the voltage controlled oscillator 140. Alternatively, the reference phase Cclk may be set to have any other phase value of 0°.

[0039] To make phase detecting better, the modulated clock signals may be modulated to have a linear phase difference from the reference phase Cclk of the output clock signal. As illustrated in FIG. 3, the modulation clock generation unit 150 modulates a phase of the output clock signal from the voltage controlled oscillator 140 to have a constant phase difference $\Delta\Phi$ between adjacent modulated clock signals.

[0040] The modulation clock generation unit 150 outputs a pair of corresponding modulated clock signals among the first modulated clock signals Lclk and the second modulated clock signals Rclk to a phase detector 110 during a predetermined time period. In FIG. 3, the pair of corresponding modulated clock signals of the modulated clock signals may be marked by the same two-digit number "00", "01"... "15". The modulation clock generation unit 150 may sequentially output the modulated clock signals from "00" to "15" or vice versa. The modulation clock generation unit 150 provides the phase detector 110 with each pair of modulated clock signals during the same time period.

[0041] FIG. 4A is a detailed block diagram illustrating a clock and data recovery device according to an exemplary embodiment of the inventive concept. Referring to FIG. 4A, a phase detector 110 contains a first phase com-

parison unit 112 and a second phase comparison unit 111. A charge pump unit 120 contains a first charge pump 122 and a second charge pump 121.

[0042] The first phase comparison unit 112 sequentially receives modulated clock signals from a modulation clock generation unit 150 and compares a phase of a data clock signal with a phase of each modulated clock signal every rising edge of the output clock signal using the modulated clock signal as a sampling signal. The first phase comparison unit 112 outputs a first comparison signal as a comparison result. The first phase comparison unit 112 determines a phase difference between the output clock signal from the voltage controlled oscillator 140 and the data clock signal as being one of multiple levels (or multi-level). The number of multiple levels may correspond to the number of paired modulated clock signals that the modulation clock generation unit 150 generates to have different phases.

[0043] The second phase comparison unit 111 compares phases of the data clock signal and the output clock signal of the voltage controlled oscillator 140 to output a second comparison signal. The second phase comparison unit 111 receives the output clock signal of the voltage controlled oscillator 140 as a sampling signal. The second phase comparison unit 111 compares phases of the data clock signal and the output clock signal every rising edge of the output clock signal of the voltage controlled oscillator 140. The second phase comparison unit 111 outputs a second comparison signal as a result of determining whether a phase of the output clock signal precedes a phase of the data clock signal. For example, the second phase comparison unit 111 may be implemented with a Bang-Bang Phase Detector (BBPD).

[0044] The second charge pump 121 adjusts the amount of charges to be supplied in response to the second comparison signal from the second phase comparison unit 111. The second phase comparison unit 111 implemented with the bang-bang phase detector determines whether a phase of the output clock signal is leading or lagging the data clock signal, but it does not determine how a phase of the output clock signal is leading or lagging the data clock signal. The clock and data recovery device 100 according to an exemplary embodiment of the inventive concept includes the first phase comparison unit 112 to determine a phase difference between the output clock signal and the data clock signal.

[0045] FIG. 4B is a diagram illustrating a modulated clock signal input to a first phase comparison unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept. In FIG. 4B, signals designated by a dotted line correspond to first modulation clocks signal Lclk shown in FIG. 3, and signals designated by a solid line correspond to second modulated clock signals Rclk. In illustration of FIG. 4, a reference phase of an output clock signal of a voltage controlled oscillator 140 may be set to "0°". As illustrated, in the event that first N modulated clock signals Lclk and second N modulated clock signals Rclk are sequentially provided to a first phase comparison unit 112, a phase difference between the data clock signal and the output clock signal may be detected as one of N phase differences. Accordingly, as a phase interval between modulated clock signals becomes narrower and as the number of modulated clock signals increases, a phase difference between the data clock signal and the output clock signal is determined more precisely.

[0046] Returning to FIG. 4B, a first charge pump 122 adjusts the amount of charges to be supplied in response to a first comparison signal from a first phase comparison unit 112. A loop filter unit 130 sums the amount of charges to be supplied of the first charge pump 122 and the amount of charges to be supplied of a second charge pump 121 for accumulation. The voltage controlled oscillator 140 adjusts the output clock signal according to an output value (adjustment signal) of the loop filter unit 130, so the output clock signal is synchronized with the data clock signal. The voltage controlled oscillator 140 may be implemented with, but not limited to, a voltage control type oscillator or a current control type oscillator. The output clock signal output from the voltage controlled oscillator 140 may be generated to be fit to a data rate of a data receiver stage. In exemplary embodiments, the data clock signal may be sampled using a 180° phase of the output clock signal as a sampling signal. Sampling of the data clock signal may be performed, for example, by a second phase comparison unit 111.

[0047] FIG. 5A is a timing diagram for describing a function of a modulation clock generation unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept. Referring to FIGS. 4A and 5A, a modulation clock generation unit 150 contains a frequency divider 151, a bit generator 152, and a modulation clock output unit 153. The frequency divider 151 divides a frequency of an output clock signal f_{clock} by 1/M (M being an integer of 2 or more) to generate a frequency division clock signal f_{clock}/M. The frequency division clock signal f_{clock}/M may have a period corresponding to M times the period of the output clock signal f_{clock}.

[0048] The bit generator 152 generates a bit signal in response to a clock edge of the frequency division clock signal f_{clock}/M, for example, a rising edge thereof. The modulation clock output unit 153 sequentially outputs modulated clock signals Lclk and Rclk according to the bit signal that the bit generator 152 generates. FIG. 5B is an expanded diagram of a portion "A" of FIG. 5A, and FIG. 5C is an expanded diagram of a portion "B" of FIG. 5A. Referring to FIGS. 4A and 5A to 5C, the modulation clock output unit 153 sequentially outputs the modulated clock signals Lclk and Rclk in synchronization with a rising edge of the bit signal from the bit generator 152. The modulated clock signals Lclk and Rclk may be sequentially input to a first phase comparison unit 112.

[0049] FIG. 6 is a diagram for describing a function of a second phase comparison unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept. FIG. 7 is a diagram for describ-

ing a function of a first phase comparison unit of a clock and data recovery device according to an exemplary embodiment of the inventive concept. FIGS. 8A to 8D are diagrams for describing a function of a phase detector according to an exemplary embodiment of the inventive concept. A second phase comparison unit 111, as illustrated in FIG. 6, outputs a second comparison signal as a result of only determining whether an output clock signal is leading or lagging a data clock signal. When a phase difference value between the data clock signal and the output clock signal is greater than a phase modulation value of a modulated clock signal, as illustrated in FIG. 7, a first phase comparison unit 112 outputs a first comparison signal for adjusting a phase of the output clock signal.

[0050] When a phase difference value between the data clock signal and the output clock signal is smaller than "Φ_1", the first phase comparison unit 112 does not output the first comparison signal for adjusting a phase of the output clock signal with respect to all modulated clock signals. When a phase difference value between the data clock signal and the output clock signal is greater than "Φ_N", the first phase comparison unit 112 outputs the first comparison signal for adjusting a phase of the output clock signal with respect to all modulated clock signals. Accordingly, the first phase comparison unit 112 outputs the first comparison signal for adjusting a phase of the output clock signal only if there is received a modulated clock signal having a phase modulation value smaller than a phase difference value between the data clock signal and the output clock signal. As illustrated in FIG. 8A, a phase of the data clock signal may be determined in a multi-level according to the first comparison signal accumulated with respect to all modulated clock signals.

[0051] A modulation clock generation unit 150 provides each of the modulated clock signals to a phase detector 110 during a predetermined time period. To improve a performance index of a clock and data recovery device, the time period where each modulated clock signal is provided to the phase detector 110 may be previously determined to have an optimum value according to the repetition rate of the modulated clock signal, the number of modulated clock signals, or a jitter characteristic of restored data.

[0052] Referring to FIG. 8B, in the event that an input data clock signal includes great noise, a phase modulation level of modulated clock signals, the level number of modulated clock signals and a time period where modulated clock signals are provided to the phase detector 110 may be set such that gain G, that is, a change ratio of an output current value (the amount of charges) of a charge pump unit 120 to a phase modulation step is decreased. In other exemplary embodiments, when the input data clock signal includes relatively small noise, the gain G may be decreased. In still other exemplary embodiments, the gain G may be decreased if the number of modulated clock signals, that is, the number of levels is set to a relatively great value and may be increased if the number of levels is set to a relatively small value. With the above description, it is possible to improve a jitter characteristic of restored data and a band-width characteristic of a clock and data recovery device.

[0053] Referring to FIGS. 8C and 8D, a gain is changed differently according to an interval of modulated clock signals by increasing a time when a modulated clock signal experiencing relatively great phase modulation is provided to a phase detector. Accordingly, a performance index of the clock and data recovery device is improved.

[0054] FIG. 9 is a detailed block diagram illustrating a phase detector of a clock and data recovery device according to an exemplary embodiment of the inventive concept. Referring to FIG. 9, a second phase comparison unit 111 contains a first flip-flop 1111, a second flip-flop 1112, a third flip-flop 1113, a fourth flip-flop 1114, a first XOR gate 1115, and a second XOR gate 1116. The first flip-flop 1111 outputs a data clock signal in response to a first clock edge (e.g., a rising edge) CK0 of an output clock signal of a voltage controlled oscillator 140. The second flip-flop 1112 outputs an output value of the first flip-flop 1111 in response to a first clock edge CK0. The third flip-flop 1113 outputs the data clock signal in response to a second clock edge (e.g., a falling edge) CK180 of the output clock signal. The fourth flip-flop 1114 outputs an output value of the third flip-flop 1113 in response to the first clock edge CK0.

[0055] The first XOR gate 1115 compares the output value of the first flip-flop 1111 and the output value of the fourth flip-flop 1114. The second XOR gate 1116 compares the output value of the second flip-flop 1112 and the output value of the fourth flip-flop 1114. A second comparison signal from the second phase comparison unit 111, that is, an output value of the first XOR gate 1115 and an output value of the second XOR gate 1116 are provided to a second charge pump 121.

[0056] A first phase comparison unit 112 contains a fifth flip-flop 1121, a sixth flip-flop 1122, a seventh flip-flop 1123, an eighth flip-flop 1124, a third XOR gate 1125, and a fourth XOR gate 1126. The fifth flip-flop 1121 outputs a data clock signal in response to a first modulated clock signal CK180-pi (Lclk) sequentially input by a given time interval. The sixth flip-flop 1122 outputs an output value of the fifth flip-flop 1121 in response to the first clock edge CK0 of the output clock signal. The seventh flip-flop 1123 outputs the data clock signal in response to a second modulated clock signal CK180+pi (Rclk) sequentially input by a given time interval. The eighth flip-flop 1124 outputs an output value of the seventh flip-flop 1123 in response to the first clock edge CK0 of the output clock signal.

[0057] The third XOR gate 1125 compares an output value of the fourth or fifth flip-flop 1114 or 1121 and an output value of the sixth flip-flop 1122. The fourth XOR gate 1126 compares an output value of the second or fourth fifth flip-flop 1122 or 1114 and an output value of the eighth flip-flop 1124. A first comparison signal from the first phase comparison unit 112, that is, an output

value of the third XOR gate 1125 and an output value of the fourth XOR gate 1126 are provided to a first charge pump 122.

[0058] FIGS. 10 and 11 are diagrams for describing an operation of a clock and data recovery device according to an exemplary embodiment of the inventive concept. Referring to FIGS. 10 and 11, there are generated three pairs of modulated clock signals modulated according to three different phase modulation levels Φ_1, Φ_2, and Φ_3. The modulated clock signals are sequentially input to a phase detector. Current values of a charge pump unit 120 about data clock signals corresponding to four cases shown in FIG. 10 are illustrated in FIG. 11. In FIG. 11, "I_{CP1}" denotes a current value of a second charge pump 121 according to an output of a second phase comparison unit 111, and "I_{CP2}" denotes a current value of a first charge pump 122 according to an output of a first phase comparison unit 112.

[0059] For case 1, a phase difference between an output clock signal of a voltage controlled oscillator 140 and a data clock signal belongs to dead-zones between all modulated clock signal pairs, so the current I_{CP2} does not flow to the first charge pump 122 with respect to all modulated clock signals. Here, the dead-zone may mean a phase zone between paired modulated clock signals. Since a phase difference between the output clock signal and the data clock signal increases toward case 4 from case 2, a time when the current I_{CP2} flows to the first charge pump 122 increases stepwise. For case 4, a phase difference between the output clock signal and the data clock signal gets out of dead-zones between all modulated clock signal pairs. In this case, the current I_{CP2} flows to the first charge pump 122 regardless of a received modulated clock signal. According to an exemplary embodiment of the inventive concept, it is possible to minimize hardware components to be added and to implement a multi-level phase detector. In addition, it is possible to make a clock and data recovery device formed in a small area and having a low-power characteristic. The phase detector and the clock and data recovery device according to an exemplary embodiment of the inventive concept are applicable to a phase locked loop circuit.

[0060] FIG. 12A is a block diagram schematically illustrating a clock and data recovery device according to another exemplary embodiment of the inventive concept. In describing an embodiment of FIG. 12A, a description about components that are identical or equal to those of the above-described embodiment is omitted. Referring to FIG. 12A, a clock and data recovery device 100 contains a phase detector 110, a charge pump unit 120, a loop filter unit 130, a voltage controlled oscillator 140, a modulation clock generation unit 150, and a jitter measurement unit 160.

[0061] The jitter measurement unit 160 measures jitter of the clock and data recovery device 100 by comparing cumulative values of comparison signal from the phase detector 110 for different modulated clock signals. The jitter measurement unit 160 may measure the jitter by analyzing each cumulative value, corresponding to each of the modulated clock signals, through a histogram method.

[0062] FIG. 12B is a detailed block diagram illustrating a clock and data recovery device of FIG. 12A. Referring to FIGS. 12A and 12B, a jitter measurement unit 160 contains a plurality of counters 162, a selection circuit 164, and a histogram analysis unit 166. Each of the counters 162 may be provided for each modulated clock signal. The counters 162 individually measure cumulative values of comparison signal that correspond to modulated clock signals sequentially input to a first phase comparison unit 112. The selection circuit 164 is connected between a first phase comparison unit 112 and the counters 162 and selects one or more of the counters 162 in accordance with the modulated clock signal input to the first phase comparison unit 112. The histogram analysis unit 166 measures jitter through a histogram analysis about cumulative values respectively measured by the counters 162.

[0063] In an embodiment of FIG. 12B, there are provided 2N counters C_{-N}, C_{-N+1}... C_N corresponding to N pairs of modulated clock signals. In exemplary embodiments, the selection circuit 164 may select a counter by turning on a switch (e.g., a transistor) in the following order according to a bit signal of a bit generator 152: $(C_1, C_{-1}) \rightarrow (C_2, C_{-2}) \ldots (C_{N-1}, C_{-N+1}) \rightarrow (C_N, C_{-N})$. The selected counter counts the event that a phase of a data clock signal gets out of a phase zone (dead-zone) between paired modulated clock signals. That is, the selected counter (or accumulator) may count and accumulate the event that a transition of the data clock signal gets out of a dead-zone.

[0064] In exemplary embodiments, N counters C_1 to C_N may count the event that the data clock signal is changed at the right of a modulated clock signal, that is, the event that a phase of the data clock signal is lagging a modulated clock signal. Remaining counters C_{-1} to C_{-N} may count the event that the data clock signal is changed at the left of a modulated clock signal, that is, the event that a phase of the data clock signal is leading a modulated clock signal.

[0065] FIGS. 13A to 13C and 14 are diagrams for describing a jitter measurement method of a clock and data recovery device of FIG. 12B. Referring to FIG. 13A, when an x-th modulated clock signal is input to a first phase comparison unit 112, a selected counter with respect to the x-th modulated clock signal counts a comparison signal from the first phase comparison unit 112 and provides a histogram analysis unit 166 with a cumulative value C_x of the count result. When an x+1st modulated clock signal is input to the first phase comparison unit 112, a selected counter with respect to the x+1st modulated clock signal counts a comparison signal from the first phase comparison unit 112 and provides the histogram analysis unit 166 with a cumulative value C_{x+1} of the count result.

[0066] Referring to FIG. 13C, the histogram analysis

unit 166 subtracts the cumulative value C_{x+1} of the x+1st counter from the cumulative value C_x of the x-th counter. A subtracted value (C_x - C_{x+1}) indicates the number of events that a data clock signal transitions between phases Φ_x and Φ_{x+1}. A histogram diagram shown in FIG. 14 is obtained through subtracting results of cumulative values between counters 162 with respect to all dead-zones. In FIG. 13, a "Co" value is set to a value with respect to the number of data edges that exists between Φ_0 and Φ_1 under a condition where a data transition occurs between Φ_{-1} and Φ_1.

[0067] It is understood that jitter is smaller as a jitter histogram is focused toward a center. That the jitter histogram is distributed means that the jitter is greater. As the jitter of a clock and data recovery device becomes smaller, there is reduced the number of events that a data clock signal transitions at a phase zone between adjacent modulated clock signals, with a phase of an output clock signal synchronized with the clock and data recovery device. In this case, values $C_{\pm1}$, $C_{\pm2}$... $C_{\pm N}$ measured by counters are reduced, thereby making a jitter histogram distribution focused toward a center.

[0068] In contrast, as the jitter of the clock and data recovery device becomes greater, there is increased the number of events that a data clock signal transitions at a phase zone between adjacent modulated clock signals, with a phase of an output clock signal synchronized with the clock and data recovery device. In this case, a level of jitter measured by a counter may permit values $C_{\pm1}$, $C_{\pm2}$... $C_{\pm N}$ to increase, values (C_0 - C_1) and (C_0 - C_{-1}) to relatively decrease, and values (C_1 - C_2) and (C_2 - C_3) to relatively increase. This means that the jitter histogram distribution becomes wide.

[0069] Thus, it is possible to monitor the jitter of the clock and data recovery device from the jitter histogram distribution. According to an exemplary embodiment of the inventive concept, how many a signal transition occurs between dead-zones is determined through simple calculation. This is converted into the form of quantity and shape of a jitter distribution by analyzing the jitter histogram, thereby making it possible to monitor the jitter of the clock and data recovery device.

[0070] A clock and data recovery device according to an exemplary embodiment of the inventive concept outputs a comparison signal as a result of comparing phases between a data clock signal and each modulated clock signal modulated to have different phases using an output clock signal. The clock and data recovery device measures jitter by comparing cumulative values of comparison signals corresponding to the modulated clock signals. Accordingly, it is possible to measure the jitter of the clock and data recovery device simply and efficiently by maximally using circuits that the clock and data recovery device itself includes.

[0071] While the inventive concept has been described with reference to exemplary embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the the inventive concept specified by the appended claims. Therefore, it should be understood that the above embodiments are not limiting, but illustrative.

Claims

1. A clock and data recovery device (100) comprising:

a phase detector (110) configured to output a comparison signal;
a charge pump unit (120) configured to adjust an amount of charges to be supplied according to the comparison signal;
a loop filter unit (130) configured to accumulate the amount of charges to be supplied to output an adjustment signal;
a voltage controlled oscillator (140) configured to generate an output clock signal variable according to the adjustment signal; **characterized by**
a modulation clock generation unit (150) configured to modulate the phase of the output clock signal to generate pairs of corresponding modulated clock signals among first modulated clock signals (Lclk) having a phase preceding a predetermined reference phase (Cclk) and second modulated clock signals (Rclk) having a phase lagging said reference phase (Cclk) and to provide the pairs of modulated clock signals sequentially to the phase detector(110),
wherein the phase detector (110) is configured to receive the data clock signal and the pairs of modulated clock signals, and to compare phases of the data clock signal and each of the sequentially received pairs of modulated clock signals, to output the comparison signal.

2. The clock and data recovery device (100) of claim 1, wherein the modulation clock generation unit (150) comprises:

a frequency divider (151) configured to divide a frequency of the output clock signal to generate a frequency division clock signal;
a bit generator (152) configured to generate a bit signal in response to a clock edge of the frequency division clock signal; and
a modulation clock output unit (153) configured to sequentially output the pairs of modulated clock signals according to the bit signal.

3. The clock and data recovery device (100) of claim 1, wherein the modulation clock generation unit (150) is configured to generate the sequential, modulated clock signals with a linearly varying phase difference from the output clock signal.

4. The clock and data recovery device (100) of claim 1, wherein the modulation clock generation unit (150) is configured to provide the phase detector (110) with each pair of modulated clock signals during a predetermined time period, and the predetermined time period of each pair of modulated clock signal is set according to the repetition rate of the pair of modulated clock signals the number of modulated clock signals, or both.

5. The clock and data recovery device (100) of claims 1 or 3, wherein the phase detector (110) comprises:

a first phase comparison unit (112) configured to sequentially compare a phase of the data clock signal and a phase of each modulated clock signal to output a first comparison signal.

6. The clock and data recovery device (100) of claim 5, wherein the phase detector (110) further comprises:

a second phase comparison unit (111) configured to compare phases of the data clock signal and the output clock signal to output a second comparison signal.

7. The clock and data recovery device (100) of claim 6, wherein the charge pump unit (120) comprises:

a first charge pump (122) configured to adjust the amount of charges to be supplied according to the first comparison signal; and
a second charge pump (121) configured to adjust the amount of charges to be supplied according to the second comparison signal.

8. The clock and data recovery device (100) of claim 7, wherein the second phase comparison unit (111) comprises:

a first flip-flop (1111) configured to output the data clock signal in response to a first clock edge of the output clock signal;
a second flip-flop (1112) configured to output an output value of the first flip-flop (1111) in response to the first clock edge;
a third flip-flop (1113) configured to output the data clock signal in response to a second clock edge of the output clock signal;
a fourth flip-flop (1114) configured to output an output value of the third flip-flop (1113) in response to the first clock edge;
a first XOR gate (1115) configured to compare the output value of the first flip-flop (1111) and an output value of the fourth flip-flop (1114); and
a second XOR gate (1116) configured to compare an output value of the second flip-flop (1112) and the output value of the fourth flip-flop (1114).

9. The clock and data recovery device (100) of claim 8, wherein the first phase comparison unit (112) comprises:

a fifth flip-flop (1121) configured to output the data clock signal in response to a first modulated clock signal sequentially input;
a sixth flip-flop (1122) configured to output an output value of the fifth flip-flop (1121) in response to the first clock edge;
a seventh flip-flop (1123) configured to output the data clock signal in response to a second modulated clock signal sequentially input;
an eighth flip-flop (1124) configured to output an output value of the seventh flip-flop (1123) in response to the first clock edge;
a third XOR gate (1125) configured to compare the output value of the first flip-flop (1111) or fourth flip-flop (1114) and an output value of the sixth flip-flop (1122); and
a fourth XOR gate (1126) configured to compare the output value of the second flip-flop (1112) or fourth flip-flop (1114) and an output value of the eighth flip-flop (1124).

10. The clock and data recovery device (100) of claim 9, wherein the first modulated clock signal is a signal having a phase leading the output clock signal, and wherein the second modulated clock signal is a signal having a phase lagging the output clock signal.

11. The clock and data recovery device (100) of claim 9, wherein the first comparison signal comprises an output value of the first XOR gate (1115) and an output value of the second XOR gate (1116), and
wherein the second comparison signal comprises an output value of the third XOR gate (1125) and an output value of the fourth XOR gate (1126).

Patentansprüche

1. Takt- und Datenwiederherstellungsvorrichtung (100), die umfasst:

einen Phasendetektor (110), der konfiguriert wird, ein Vergleichssignal auszugeben; eine Ladungspumpeneinheit (120), die konfiguriert wird, eine gemäß dem Vergleichssignal zu liefernden Menge von Ladungen einzustellen;
eine Schleifenfiltereinheit (130), die konfiguriert wird, die Menge von zu liefernden Ladungen aufzuspeichern, um ein Einstellsignal auszugeben;
einen spannungsgesteuerten Oszillator (140),

der konfiguriert wird, eine Ausgangtaktsignalgröße gemäß dem Einstellsignal zu erzeugen; **gekennzeichnet durch**

eine Einheit zur Modulationstakterzeugung (150), die konfiguriert wird, die Phase des Ausgangstaktsignals anzupassen, um entsprechend modulierte Taktsignalpaare unter ersten modulierten Taktsignalen (Lclk) mit einer einer vorgegebenen Referenzphase (Cclk) voreilenden Phase und zweiten modulierten Taktsignalen (Rclk) mit einer der Referenzphase (Cclk) nacheilenden Phase zu erzeugen, und

die modulierten Taktsignalpaare dem Phasendetektor (110) sequentiell bereitzustellen,

wobei der Phasendetektor (110) konfiguriert wird, das Datentaktsignal und die modulierten Taktsignalpaare zu empfangen und Phasen des Datentaktsignals und jedes der sequentiell empfangenen modulierten Taktsignalpaare zu vergleichen, um das Vergleichssignal auszugeben.

2. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 1, wobei die Einheit für Modulationstakterzeugung (150) umfasst:

einen Frequenzteiler (151), der konfiguriert wird, eine Frequenz des Ausgangstaktsignals zu teilen, um ein Frequenzteilungstaktsignal zu erzeugen;

einen Bitgenerator (152), der konfiguriert wird, ein Bitsignal als Reaktion auf eine Taktflanke des Frequenzteilungstaktsignals zu erzeugen; und

eine Ausgabeeinheit für Taktmodulation (153), die konfiguriert wird, die modulierten Taktsignalpaare gemäß dem Bitsignal sequentiell auszugeben.

3. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 1, wobei die Einheit für Modulationstakterzeugung (150) konfiguriert wird, die sequentiellen, modulierten Taktsignale mit einer linear variierenden Phasendifferenz aus dem Ausgangstaktsignal zu erzeugen.

4. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 1, wobei die Einheit für Modulationstakterzeugung (150) konfiguriert wird, dem Phasendetektor (110) jedes Paar modulierter Taktsignale während einer vorgegebenen Zeitdauer bereitzustellen, und

die vorgegebene Zeitdauer jedes Paars modulierter Taktsignale gemäß der Wiederholungsrate des Paars modulierter Taktsignale oder der Anzahl der modulierten Taktsignale, oder beider, eingestellt wird.

5. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 1 oder 3, wobei der Phasendetektor (110) umfasst:

eine erste Phasenvergleichseinheit (112), die konfiguriert wird, eine Phase des Datentaktsignals und eine Phase jedes modulierten Taktsignals sequentiell zu vergleichen, um ein erstes Vergleichssignal auszugeben.

6. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 5, wobei der Phasendetektor (110) des Weiteren umfasst:

eine zweite Phasenvergleichseinheit (111), die konfiguriert wird, Phasen des Datentaktsignals und des Ausgangstaktsignals zu vergleichen, um ein zweites Vergleichssignal auszugeben.

7. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 6, wobei die Ladungspumpeneinheit (120) umfasst:

eine erste Ladungspumpe (122), die konfiguriert wird, die Menge von zu liefernden Ladungen gemäß dem ersten Vergleichssignal einzustellen; und

eine zweite Ladungspumpe (121), die konfiguriert wird, die Menge von zu liefernden Ladungen gemäß dem zweiten Vergleichssignal einzustellen.

8. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 7, wobei die zweite Phasenvergleichseinheit (111) umfasst:

ein erstes Flip-Flop (1111), das konfiguriert wird, das Datentaktsignal als Reaktion auf eine erste Taktflanke des Ausgangstaktsignals auszugeben;

ein zweites Flip-Flop (1112), das konfiguriert wird, einen Ausgangswert des ersten Flip-Flops (1111) als Reaktion auf die erste Taktflanke auszugeben;

ein drittes Flip-Flop (1113), das konfiguriert wird, das Datentaktsignal als Reaktion auf eine zweite Taktflanke des Ausgangstaktsignals auszugeben;

ein viertes Flip-Flop (1114), das konfiguriert wird, einen Ausgangswert des dritten Flip-Flops (1113) als Reaktion auf die erste Taktflanke auszugeben;

ein erstes XOR-Gatter (1115), das konfiguriert wird, den Ausgangswert des ersten Flip-Flops (1111) und einen Ausgangswert des vierten Flip-Flops (1114) zu vergleichen; und

ein zweites XOR-Gatter (1116), das konfiguriert wird, einen Ausgangswert des zweiten Flip-

Flops (1112) und den Ausgangswert des vierten Flip-Flops (1114) zu vergleichen.

9. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 8, wobei die erste Phasenvergleichseinheit (112) umfasst:

ein fünftes Flip-Flop (1121), das konfiguriert wird, das Datentaktsignal als Reaktion auf ein erstes sequentiell eingegebenes moduliertes Taktsignal auszugeben;
ein sechstes Flip-Flop (1122), das konfiguriert wird, einen Ausgangswert des fünften Flip-Flops (1121) als Reaktion auf die erste Taktflanke auszugeben;
ein siebtes Flip-Flop (1123), das konfiguriert wird, das Datentaktsignal als Reaktion auf ein zweites sequentiell eingegebenes moduliertes Taktsignal auszugeben;
ein achtes Flip-Flop (1124), das konfiguriert wird, einen Ausgangswert des siebten Flip-Flops (1123) als Reaktion auf die erste Taktflanke auszugeben;
ein drittes XOR-Gatter (1125), das konfiguriert wird, den Ausgangswert des ersten Flip-Flops (1111) oder vierten Flip-Flops (1114) und einen Ausgangswert des sechsten Flip-Flops (1122) zu vergleichen; und
ein viertes XOR-Gatter (1126), das konfiguriert wird, den Ausgangswert des zweiten Flip-Flops (1112) oder vierten Flip-Flops (1114) und einen Ausgangswert des achten Flip-Flops (1124) zu vergleichen.

10. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 9, wobei das erste modulierte Taktsignal ein Signal mit einer dem Ausgangstaktsignal voreilenden Phase ist, und
wobei das zweite modulierte Taktsignal ein Signal mit einer dem Ausgangstaktsignal nacheilenden Phase ist.

11. Takt- und Datenwiederherstellungsvorrichtung (100) nach Anspruch 9, wobei das erste Vergleichssignal einen Ausgangswert des ersten XOR-Gatters (1115) und einen Ausgangswert des zweiten XOR-Gatters (1116) umfasst, und
wobei das zweite Vergleichssignal einen Ausgangswert des dritten XOR-Gatters (1125) und einen Ausgangswert des vierten XOR-Gatters (1126) umfasst.

Revendications

1. Dispositif d'extraction de signaux d'horloge et de données (100) comprenant :

un détecteur de phase (110) conçu pour délivrer en sortie un signal de comparaison ; une unité de pompes à charge (120) conçue pour régler une quantité de charges à délivrer conformément au signal de comparaison ;
une unité filtre à boucle (130) conçue pour accumuler la quantité de charges à délivrer de façon à délivrer en sortie un signal de réglage ;
un oscillateur commandé en tension (140) conçu pour générer un signal d'horloge de sortie variable conformément au signal de réglage ;
caractérisé par
une unité génératrice de signaux d'horloge de modulation (150) conçue pour moduler la phase du signal d'horloge de sortie de façon à générer des paires de signaux d'horloge modulés correspondants entre des premiers signaux d'horloge modulés (Lclk) ayant une phase en avance sur une phase de référence prédéterminée (Cclk) et des seconds signaux d'horloge modulés (Rclk) ayant une phase en retard sur ladite phase de référence (Cclk) et pour délivrer les paires de signaux d'horloge modulés séquentiellement au détecteur de phase (110),
dans lequel le détecteur de phase (110) est conçu pour recevoir le signal d'horloge de données et les paires de signaux d'horloge modulés, et pour comparer les phases du signal d'horloge de données et de chacune des paires reçues séquentiellement de signaux d'horloge modulés, de façon à délivrer en sortie le signal de comparaison.

2. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 1, dans lequel l'unité génératrice de signaux d'horloge de modulation (150) comprend :

un diviseur de fréquence (151) conçu pour diviser une fréquence du signal d'horloge de sortie de façon à générer un signal d'horloge de division de fréquence ;
un générateur de signal binaire (152) conçu pour générer un signal binaire en réponse à un front de signal d'horloge du signal d'horloge de division de fréquence ; et
une unité de sortie de signaux d'horloge de modulation (153) conçue pour délivrer séquentiellement les paires de signaux d'horloge modulés conformément au signal binaire.

3. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 1, dans lequel l'unité génératrice de signaux d'horloge de modulation (150) est conçue pour générer les signaux d'horloge modulés séquentiels avec un déphasage qui varie de façon linéaire par rapport au signal d'horloge de sortie.

4. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 1, dans lequel l'unité génératrice de signaux d'horloge de modulation (150) est conçue pour délivrer au détecteur de phase (110) chaque paire de signaux d'horloge modulés pendant une période de temps prédéterminée, et
la période de temps prédéterminée de chaque paire de signaux d'horloge modulés est fixée conformément au rythme de répétition de la paire de signaux d'horloge modulés, du nombre de signaux d'horloge modulés, ou des deux.

5. Dispositif d'extraction de signaux d'horloge et de données (100) selon les revendications 1 ou 3, dans lequel le détecteur de phase (110) comprend :

une première unité de comparaison de phases (112) conçue pour comparer séquentiellement une phase du signal d'horloge de données et une phase de chaque signal d'horloge modulé de façon à délivrer en sortie un premier signal de comparaison.

6. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 5, dans lequel le détecteur de phase (110) comprend en outre :

une seconde unité de comparaison de phases (111) conçue pour comparer des phases du signal d'horloge de données et du signal d'horloge de sortie de façon à délivrer en sortie un second signal de comparaison.

7. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 6, dans lequel l'unité de pompes à charge (120) comprend :

une première pompe à charge (122) conçue pour régler la quantité de charges à délivrer conformément au premier signal de comparaison ; et
une seconde pompe à charge (121) conçue pour régler la quantité de charges à délivrer conformément au second signal de comparaison.

8. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 7, dans lequel la seconde unité de comparaison de phases (111) comprend :

une première bascule (1111) conçue pour délivrer en sortie le signal d'horloge de données en réponse à un premier front de signal d'horloge du signal d'horloge de sortie ;
une deuxième bascule (1112) conçue pour délivrer en sortie une valeur de sortie de la première bascule (1111) en réponse au premier front de signal d'horloge ;
une troisième bascule (1113) conçue pour délivrer en sortie le signal d'horloge de données en réponse à un second front de signal d'horloge du signal d'horloge de sortie ;
une quatrième bascule (1114) conçue pour délivrer en sortie une valeur de sortie de la troisième bascule (1113) en réponse au premier front de signal d'horloge ;
une première porte OU exclusif (1115) conçue pour comparer la valeur de sortie de la première bascule (1111) et une valeur de sortie de la quatrième bascule (1114) ; et
une deuxième porte OU exclusif (1116) conçue pour comparer une valeur de sortie de la deuxième bascule (1112) et la valeur de sortie de la quatrième bascule (1114).

9. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 8, dans lequel la première unité de comparaison de phases (112) comprend :

une cinquième bascule (1121) conçue pour délivrer en sortie le signal d'horloge de données en réponse à une entrée séquentielle d'un premier signal d'horloge modulé ;
une sixième bascule (1122) conçue pour délivrer en sortie une valeur de sortie de la cinquième bascule (1121) en réponse au premier front de signal d'horloge ;
une septième bascule (1123) conçue pour délivrer en sortie le signal d'horloge de données en réponse à une entrée séquentielle d'un second signal d'horloge modulé ;
une huitième bascule (1124) conçue pour délivrer en sortie une valeur de sortie de la septième bascule (1123) en réponse au premier front de signal d'horloge ;
une troisième porte OU exclusif (1125) conçue pour comparer la valeur de sortie de la première bascule (1111) ou de la quatrième bascule (1114) et une valeur de sortie de la sixième bascule (1122) ; et
une quatrième porte OU exclusif (1126) conçue pour comparer la valeur de sortie de la deuxième bascule (1112) ou de la quatrième bascule (1114) et une valeur de sortie de la huitième bascule (1124).

10. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 9, dans lequel le premier signal d'horloge modulé est un signal ayant une phase en avance sur celle du signal d'horloge de sortie, et
dans lequel le second signal d'horloge modulé est un signal ayant une phase en retard sur celle du signal d'horloge de sortie.

11. Dispositif d'extraction de signaux d'horloge et de données (100) selon la revendication 9, dans lequel le premier signal de comparaison comprend une valeur de sortie de la première porte OU exclusif (1115) et une valeur de sortie de la deuxième porte OU exclusif (1116), et
dans lequel le second signal de comparaison comprend une valeur de sortie de la troisième porte OU exclusif (1125) et une valeur de sortie de la quatrième porte OU exclusif (1126).

FIG. 1

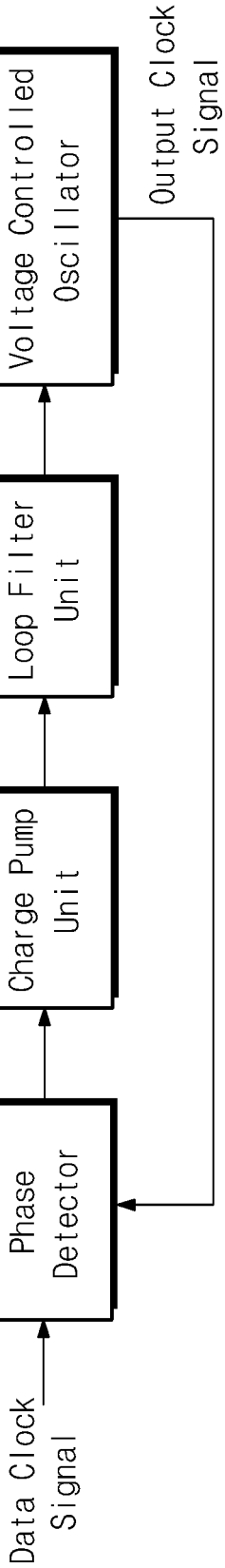

10
11
Phase Detector
12
Charge Pump Unit
13
Loop Filter Unit
14
Voltage Controlled Oscillator
Data Clock Signal
Output Clock Signal

FIG. 2

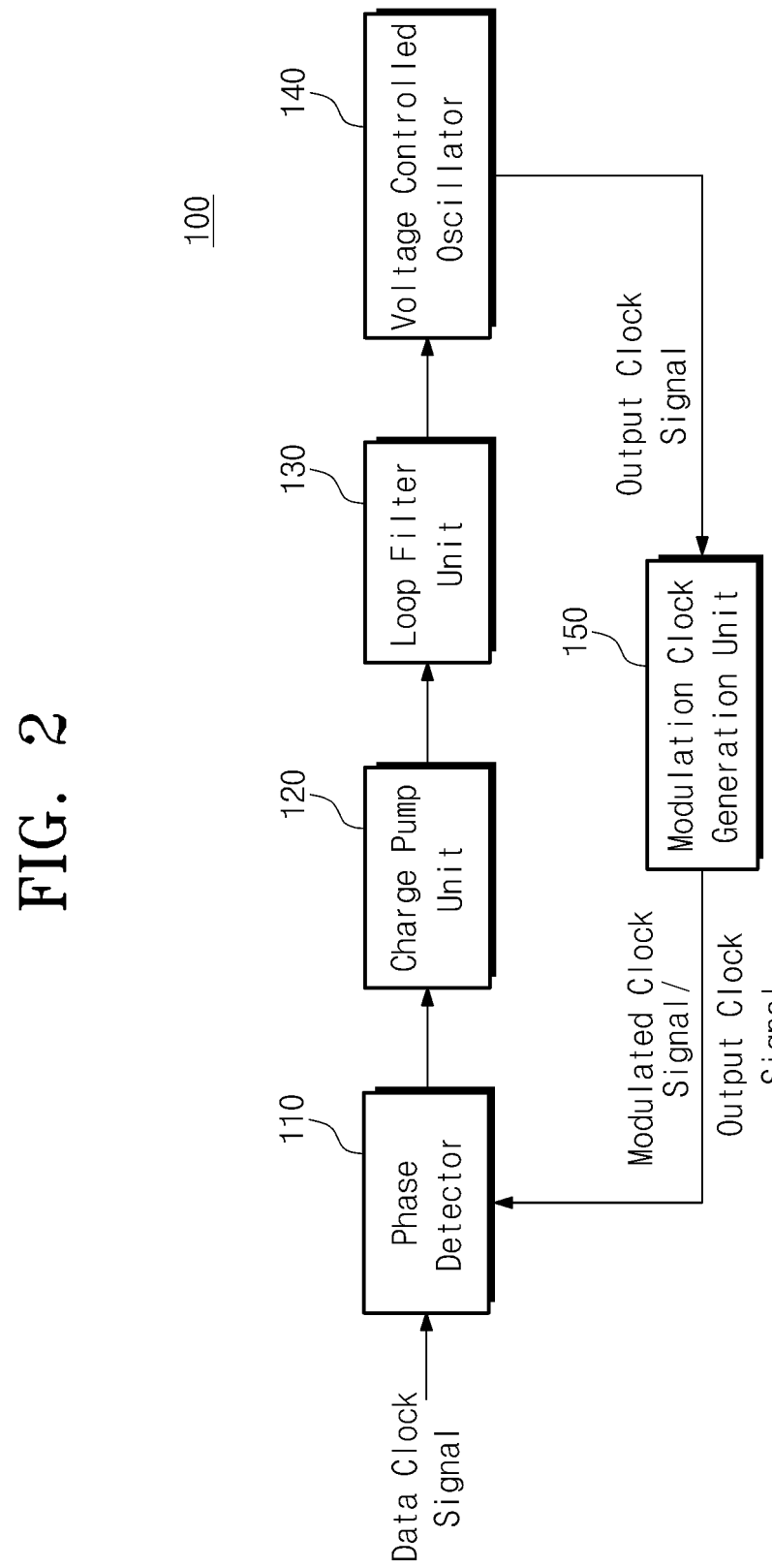

100
110
Phase Detector
120
Charge Pump Unit
130
Loop Filter Unit
140
Voltage Controlled Oscillator
150
Modulation Clock Generation Unit
Data Clock Signal
Modulated Clock Signal/ Output Clock Signal
Output Clock Signal

FIG. 3

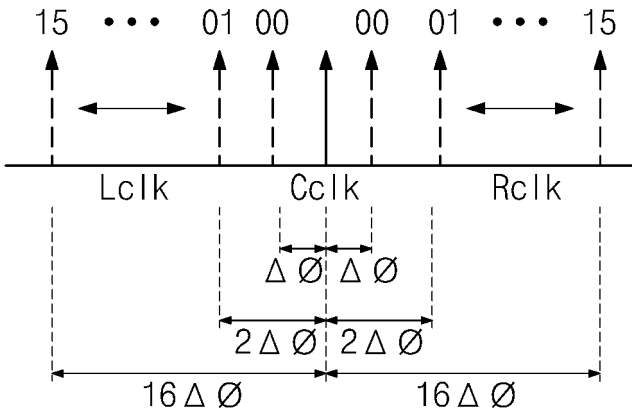


FIG. 4A

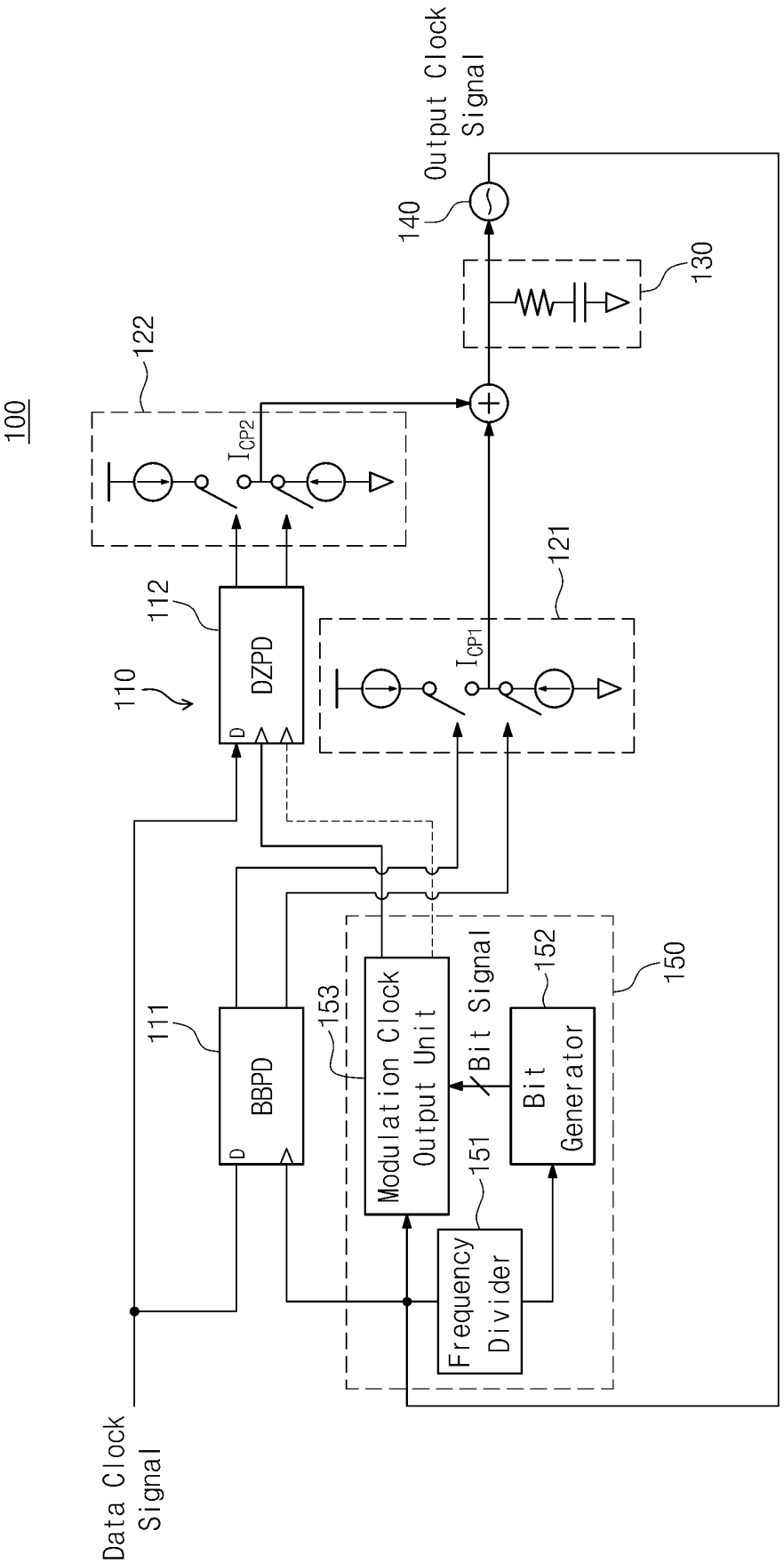

100
Data Clock Signal
Output Clock Signal
140
130
122
121
112
110
DZPD
D
I_{CP2}
I_{CP1}
111
BBPD
153
Modulation Clock Output Unit
Bit Signal
152
Bit Generator
150
151
Frequency Divider

FIG. 4B

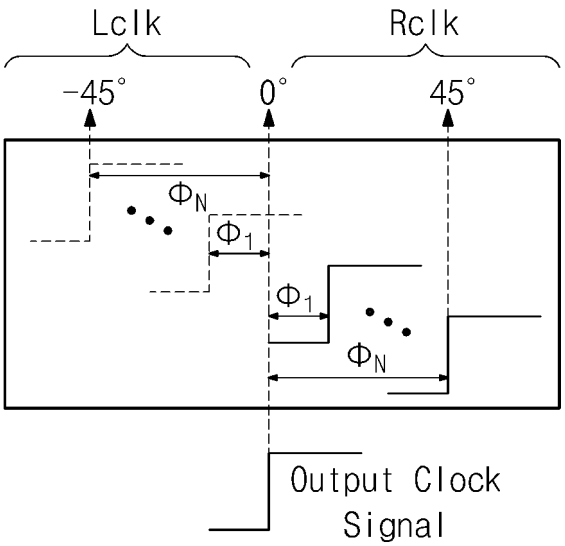


FIG. 5A

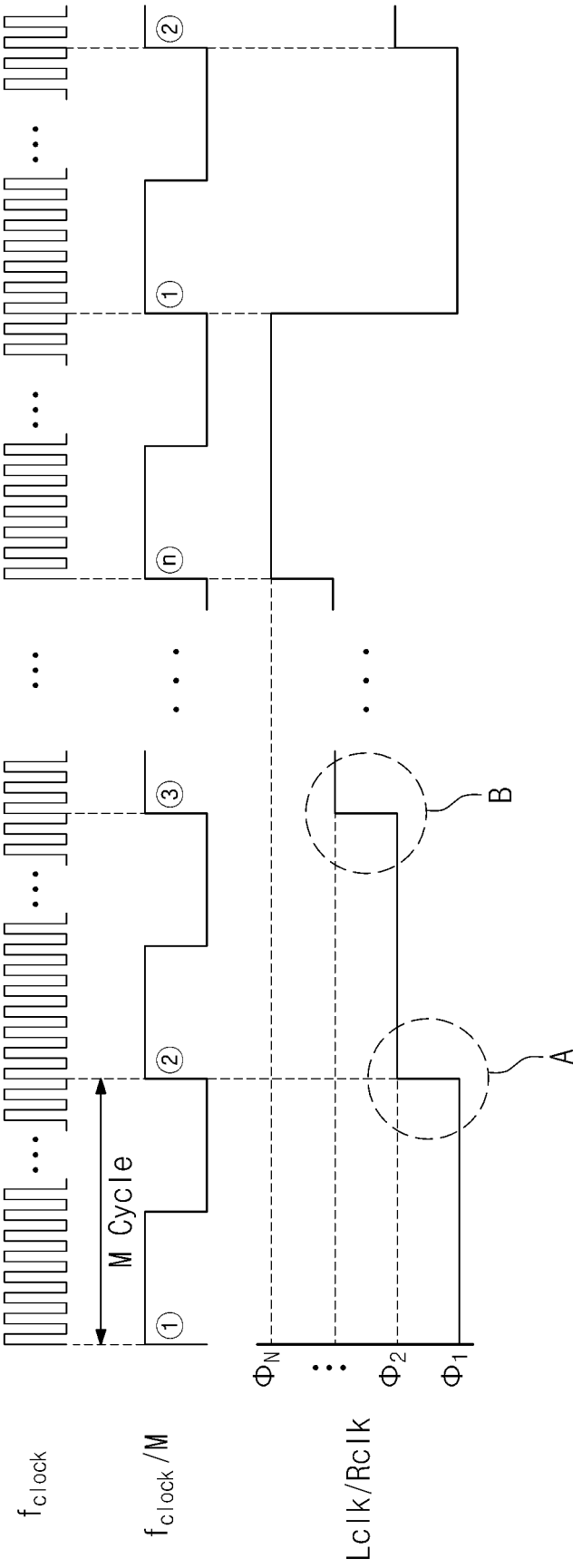


FIG. 5B

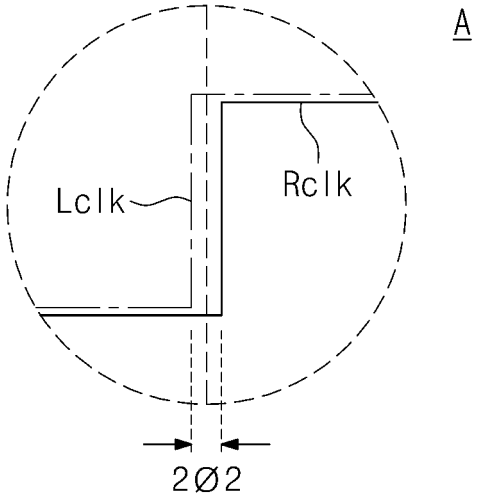


FIG. 5C

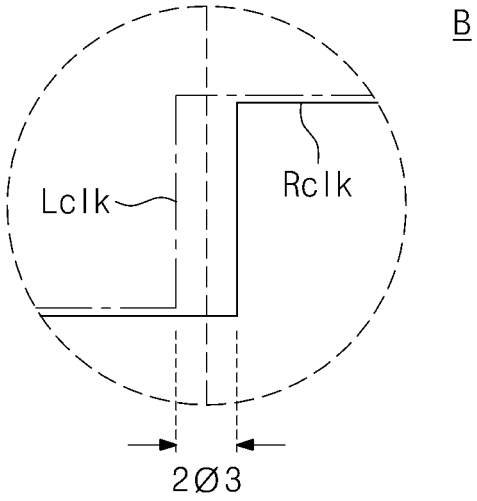


FIG. 6

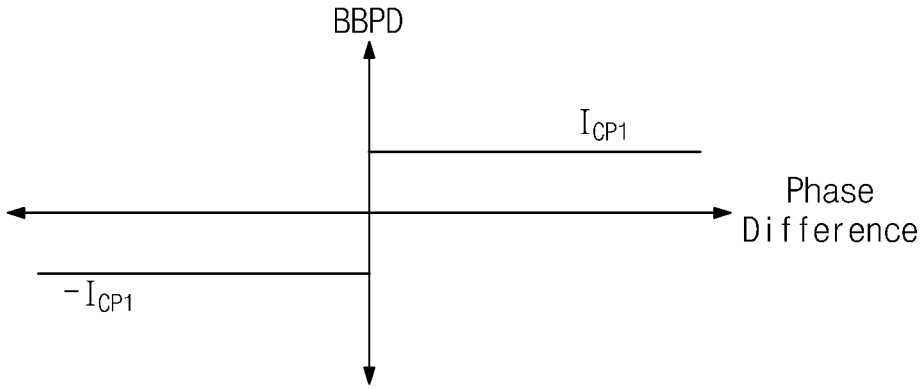

BBPD
I_{CP1}
Phase
Difference
$-I_{CP1}$

FIG. 7

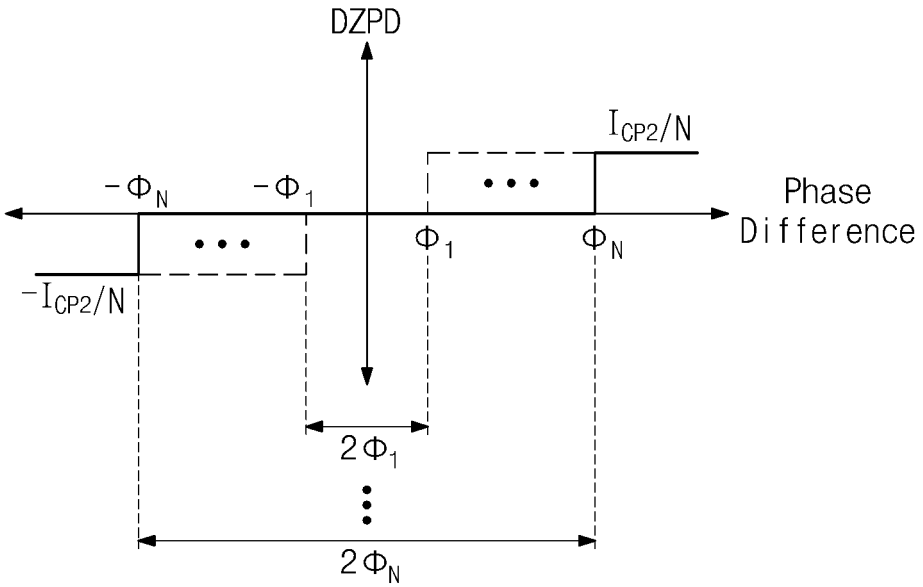

DZPD
$I_{CP2/N}$
$-\Phi_N$
$-\Phi_1$
Phase
Difference
Φ_1
Φ_N
$-I_{CP2/N}$
$2\Phi_1$
$2\Phi_N$

FIG. 8A

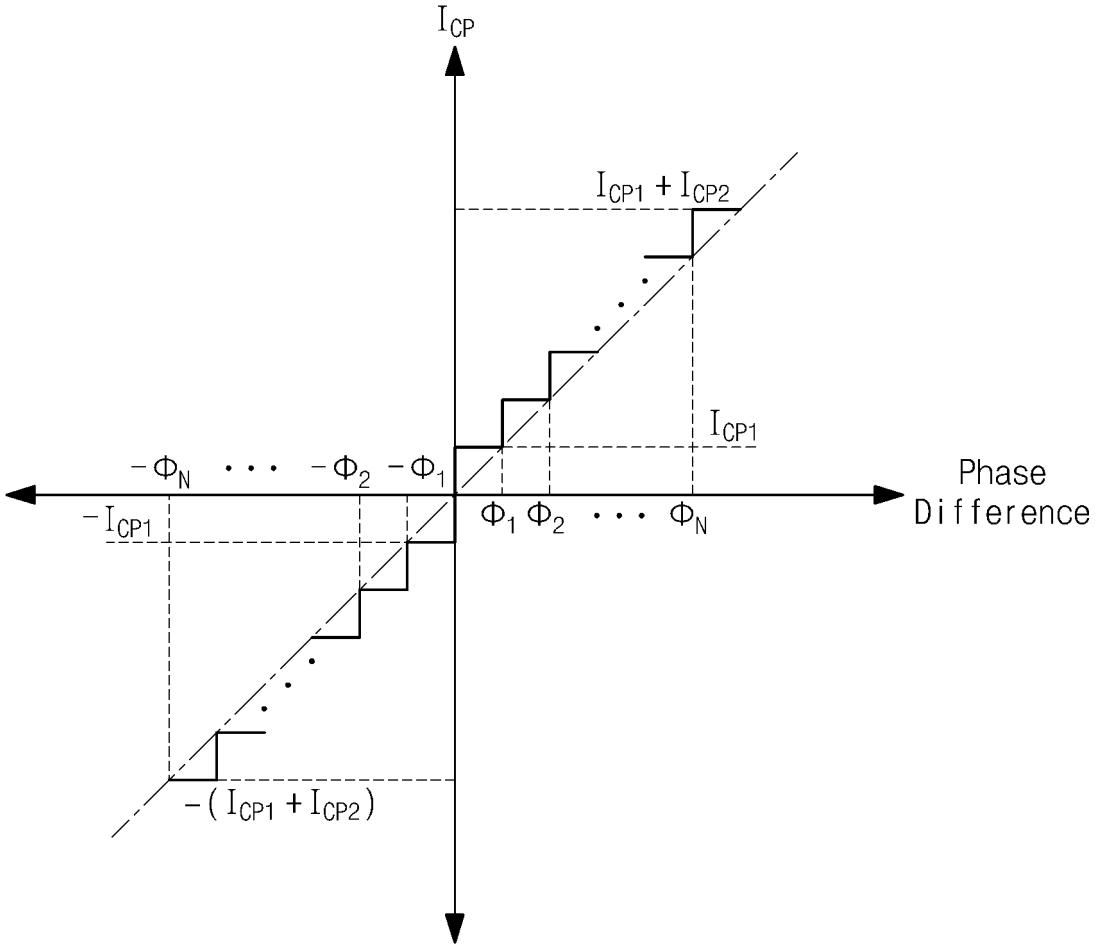

I_{CP}
$I_{CP1} + I_{CP2}$
I_{CP1}
$-\Phi_N \cdots -\Phi_2 -\Phi_1$
$\Phi_1 \Phi_2 \cdots \Phi_N$
Phase Difference
$-I_{CP1}$
$-(I_{CP1} + I_{CP2})$

FIG. 8B

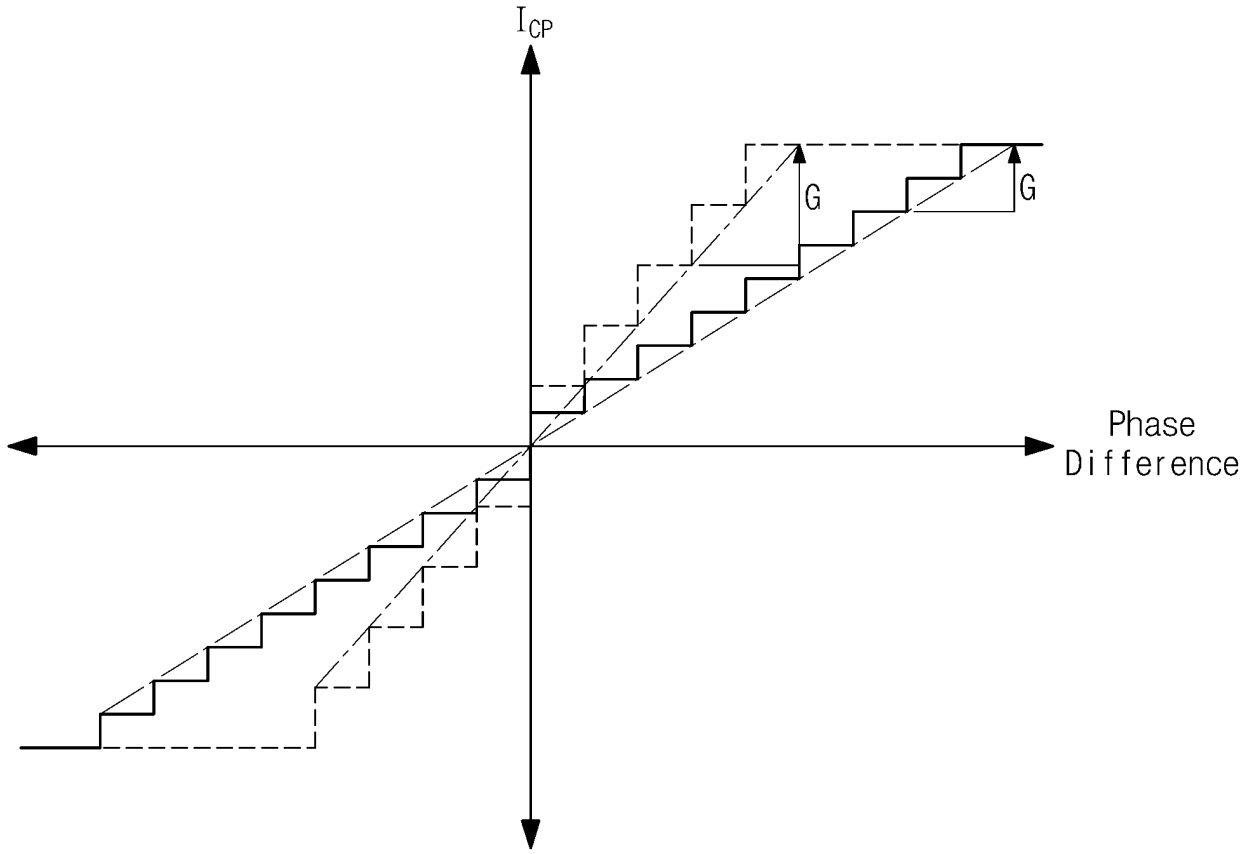


FIG. 8C

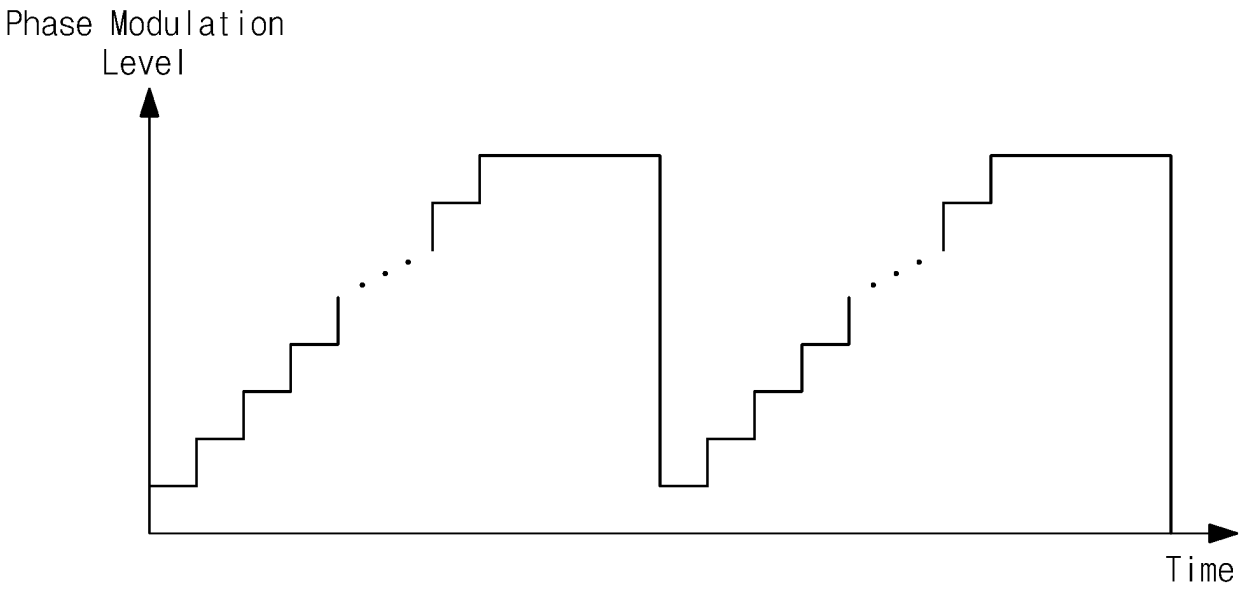


FIG. 8D

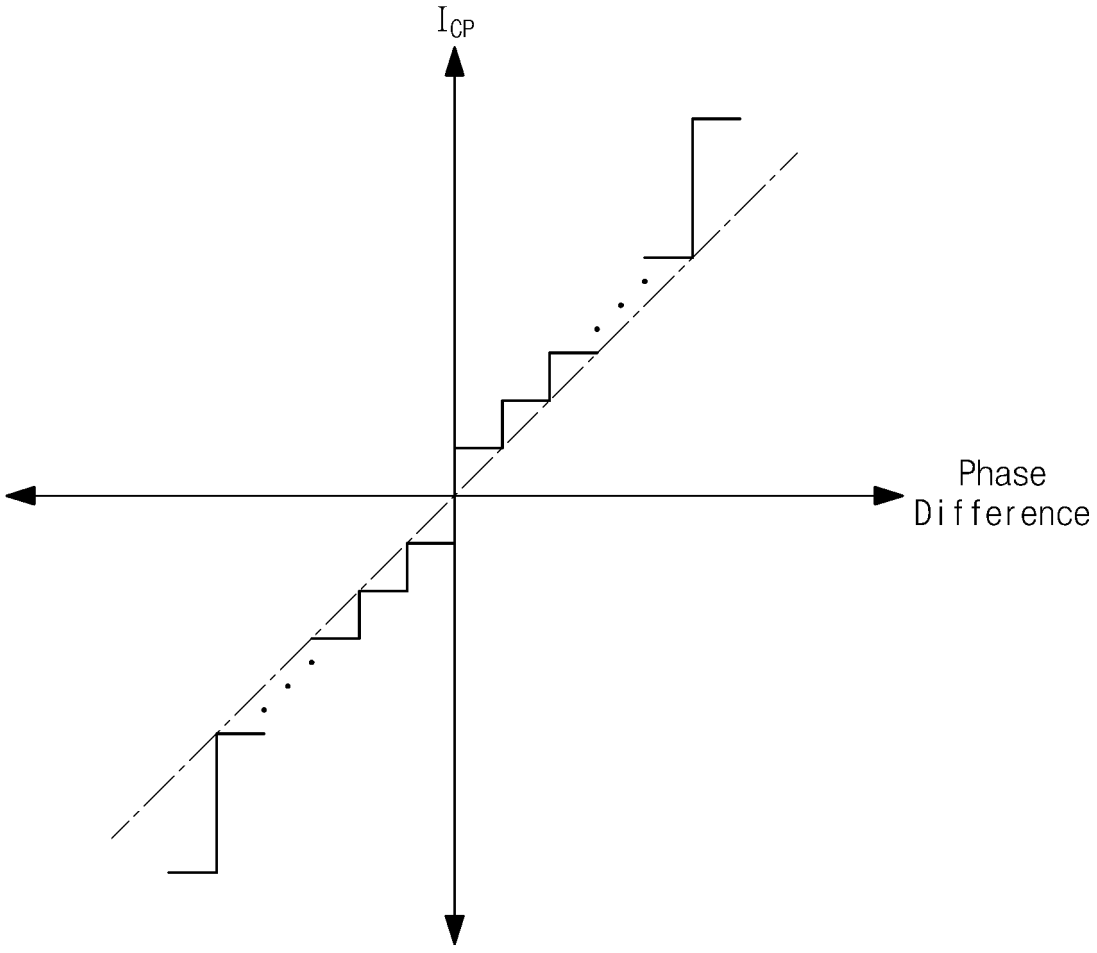


FIG. 9

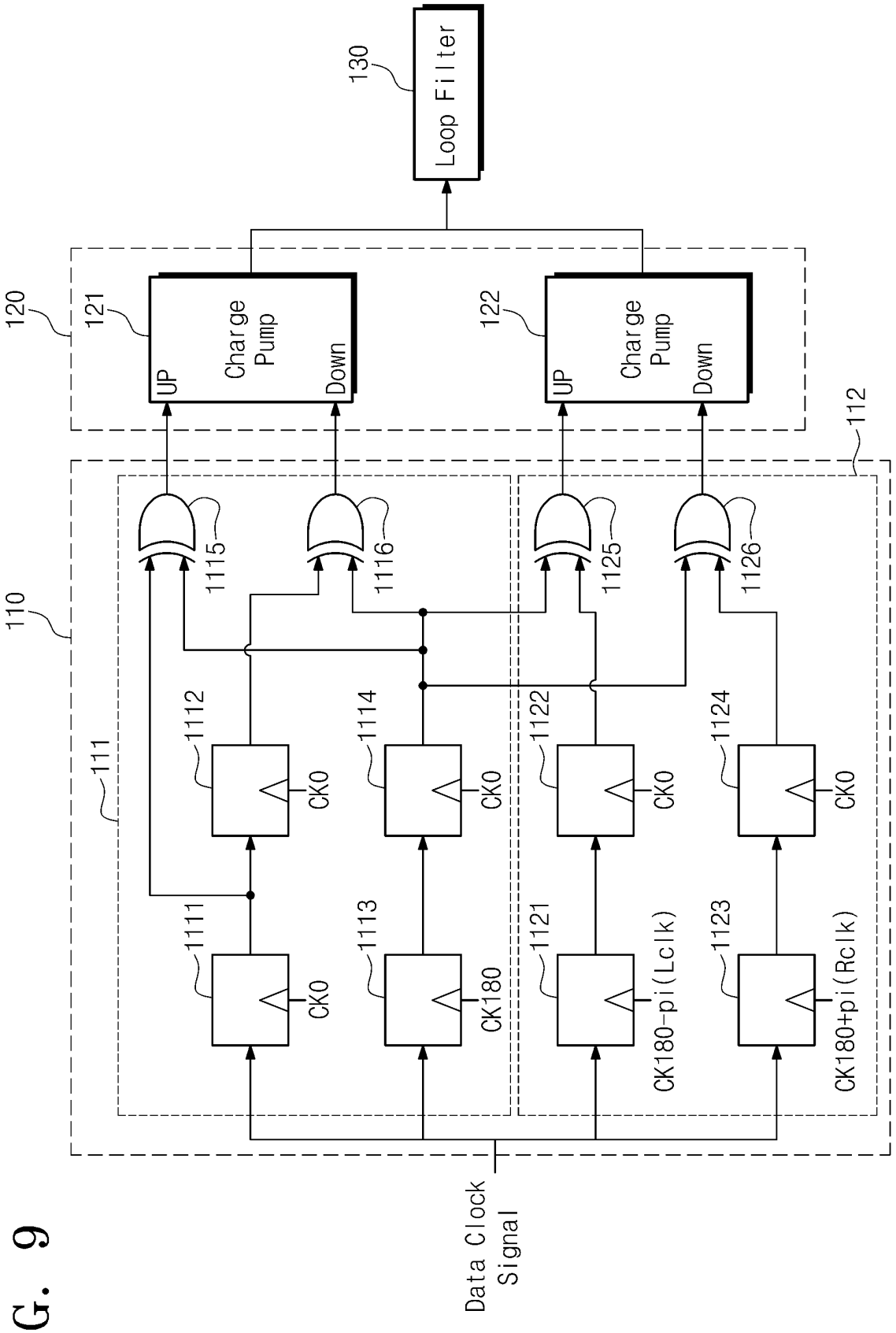

130
Loop Filter
120
121
Charge Pump
UP
Down
122
Charge Pump
UP
Down
112
110
111
1115
1116
1125
1126
1112
1114
1122
1124
CK0
1111
1113
1121
1123
CK180
CK180-pi(Lclk)
CK180+pi(Rclk)
Data Clock Signal

FIG. 10

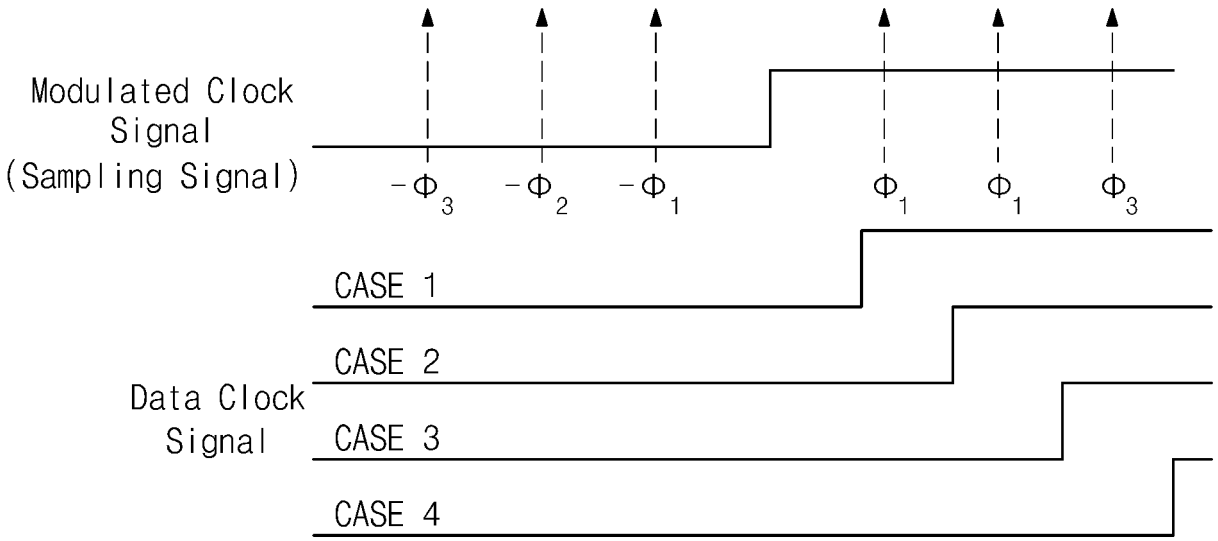

Modulated Clock Signal (Sampling Signal)
$-\Phi_3$
$-\Phi_2$
$-\Phi_1$
Φ_1
Φ_1
Φ_3
Data Clock Signal
CASE 1
CASE 2
CASE 3
CASE 4

FIG. 11

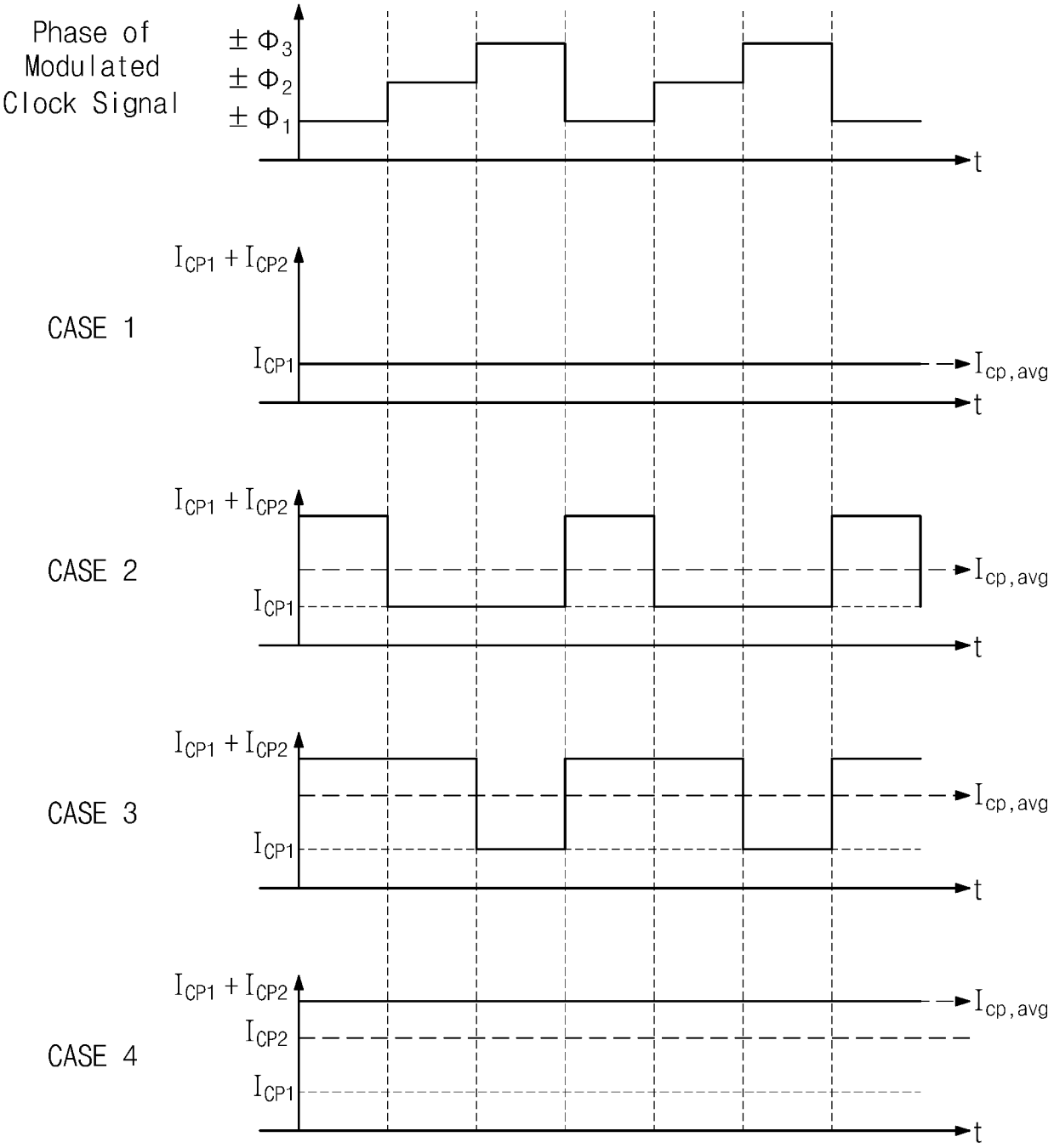
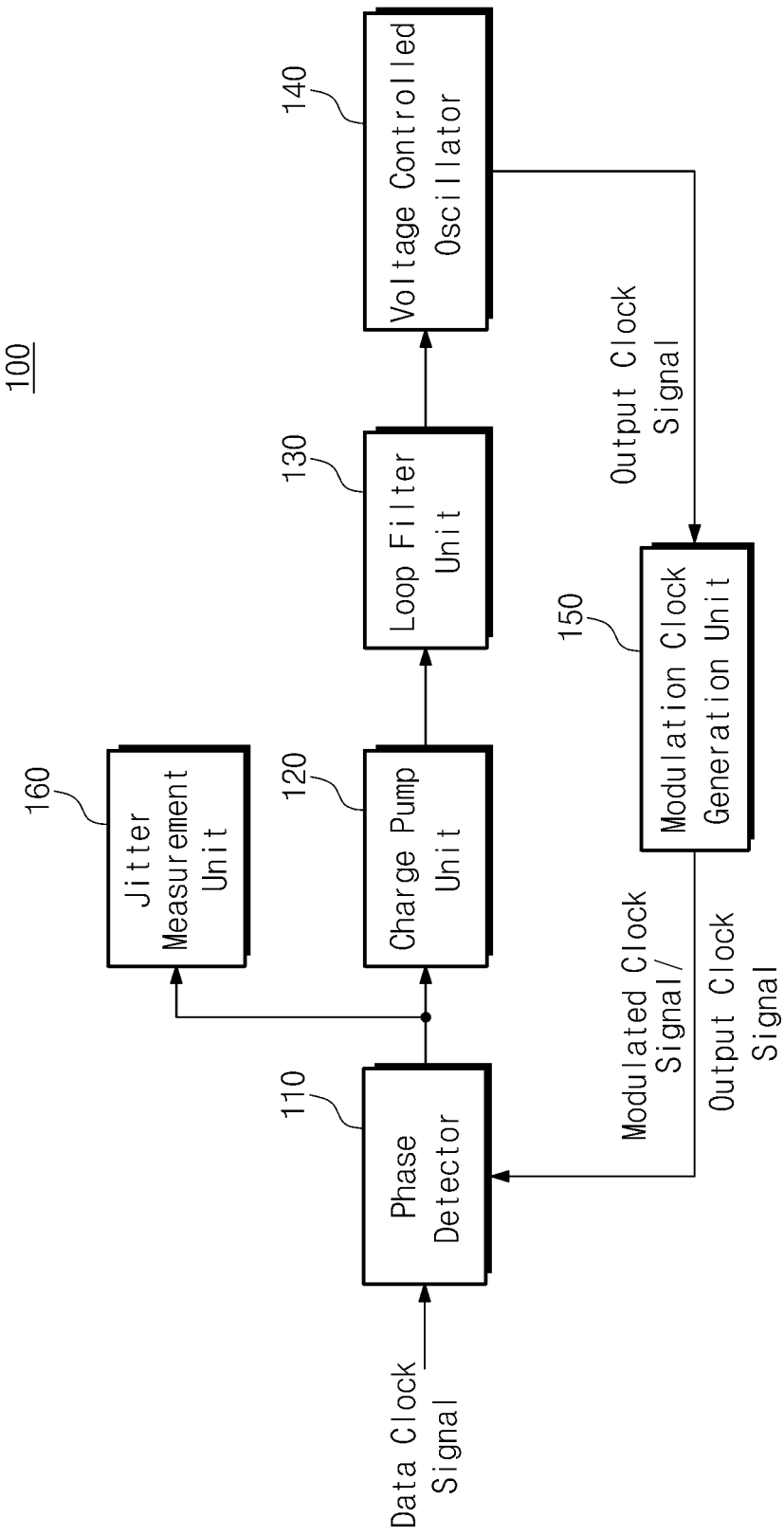

Phase of Modulated Clock Signal
± Φ3
± Φ2
± Φ1
t
CASE 1
ICP1 + ICP2
ICP1
Icp,avg
t
CASE 2
ICP1 + ICP2
ICP1
Icp,avg
t
CASE 3
ICP1 + ICP2
ICP1
Icp,avg
t
CASE 4
ICP1 + ICP2
ICP2
ICP1
Icp,avg
t

FIG. 12A


100
Data Clock Signal
110
Phase Detector
120
Charge Pump Unit
130
Loop Filter Unit
140
Voltage Controlled Oscillator
150
Modulation Clock Generation Unit
160
Jitter Measurement Unit
Modulated Clock Signal/ Output Clock Signal
Output Clock Signal

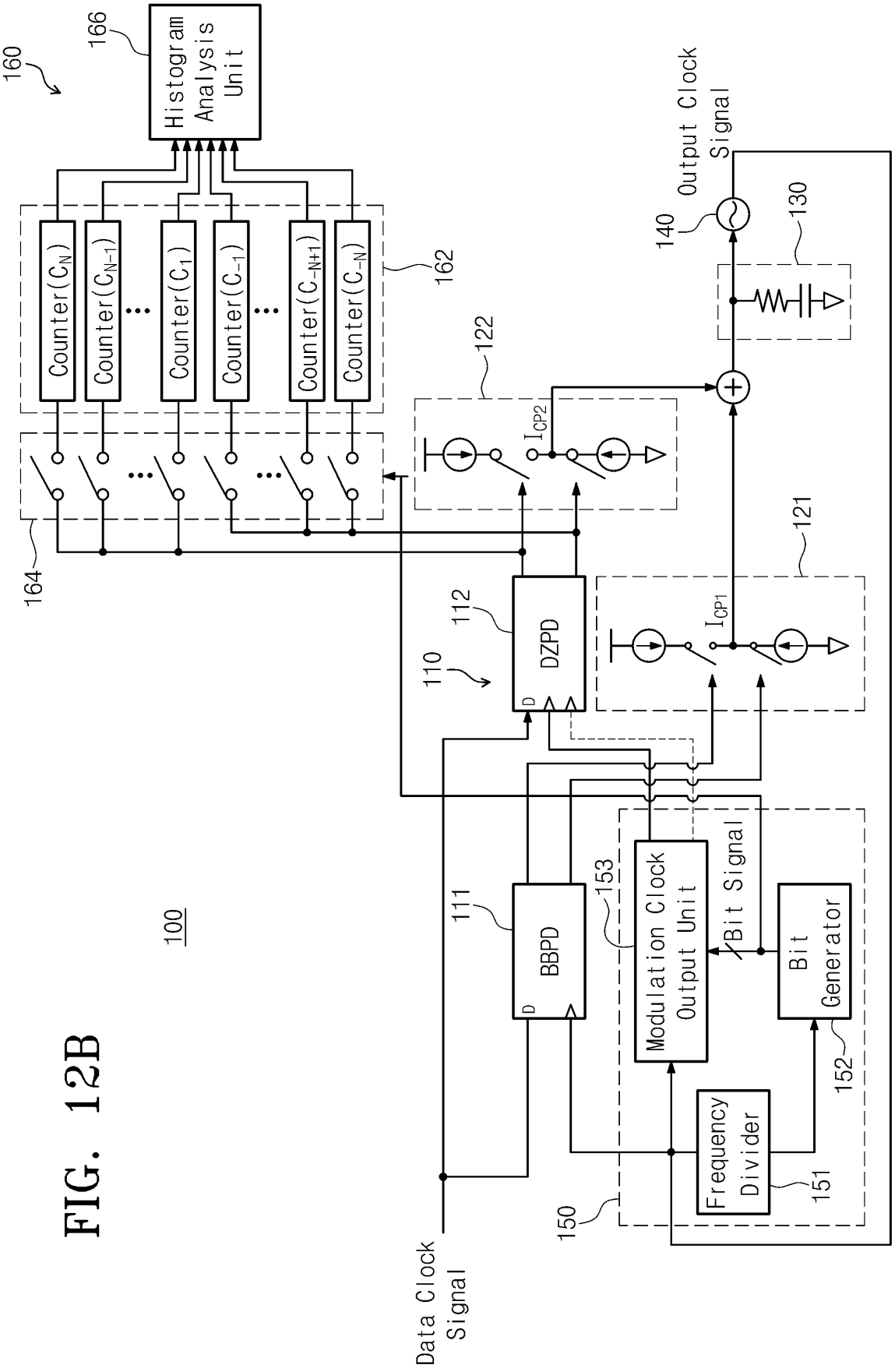

160
166
Histogram Analysis Unit
Counter(C_N)
Counter(C_{N-1})
Counter(C_1)
Counter(C_{-1})
Counter(C_{-N+1})
Counter(C_{-N})
162
164
122
I_{CP2}
140
Output Clock Signal
130
121
I_{CP1}
112
DZPD
110
111
BBPD
153
Modulation Clock Output Unit
Bit Signal
Bit Generator
152
Frequency Divider
151
150
Data Clock Signal
100

FIG. 12B

FIG. 13A

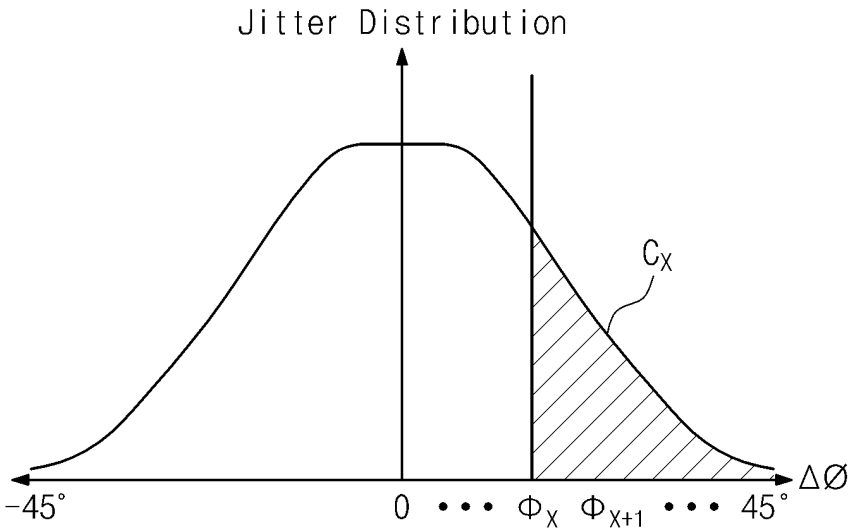


FIG. 13B

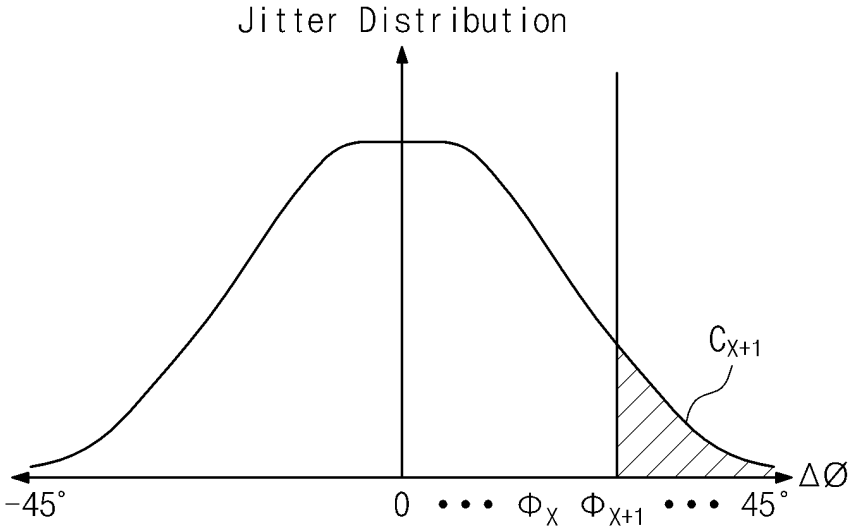


FIG. 13C

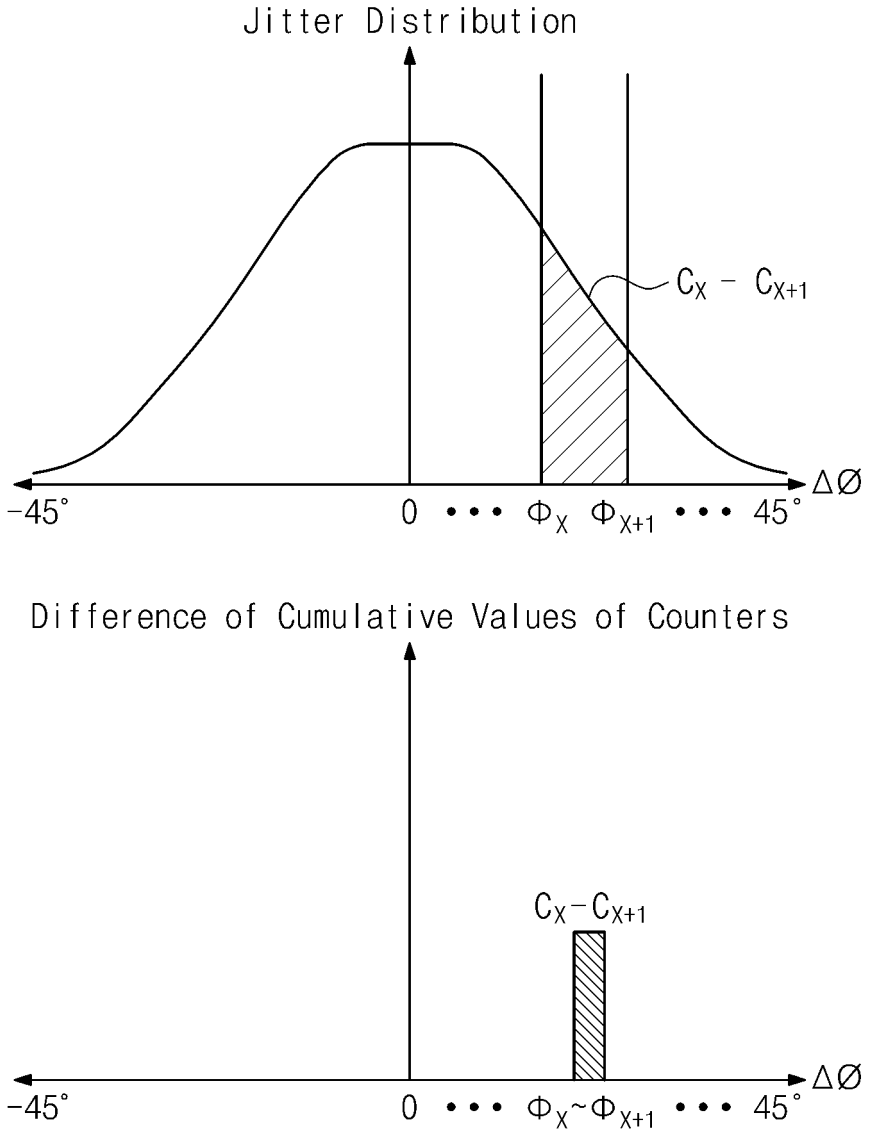
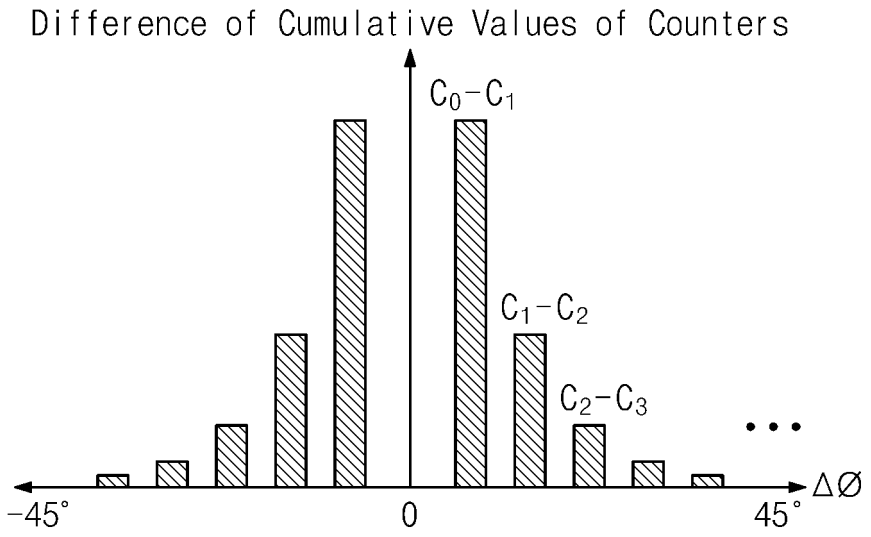

Jitter Distribution
$C_X - C_{X+1}$
ΔØ
-45°
0 ••• Φ_X Φ_{X+1} ••• 45°
Difference of Cumulative Values of Counters
$C_X - C_{X+1}$
ΔØ
-45°
0 ••• $\Phi_X \sim \Phi_{X+1}$ ••• 45°

FIG. 14


Difference of Cumulative Values of Counters
C0-C1
C1-C2
C2-C3
...
ΔØ
-45°
0
45°

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2013108001 A1 **[0002]**
- US 2002126867 A1 **[0002]**