Silicon Avalanche Photodetectors Fabricated With Standard CMOS/BiCMOS Technology

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Silicon Avalanche Photodetectors Fabricated With Standard CMOS/BiCMOS Technology

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Abstract

Silicon Avalanche Photodetectors Fabricated With Standard CMOS/BiCMOS Technology

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High-performance silicon avalanche photodetectors (APDs) are designed and fabricated with standard complementary metal-oxide-semiconductor (CMOS) technology and bipolar CMOS (BiCMOS) technology without any design or layout rule violation. To investigate the performance of CMOS-compatible silicon APDs (CMOS-APDs), DC and AC characteristics of the CMOS-APDs are experimentally characterized. In addition, equivalent circuit models for CMOS-APDs are developed to better understand CMOS-APD characteristics.

CMOS-APDs are investigated with several considerations such as guard ring (GR), electrode, silicide, area, and junction for the goal of

identifying the factors that influence the CMOS-APD performance and achieving the optimal CMOS-APD performance. Several types of CMOS-APDs are realized with the considerations, and current characteristics, responsivity, avalanche gain, electrical reflection coefficients, and photodetection bandwidth for CMOS-APDs are measured and compared. In addition, their characteristics are analyzed with technology computer-aided-design (TCAD) simulation and the equivalent circuit models. From these investigations, dominant factors that influence the CMOS-APD performances are identified, and then the CMOS-APD is optimized. The optimized CMOS-APD shows the highest gain and photodetection bandwidth performances among CMOS-compatible photodetectors reported until now.

Then, with the optimized CMOS-APD, their characteristics are measured and compared at different bias voltages and incident optical power with the goal of achieving the optimal operating conditions. The characteristics depending on the reverse bias voltage and incident optical power are analyzed with equivalent circuit models, and consequently dominant limiting factors that influence the performances of CMOS-APDs are identified, and then the optimal operating conditions are clarified.

From these investigations, dominant factors that influence the

CMOS-APD performances are identified, and then the optimal operating conditions are clarified. It is expected that the optimized CMOS-APDs can play an important role in silicon-photonics applications to achieve cost reduction of systems by enabling monolithic electronic-photonic integrated circuits based on the mature CMOS technology. In addition, the equivalent-circuit analysis can be very useful for realizing and understanding monolithically integrated optical receivers having germanium avalanche photodetectors as well as silicon avalanche photodetectors.

Keywords: Avalanche gain, avalanche photodetector (APD), avalanche photodiode, edge breakdown, equivalent circuit model, guard ring, inductive-peaking effect, optical interconnect, optical receiver, optoelectronics, photodetector, photodetection bandwidth, photodiode, photogenerated-carrier transit time, responsivity, rf peaking, shallow trench isolation (STI), silicide, silicon avalanche photodetector, silicon photodiode, silicon photonics, standard CMOS technology

1. Introduction

1-1. Silicon Photonics for High-Speed Interconnects

The data transmission requirements for many interconnect applications are continuously increasing. Existing electrical interconnects, however, face severe problems due to their link length limitation as well as increasing cross-talk noise and power consumption [1], [2]. As a solution for this problem, optical interconnect technology has been vigorously investigated. However, as of yet, it is difficult to replace electrical interconnects with optical interconnects in many applications since optical components are relatively expensive and bulky [2], [3]. Consequently, the development of cost-effective and compact optical components is essential for the adoption of optical interconnect technology. Fig. 1-1 shows current status and future prospects for electrical and optical interconnect applications.

Recently, silicon photonics has been actively investigated for optical rack-to-rack, board-to-board, and chip-to-chip interconnects because silicon photonics can provide a low-cost solution for high-speed interconnects [4]–[6]. In addition, if integration of silicon photonic components with silicon electronic circuits becomes possible, it can

bring remarkable advantages in system performance, cost, power, and size [1], [4]. Such an expectation is especially high for monolithic electronic-photonic integrated circuits (EPICs) based on complementary metal-oxide-semiconductor (CMOS) or bipolar CMOS (BiCMOS) technology as CMOS is the dominant platform for most integrated circuits [3]–[8]. Fig. 1-2 shows a conceptual diagram of silicon photonics.

In order to realize the EPICs for optical interconnects, implementation of high-speed and high-responsivity photodetectors is required. Germanium-based photodetectors have been investigated due to their large absorption coefficient at 1.3-μm and 1.5-μm wavelengths as well as compatibility with CMOS technology [9]–[11]. Another interesting approach is using standard CMOS/BiCMOS technology without any modifications for 850-nm photodetector realization. Although such CMOS-compatible photodetectors (CMOS-PDs) suffer from limitations of non-optimal device structures, they have advantages of low fabrication cost and high volume manufacturability. A high-performance CMOS-PD monolithically integrated with CMOS circuits can immediately provide very cost-effective solutions for many optical interconnect applications. The fact that there exist cheap 850-nm optical transmission systems based on vertical-cavity surface-emitting

lasers (VCSELs) and multi-mode fibers certainly helps in justifying this approach.

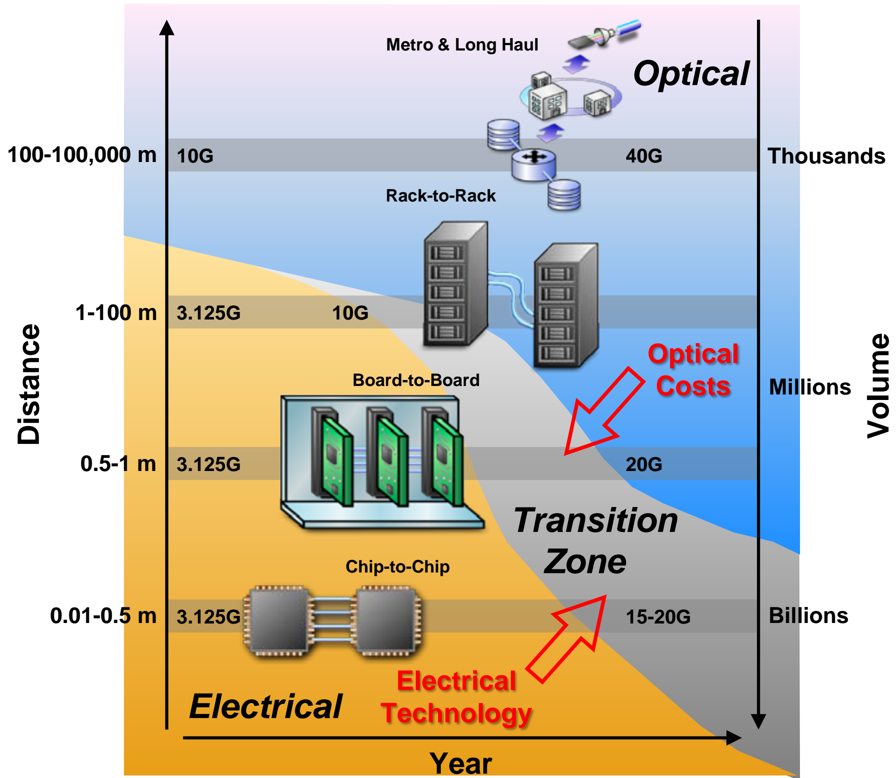


Fig. 1-1. Current status and future prospects for electrical and optical interconnects.

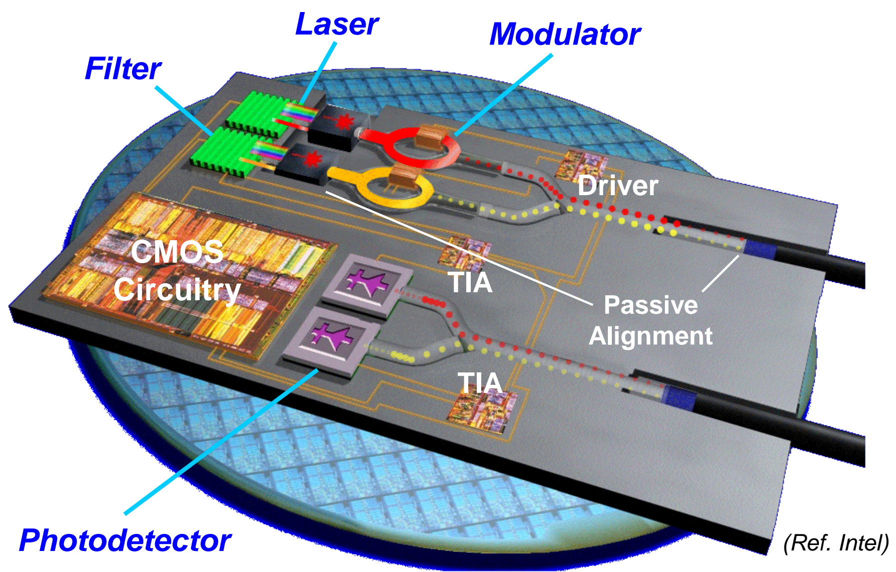


Fig. 1-2. Conceptual diagram of silicon photonics.

1-2. Silicon Photodetectors in Standard CMOS/BiCMOS Technology

The structure of a photodetector is basically a PN junction, and standard CMOS/BiCMOS technology can provide several types of PN junctions that can detect 850-nm light. Of course, such photodetectors cannot escape limitations due to non-optimal device structures provided by standard silicon technology. But if their performances can be improved to a reasonable level with a careful selection of device structure and optimization of device performance, they can immediately provide very cost-effective solutions for many applications.

Several approaches have been tried to improve the bandwidth-efficiency product of CMOS-PDs, because they have the inherent disadvantage of low bandwidth-efficiency product due to the low absorption coefficient of silicon and the narrow depletion regions caused by high doping concentrations in standard CMOS technology. To improve the photodetection bandwidth performance, a lateral PIN photodetector implemented by a P^+/P-substrate/N^+ interleaved structure was proposed [12]. The photodetector has photodetection bandwidth of 1.9 GHz, but it has weakness of relatively low responsivity. As another

approach of enhancing the photodetector bandwidth, spatially-modulated photodetectors (SMPDs) have been reported [13]–[15]. The SMPDs show enhanced photodetection bandwidth, but they suffer from low responsivity. A photodetector formed by multiple p^{+}-p-n structure in standard CMOS technology was reported, which provides high responsivity with the large depletion region and avalanche gain [16]. However, it has disadvantages of relatively high dark currents, low avalanche gain, and limited bandwidth. Based on the same structure, bandwidth enhancement was achieved with elimination of slow diffusion photogenerated carriers by body biasing [17]. Although bandwidth can be enhanced with this approach, responsivity is severely reduced owing to the decreased depletion region of N-well/P-substrate junction and reduced diffusion currents from P-substrate.

High-performance CMOS-compatible avalanche photodetectors (CMOS-APDs) fabricated with standard CMOS/BiCMOS technology have been previously reported [18]–[21]. Specifically, the CMOS-APDs are based on P^{+}/N-well or N^{+}/P-well junction, which provides higher photodetection bandwidth without slow photogenerated diffusion currents in the P-substrate region. In addition, photodetection responsivity can be greatly enhanced by large avalanche gain.

2. Photodetectors in Standard CMOS/BiCMOS Technology

2-1. Characteristics of CMOS/BiCMOS Technology for Photodetectors

There are inherent limitations of standard CMOS technology for photodetector applications. Fig. 2-1 shows the simplified cross section of typical twin-well CMOS transistors. N-channel metal–oxide–semiconductor field-effect transistor (NMOSFET) is formed by N^+ source/drain regions on P-well, and P-channel MOSFET (PMOSFET) is formed by P^+ source/drain regions on N-well with gate oxides and poly-silicon gates. With these, PN junctions necessary for photodetectors can be realized with N-well/P-substrate, N^+/P-well, or P^+/N-well junctions. These PN junctions are, however, formed within about 1.5 μm below the surface, and their depletion lengths are not large enough to completely absorb 850-nm light due to high doping concentration in standard CMOS technology, which has the optical penetration depth over 10 μm in silicon [22]. Fig. 2-2 shows the simplified band diagram for the N-well/P-substrate junction. 850-nm light penetrates deep into the silicon substrate, resulting in reduction of

responsivity due to recombination of photogenerated carriers in charge-neutral regions. Furthermore, those photogenerated carriers contributing to photocurrents have to diffuse through charge-neutral regions, which significantly limit the photodetection frequency response.

Fig. 2-3 shows the cross section of heterojunction bipolar transistors (HBTs) of standard SiGe BiCMOS technology [23], in which PN junctions for photodetectors can be implemented by P^+ SiGe Base/Collector and Base/Deep Collector junctions. For optical injection into the junctions, emitter regions can be excluded in the fabrication process. These PN junctions are also formed nearby the surface, resulting responsivity and bandwidth reductions at the 850-nm wavelength.

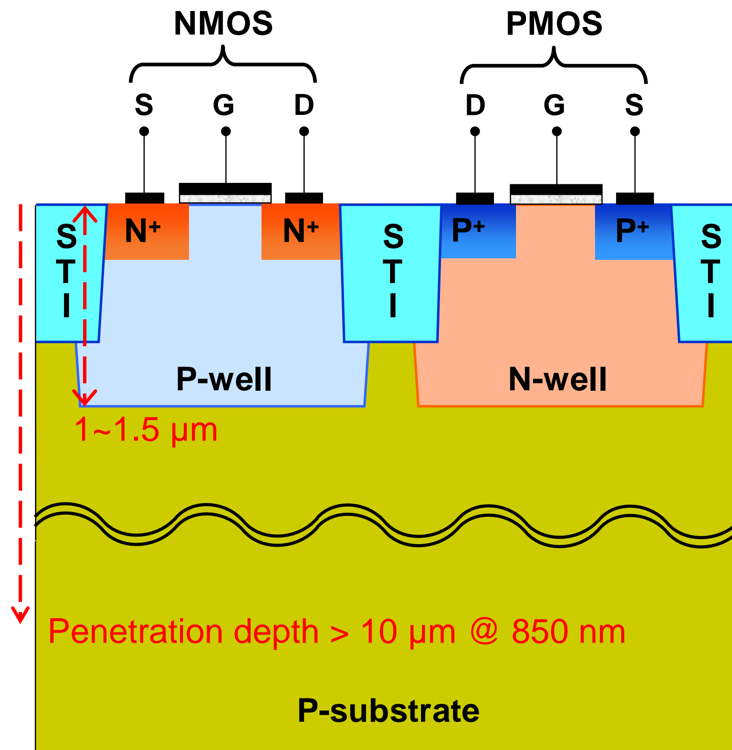


Fig. 2-1. Simplified cross section of typical twin-well CMOS transistors.

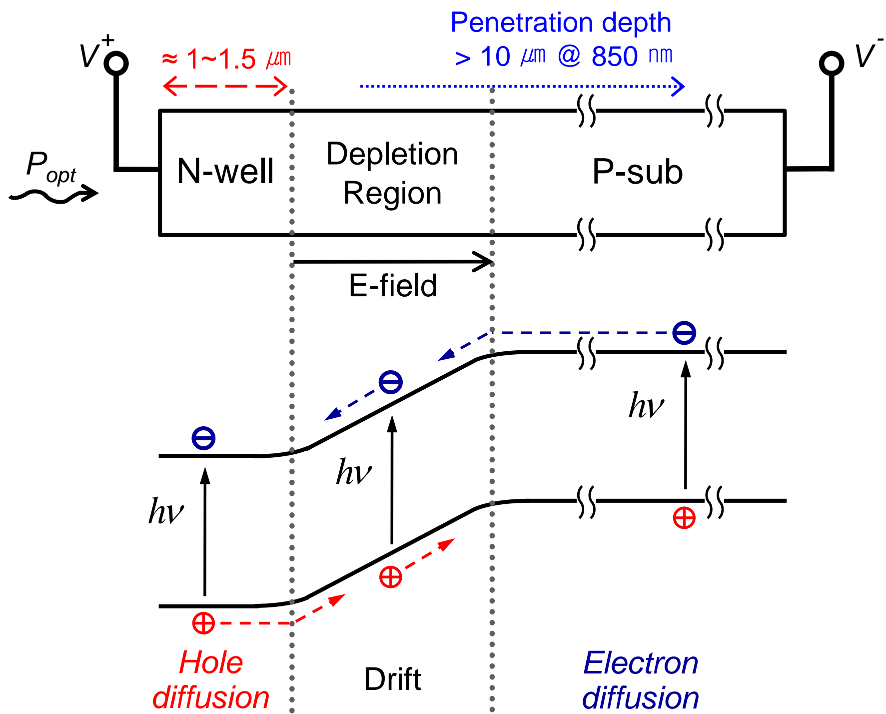


Fig. 2-2. Simplified band diagram for the N-well/P-substrate junction.

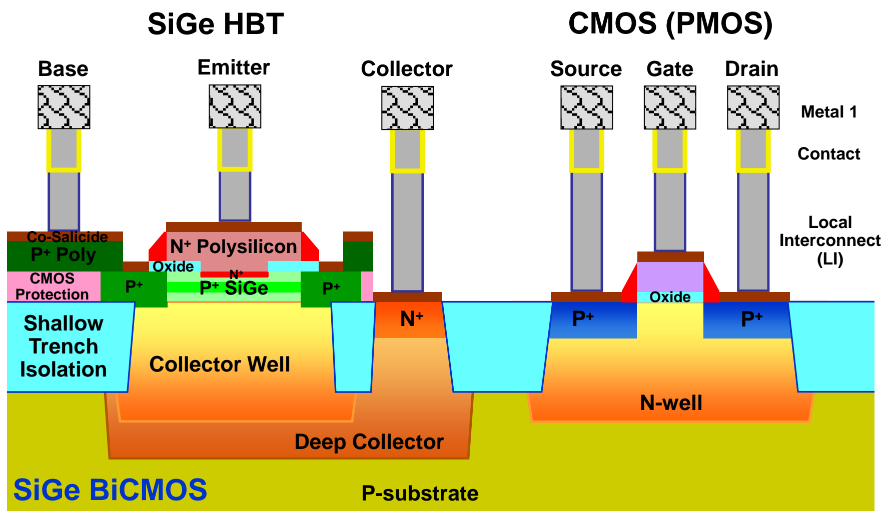


Fig. 2-3. Simplified cross section of standard SiGe BiCMOS technology.

2-2. Silicon Photodetectors in Standard CMOS Technology

The simplest way of realizing a photodetector with standard CMOS technology is using N-well/P-substrate junction as shown in Fig. 2-4(a). It can provide wider depletion regions and, consequently, better detection efficiency than any other PN junctions available in standard CMOS technology. However, this type of photodetector has very slow photodetection bandwidth in the MHz range [20], [24], and does not allow any high-speed applications. This is because many photons are absorbed in the region where photogenerated carriers experience slow diffusive transport.

With SMPDs, the photodetection bandwidth can be enhanced by excluding the slow diffusion components of the photodetectors [13]–[15]. As shown in Fig. 2-4(b), SMPDs are generally composed of a row of photodetectors alternatively covered and uncovered with light blocking materials, such as metal layers. Differential signaling is used to subtract slow diffusion components of covered region from those of uncovered region, resulting in high photodetection bandwidth. However, the SMPDs have a weakness of very low responsivity

because of the covered region and subtracted slow diffusion components.

Another approach is using a lateral PIN structure, where P^+/P-substrate/N^+ regions are interleaved as shown in Fig. 2-4(c) [12]. The photodetector is surrounded by N-well and Deep N-well (DNW) regions, and photogenerated carriers created in the lateral depletion regions contribute to photocurrents. The PIN photodetector has photodetection bandwidth of 1.9 GHz, but it also has a drawback of relatively low responsivity.

Another approach of enhancing photodetector bandwidth is using P^+/N-well junction, with which slow diffusion currents in P-substrate can be excluded. However, this structure suffers from reduced detection efficiency simply because the detection area is much reduced. This problem can be solved by using the avalanche gain. The structure of the CMOS-APD is shown in Fig. 2-4(d) [18]. Consequently, the CMOS-APD based on the P^+/N-well junction has photodetection bandwidth of several GHz, and it has high detection efficiency due to the avalanche gain.

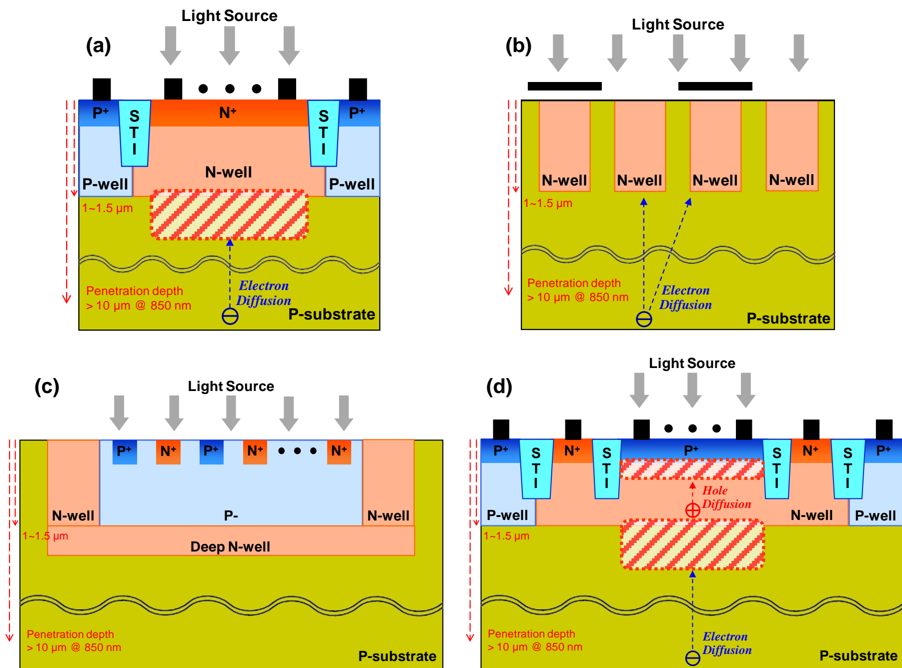


Fig. 2-4. Cross sections of silicon photodetectors: (a) N-well/P-substrate, (b) spatially-modulated, (c) lateral PIN, and (d) P^{+}/N-well photodetectors.

3. Characteristics of the Silicon APD Based on the P^+/N-well Junction

3-1. Device Description

Fig. 3-1 shows the silicon-APD structure based on the P^+/N-well junction. It can be fabricated with standard CMOS/BiCMOS technology without any design or layout rule violation. Shallow trench isolation (STI), which is generally used on standard CMOS technology to prevent current leakage between adjacent components and isolate each device and formed by depositing dielectric materials such as silicon dioxide into the shallow trench, is inserted as a guard ring between P^+ and N^+ regions since it provides a high uniform electric field profile without premature edge breakdown, resulting in high responsivity [21]. For optical-window formation, the self-aligned silicide (salicide) process, which is commonly implemented in CMOS technology for ohmic contacts, is blocked. In order to implement the CMOS-APD, two PN junctions, which are P^+/N-well and N-well/P-substrate junctions, are formed. The CMOS-APD has large photocurrents using the two PN junctions, but it has low photodetection bandwidth performance due to carrier diffusion process in the P-

substrate region. Consequently, to use only the upper PN junction, P^+/N-well, photocurrents are extracted from the P^+ port located in the N-well region so that slow diffusion currents generated in the P-substrate can be excluded by potential barrier between P^+ and N-well regions. The P^+/N-well junction is reverse biased with a positive voltage applied to the N-well port, and P^+ is grounded. The P-substrate port is also grounded.

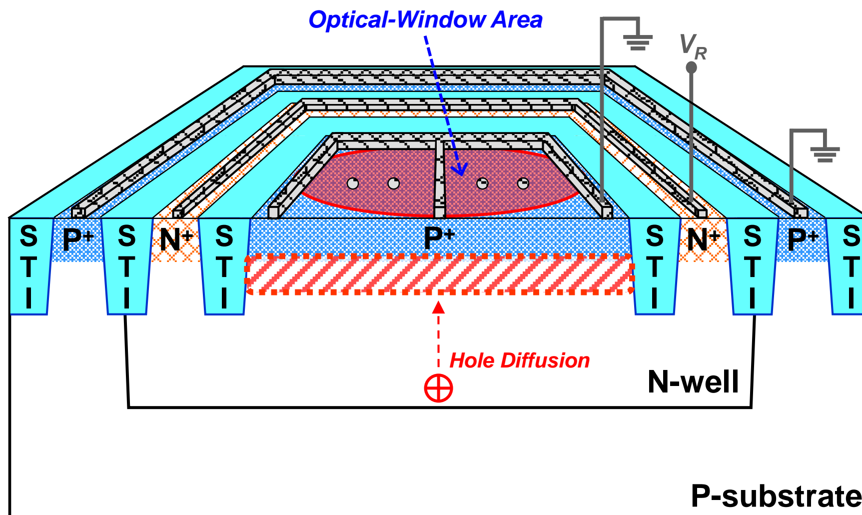


Fig. 3-1. Structure of the P^+/N-well CMOS-APD.

3-2. Experimental Setup

Fig. 3-2 shows experimental setups for CMOS-APD characterization. An 850-nm laser diode and a 20-GHz electro-optic modulator were used as an optical source, and a lensed fiber was used for injecting light into photodetectors. Incident optical power was controlled by an 850-nm optical attenuator, and the bias voltage was applied using a semiconductor parameter analyzer (Agilent 4145B). For measurements of photodetection frequency responses, a S-parameter vector network analyzer (VNA; Agilent 8719ES) was used to modulate optical signals (Port 1) and detect output signals (Port 2) of the CMOS-APDs with prior calibration of cables and RF adaptors as shown in Fig. 3-2(a). To investigate impedance characteristics of the CMOS-APDs, two-port S-parameters were measured with the VNA as shown in Fig. 3-2(b). The frequency range was from 50 MHz to 13.5 GHz for the photodetection frequency responses and S-parameters, and all measurements were done on-wafer at room temperature.

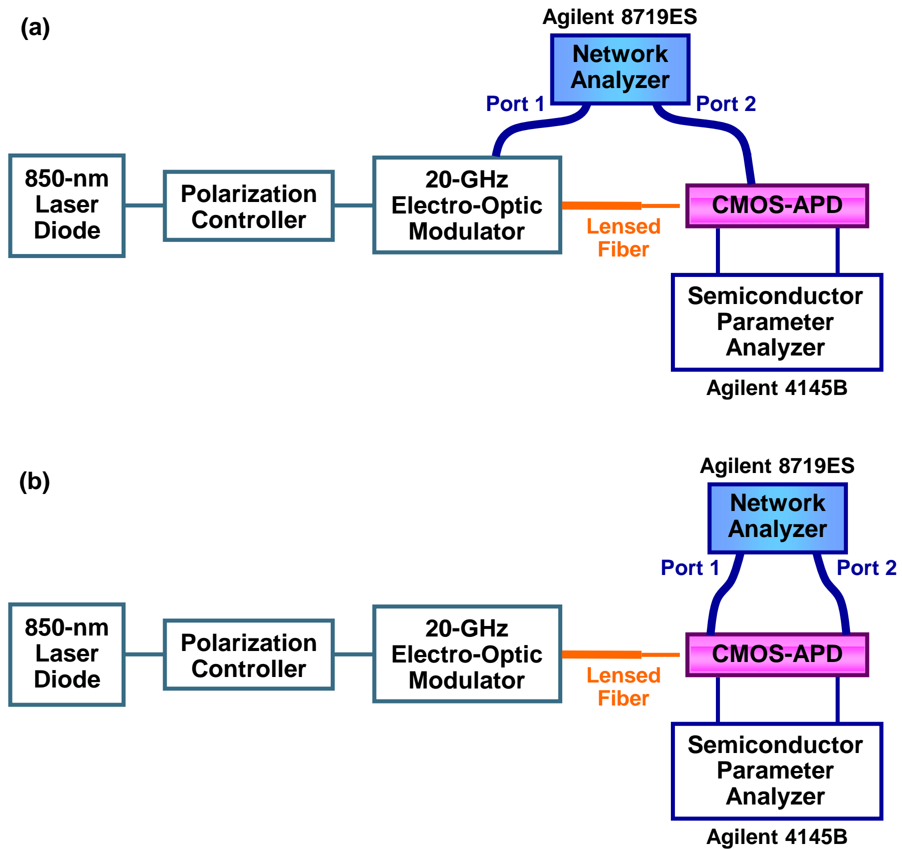


Fig. 3-2. Experimental setups for CMOS-APD characterization: (a) DC characteristic and photodetection frequency response and (b) S-parameter measurements.

3-3. DC Characteristics

3-3-1. Current-Voltage Characteristic

For the measurements, a CMOS-APD based on the P^+/N-well junction was fabricated with 0.25-μm standard BiCMOS technology, and the incident optical power was 1 mW. Fig. 3-3 shows measured current-voltage characteristics of the CMOS-APD under illumination and dark conditions. Currents obtained from the N^+ port in N-well is larger than from the P^+ port in N-well due to the currents from the N-well/P-substrate junction. When the reverse bias voltage is small, the CMOS-APD has low photogenerated currents of about 13 μA and 340 μA at the P^+ port and N^+ port, respectively, and it exhibits low dark currents below a few nA. With the reverse bias voltage approaching the avalanche breakdown voltage, the photogenerated currents start to increase dramatically with internal gain provided by the avalanche multiplication process. When the reverse bias voltage is larger than the breakdown voltage, the currents are saturated due to the series resistance and the space-charge effect [25]. The avalanche breakdown voltage can be defined as the voltage at which the dark current reaches 10 μA [9], [10], and, with this definition, the avalanche breakdown

voltage of the CMOS-APD is about 12.5 V. Fig. 3-4 shows measured dark current characteristics of the CMOS-APDs with six randomly selected chips. The range of the breakdown-voltage distribution is about 0.4 V because of the fabrication-process variation.

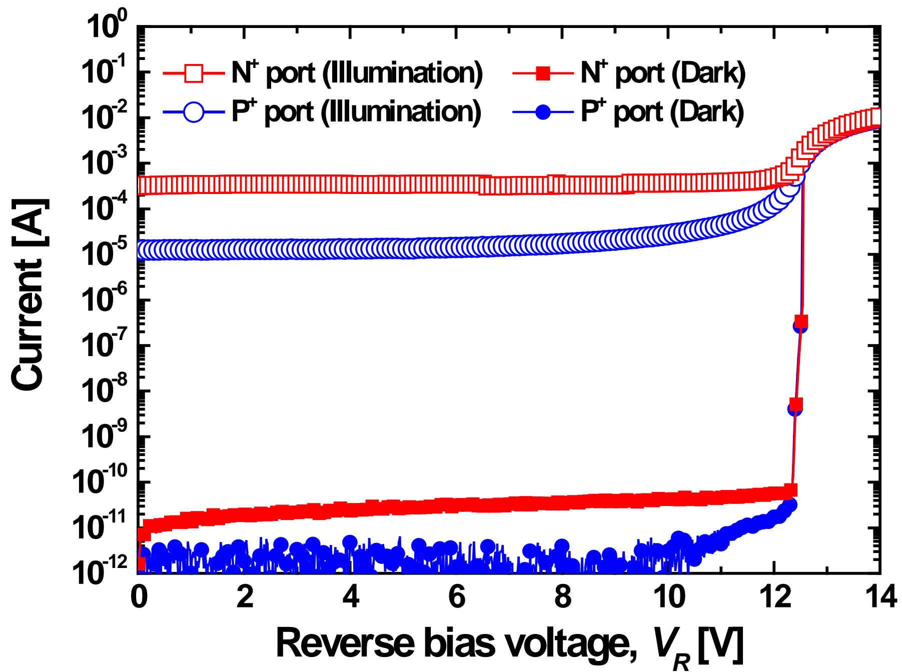


Fig. 3-3. Current-voltage characteristics of the CMOS-APD at P^+ port and N^+ port in N-well under illumination and dark conditions. The incident optical power is 1 mW.

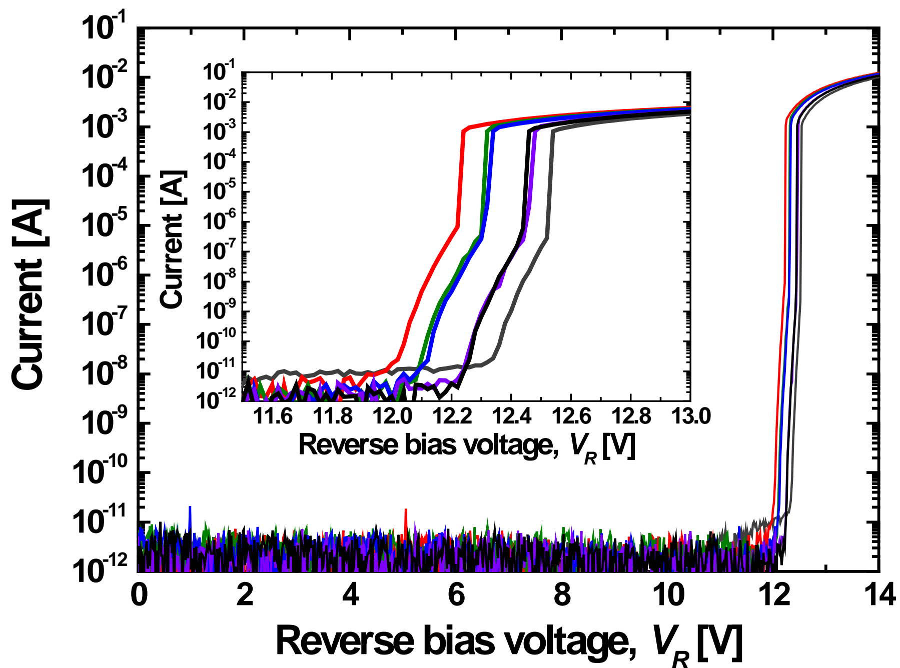


Fig. 3-4. Current-voltage characteristics of the CMOS-APDs at P^+ port on different chips under the dark condition.

3-3-2. Responsivity and Avalanche Gain

From the measured current-voltage characteristics, responsivity and avalanche gain of the CMOS-APD were calculated, and the results are shown in Fig. 3-5. The photocurrent is defined by subtracting the dark current from the photogenerated current, and responsivity is defined as the photocurrent per incident optical power. In APDs, the avalanche gain, avalanche multiplication factor, is the key parameter representing internal amplification of photogenerated carriers, and it is determined by the ratio of photocurrents between a given bias voltage and the reference voltage, where avalanche gain is insignificant. With increasing the reverse bias voltage, responsivities dramatically increase at the avalanche regime owing to the avalanche multiplication process. The maximum avalanche gain obtained from the N^+ port is lower than the P^+ port, because the photogenerated currents are saturated due to the series resistance and the space-charge effect. With further increase in the reverse bias voltage beyond the peak avalanche gain voltage, the avalanche gains rapidly go down with rapid increase in dark currents.

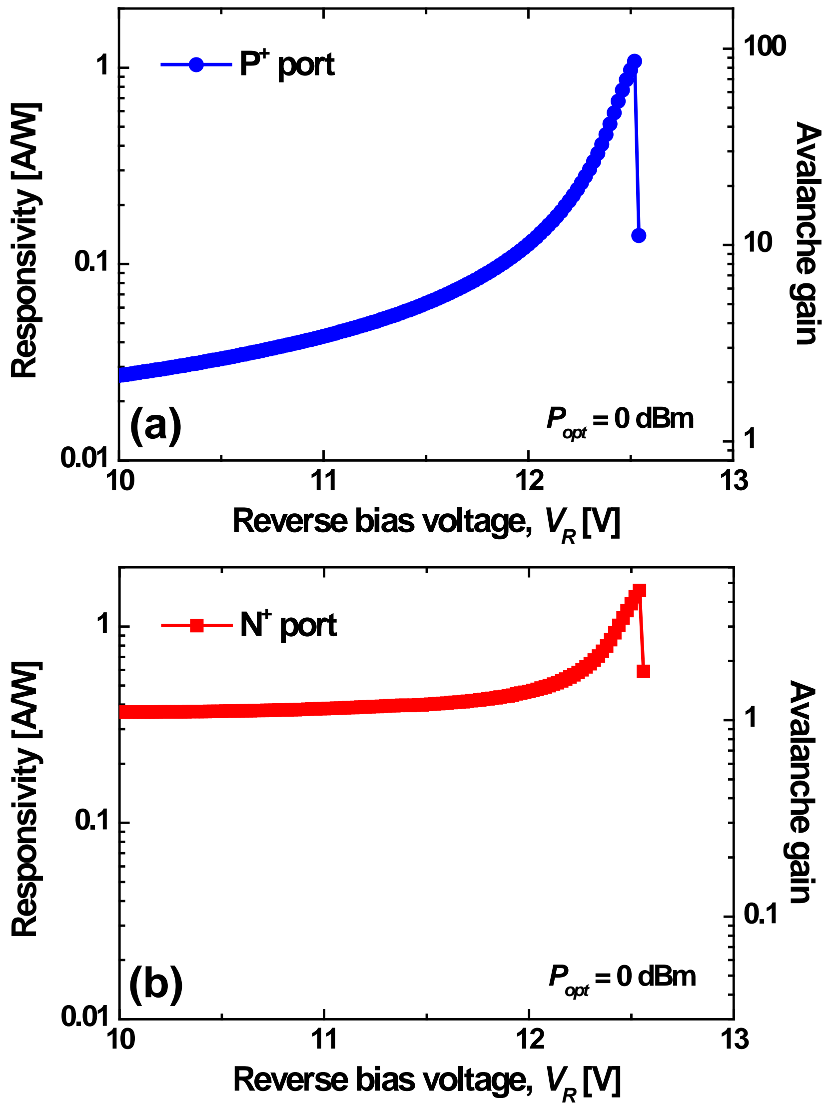


Fig. 3-5. Responsivity and avalanche gain of the CMOS-APD at (a) P^+ port and (b) N^+ port in N-well as a function of the reverse bias voltage. The incident optical power is 1 mW.

3-4. AC Characteristics

3-4-1. Photodetection Frequency Response

Fig. 3-6(a) shows photodetection frequency responses of the CMOS-APD at P^+ port and N^+ port at the reverse bias voltage of 12.3 V. As explained above, the response obtained from the N^+ port shows higher response than the P^+ port because photogenerated carriers are collected by both P^+/N-well and N-well/P-substrate junctions, but its photodetection bandwidth is lower due to slow diffusion currents from the N-well/P-substrate junction. Therefore, it is desirable to use the P^+ port for high-speed operation.

Fig. 3-6(b) shows photodetection frequency responses of the CMOS-APD at different bias voltages. As the reverse bias voltage is increased, the photodetection frequency response increases due to the increased avalanche gain but goes down when the reverse bias voltage exceeds the optimal condition, 12.3 V. Peaking in the response can be observed, especially with a large reverse bias voltage, which is due to the inductive component produced in the avalanche regime.

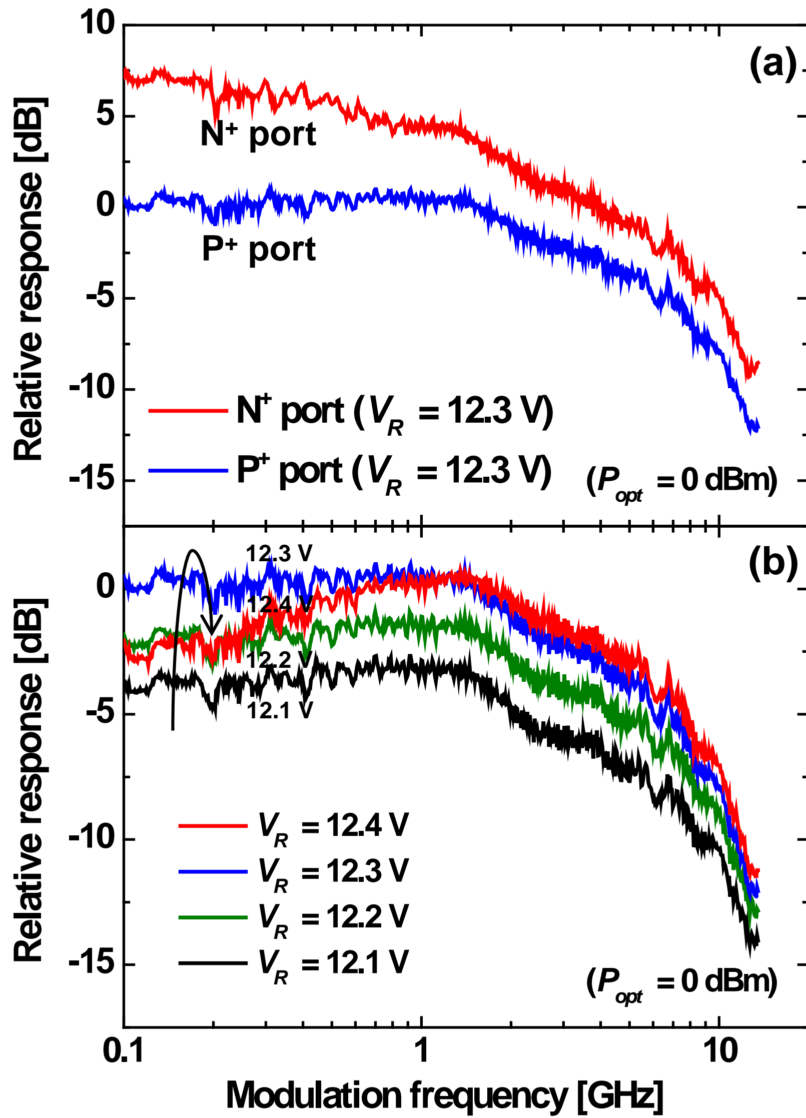


Fig. 3-6. Photodetection frequency responses of the CMOS-APD (a) at P^+ port and N^+ port in N-well at the reverse bias voltage of 12.3 V and (b) at P^+ port in N-well at different bias voltages. The incident optical power is 1 mW.

3-4-2. Electrical Reflection Coefficient

To investigate the impedance characteristics of the CMOS-APD, electrical reflection coefficients of the CMOS-APD at the P^+ port were measured at different bias voltages, and the results are shown in Fig. 3-7. At the reverse bias voltage of 12.1 V, the CMOS-APD has only capacitive and resistive components. As the reverse bias voltage is increased, however, the CMOS-APD has the inductive component, which is designated by the upper part of Smith chart. The inductive component causes resonance resulting in peaking in photodetection frequency response as can be seen in Fig. 3-6. From this measurement, it is clearly verified that the CMOS-APD has the inductive component, and the physical origin will be discussed in the next chapter, in which the inductive component as well as the impedance characteristics of the CMOS-APD will be investigated with an equivalent circuit model.

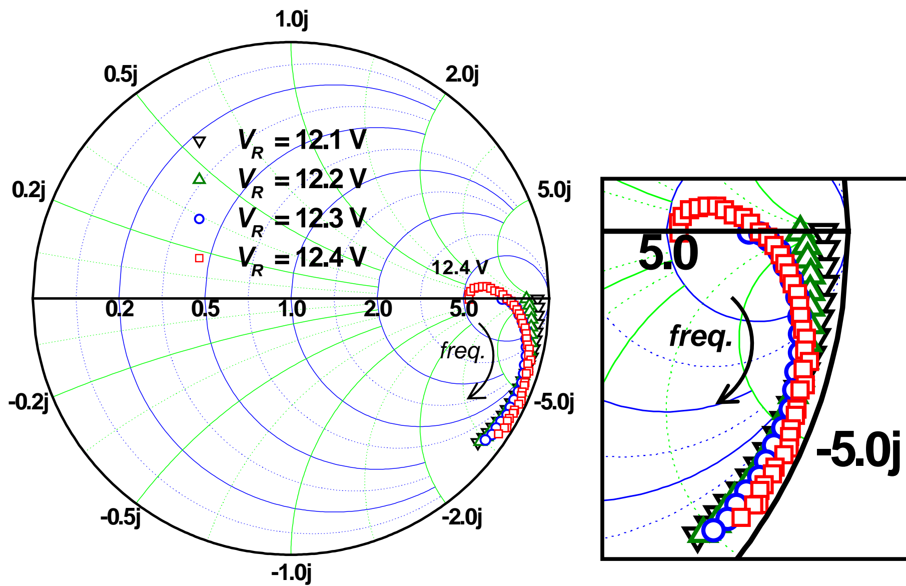


Fig. 3-7. Electrical reflection coefficients of the CMOS-APD at P^+ port from 50 MHz to 13.5 GHz at different bias voltages. The inset shows magnified images of the reflection coefficients.

4. Equivalent Circuit Model for Silicon APDs

4-1. Equivalent Circuit Model

To better understand CMOS-APD characteristics, an equivalent circuit model for CMOS-APDs is derived. Fig. 4-1 shows the equivalent circuit model used for this investigation, which is a simplified version of that reported in [26]. An inductor with a series resistor, a resistor, and a capacitor in parallel are used for modeling the APD core. Inductance, L_a, represents phase delay between currents and voltages due to impact ionization [27]. Series resistance, R_a, accounts for the finite reverse saturation current and the field-dependent velocity [27]. R_l and C are resistance and capacitance of the depletion region, respectively. R_{nw} and C_{sub} represent N-well resistance and N-well/P-substrate junction capacitance, respectively. C_p is parasitic capacitance between N^+ and P^+ electrodes, and Z_{pad} represents the equivalent circuit for pads and metal interconnects with details shown in the inset in Fig. 4-1.

The photodetection frequency response is also affected by the transit time of photogenerated carriers. For photodetectors fabricated with standard CMOS technology, this is dominated by diffusion of

photogenerated carriers in charge-neutral regions, which in the CMOS-APD correspondence to hole diffusion in the charge neutral N-well as shown in Fig. 3-1. The influence of transit time is modeled in the equivalent circuit with a current source having a single-pole frequency response, where f_{tr} represents the 3-dB bandwidth limited by hole-diffusion transit time [28].

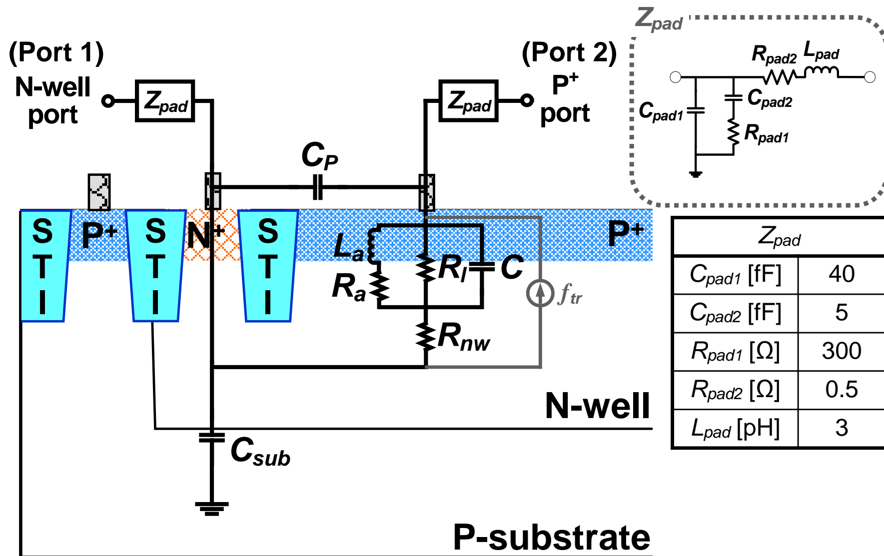


Fig. 4-1. Equivalent circuit model for CMOS-APDs.

4-2. Parameter-Extraction Process for the Equivalent Circuit Model

The parameter values for the equivalent-circuit elements are extracted from two-port S-parameter measurements. Advanced Design System (ADS) by Agilent Technology is used for the S-parameter extraction. First, Y-parameters and Z-parameters are calculated from the measured S-parameters, and open and short test patterns are used for extracting Z_{pad} parameters. The extracted parameters are listed in Fig. 4-1. Then, C_{sub} is extracted by Z_{12}, and other parameters are extracted by $Z_{22} - Z_{12}$ through a fitting process. The frequency-dependent current source is not included during this extraction and fitting process since it does not influence the values of passive circuit elements in the small-signal analysis. For fitting, initial guesses are made from theoretical equations and then manually refined [26]. The inset of Fig. 4-2 shows electrical reflection coefficients at P^+ port on Smith chart from 50 MHz to 13.5 GHz for the CMOS-APD, which is characterized in chapter 3, at the reverse bias voltage of 12.3 V and incident optical power of 1 mW, from measurement and simulation with extracted parameter values, which are listed in Table 4-1. The f_{tr} value for the frequency-dependent current source is determined by

fitting the simulated photodetection frequency response to the measurement result. Fig. 4-2 shows normalized measured and simulated photodetection frequency responses for the CMOS-APD at the same conditions. Both measurement and simulation results using the equivalent circuit model show good agreement in reflection coefficients and photodetection frequency responses.

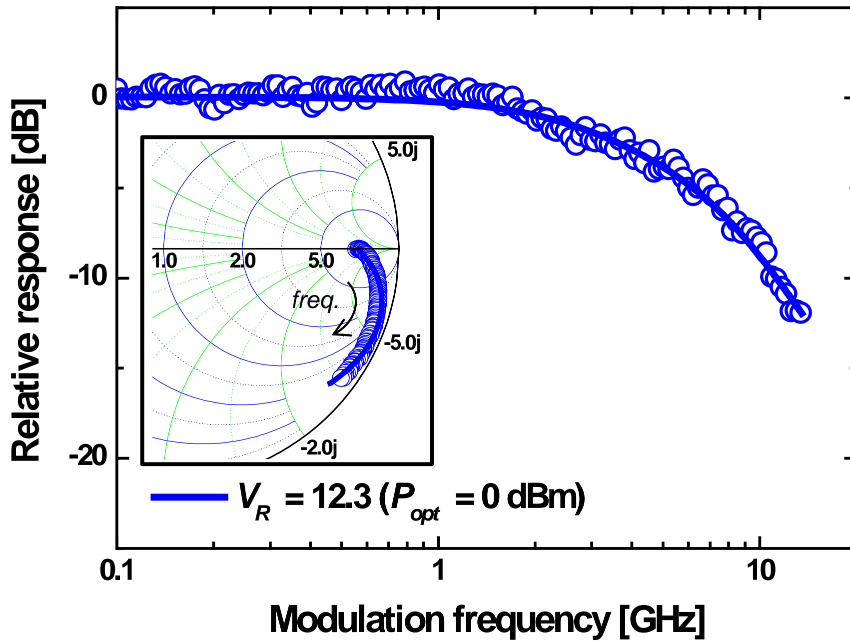


Fig. 4-2. Measured and simulated photodetection frequency responses of the CMOS-APD at the reverse bias voltage of 12.3 V and incident optical power of 1 mW. The inset shows measured and simulated electrical reflection coefficients of the CMOS-APD at the same conditions. Hollow circles represent measured data, and solid lines represent simulated results.

Table 4-1

EXTRACTED PARAMETERS FOR THE CMOS-APD
AT THE REVERSE BIAS VOLTAGE OF 12.3 V
AND INCIDENT OPTICAL POWER OF 1 mW

CMOS-APD	
L_a [nH]	15
R_l [kΩ]	5
C [fF]	21
R_{nw} [Ω]	500
C_{sub} [fF]	25
C_p [fF]	35
f_{tr} [GHz]	3.5

5. Design Considerations for Silicon-APD-Performance Enhancement

In this section, several design considerations will be investigated for the goal of identifying the factors that influence the CMOS-APD performance and achieving the optimal CMOS-APD performance. The design considerations are guard ring (GR), electrode, silicide, area, and junction. CMOS-APD characteristics will be analyzed for each consideration with measurement results, and from this investigation, dominant factors that influence the CMOS-APD performance will be identified and higher-performance CMOS-APD will be achieved.

5-1. Guard-Ring-Dependent Characteristics

In this section, the effects of various GR structures on the performance of silicon APDs fabricated with standard CMOS/BiCMOS technology will be demonstrated. Four types of CMOS-APDs based on the P^+/N-well junction having different types of GR structures were fabricated, and their electric-field profiles were analyzed with simulation. In addition, such performance parameters as current

characteristics, responsivity, avalanche gain, and photodetection bandwidth were measured and analyzed to identify the optimal GR structure for the CMOS-APD.

5-1-1. Device Structures and Simulation Results

Fig. 5-1 shows cross sections for four types of CMOS-APDs fabricated with 0.25-μm standard BiCMOS technology [23]. Although the technology offers both bipolar and CMOS devices, the APDs were fabricated with CMOS processing steps only. Triple wells including DNW are available in the technology. All four types of CMOS-APDs are based on the P^+/N-well junction, and 10×10-μm^2 optical windows are formed by blocking the salicide process. No design rule is violated for realizing these CMOS-APDs.

The CMOS-APD shown in Fig. 5-1(a) has no GR. GRs between CMOS-APD area and N^+ contacting area can be formed by P-doped regions (Fig. 5-1(b) and (c)) or by STI (Fig. 5-1(d)). In standard CMOS technology, P-type GRs can be formed by P-wells (Fig. 5-1(b)) or by P-substrate (P-sub) areas with blocked P-well and N-well (Fig. 5-1(c)). DNW regions are utilized to isolate GRs from P-sub and to connect N-

wells in the diode and contact regions. The width of the P-well and P-sub GRs is 1.5 μm according to the CMOS design rules. The width of STI GR is 0.7 μm.

Device simulation was performed with MEDICI to investigate the influence of GRs on the electric-field profiles for CMOS-APDs in reverse bias. For the simulation, doping profiles for the 0.25-μm BiCMOS technology were provided by IHP [23]. The doping concentration of P-sub is about 10^{15} cm^{-3}. The P-well and N-well doping ranges from 10^{17} cm^{-3} in the space charge region to about 5×10^{17} cm^{-3} near the surface and at a depth of 0.7 μm. The P^{+}/N-well junction depth is about 0.2 μm. Fig. 5-2 shows the simulated electric-field profiles when CMOS-APDs are reverse biased about 0.1 V below their breakdown conditions. As shown in Fig. 5-2(a), without any GR, the electric fields are much stronger around the edge of the junction than at the planar junction. In APD applications, the uniform and high electric-field profile is desired so that large avalanche gain can be obtained in a large area before the avalanche breakdown occurs. With the field profile shown in Fig. 5-2(a), the avalanche breakdown occurs at the junction edge, preventing photogenerated carriers to experience sufficient avalanche gain. With GRs, this premature edge breakdown is alleviated as shown in Fig. 5-2 (b)–(d). The maximum electric field at

the planar junction increases from 3.9×10^5 V/cm for the device without GR to about 5×10^5 V/cm with P-well or P-sub GR and 5.7×10^5 V/cm with STI GR.

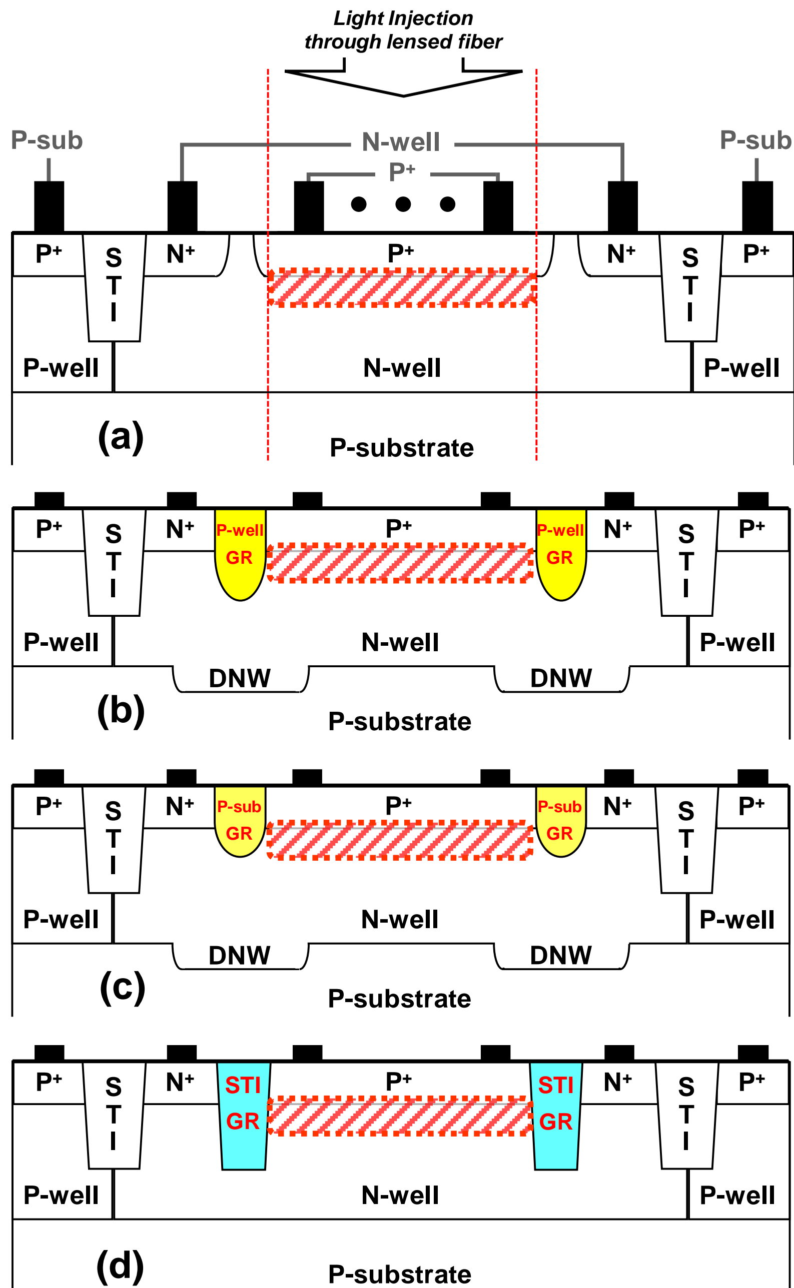


Fig. 5-1. Cross sections of CMOS-APDs: (a) w/o GR, (b) w/ P-well GR, (c) w/ P-sub GR, and (d) w/ STI GR.

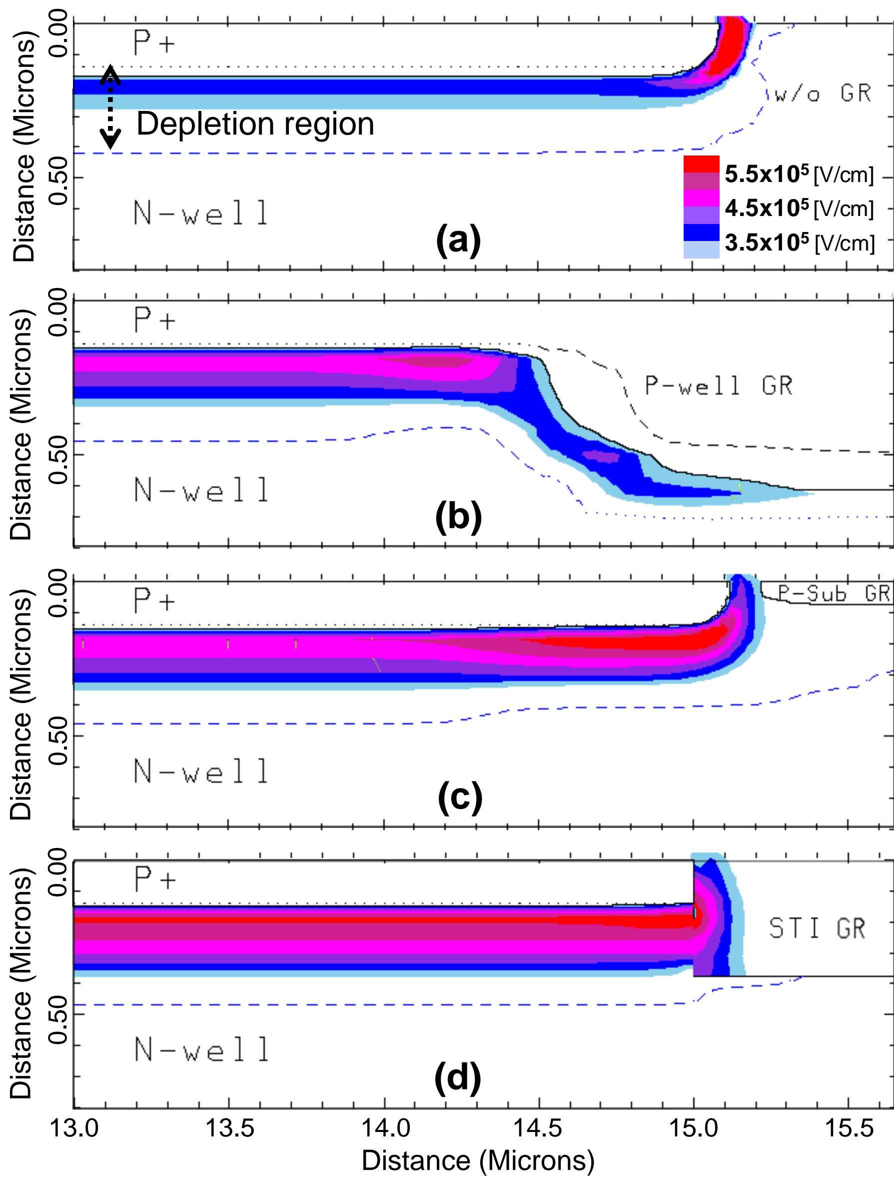


Fig. 5-2. Simulated electric-field profiles for the CMOS-APDs: (a) w/o GR, (b) w/ P-well GR, (c) w/ P-sub GR, and (d) w/ STI GR.

5-1-2. Experimental Results

For DC measurements, 0.1 mW of light measured at the lensed-fiber output was used. Fig. 5-3 shows measured current-voltage characteristics of CMOS-APDs under illumination and dark conditions. Dark currents are below the detection limit of about 5 pA for CMOS-APDs with P-sub GR and STI GR (Fig. 5-3(b)). CMOS-APDs without GR and with P-well GR show enhanced dark currents (Fig. 5-3(a)) due to tunneling at edges of P^+ regions in N-well and N^+ regions in P-well, respectively. These currents disappear when P^+ and N^+ regions are surrounded by lightly-doped P-sub or STI. All CMOS-APDs exhibit low dark currents below a few nA before avalanche breakdown. The avalanche breakdown voltage is defined as the voltage at which the dark current reaches 10 μA. Without GR, the avalanche breakdown voltage is about 9.25 V. However, the breakdown voltages increase to about 10.2 V for P-well and P-sub GRs, and 12.2 V for STI GR. This confirms the simulation results in which STI GR allows the highest electric field before breakdown, resulting in larger maximum gain as shown in Fig. 5-4. The maximum gain is about 2500 with corresponding responsivity of about 15.4 A/W for the device with STI GR while it is about 300 with about 1.9-A/W responsivity for the

device without GR.

Fig. 5-5 shows normalized photodetection frequency responses of CMOS-APDs at the bias voltage about 0.1-V below the breakdown voltages. For this measurement, the average optical power injected into photodetectors was 1 mW. The photodetection bandwidths for all CMOS-APDs are similar because all four devices are based on the same junction structure. CMOS-APDs with P-well and P-sub GR structures have no appreciable difference in the photodetection frequency response and have about 10-dB higher response than the one without GR. The CMOS-APD with STI GR has about 18 dB higher response than the device without GR structures.

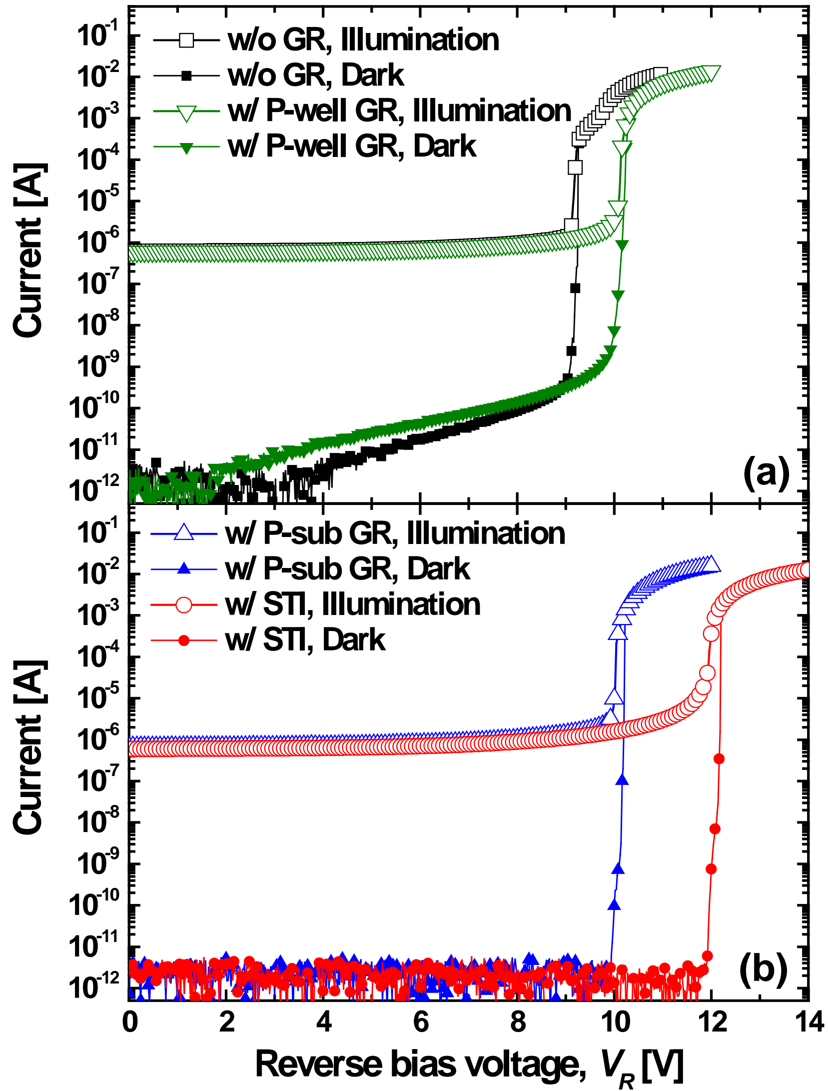


Fig. 5-3. Current-voltage characteristics of the CMOS-APDs: (a) w/o GR and w/ P-well GR, (b) w/ P-sub GR and w/ STI GR.

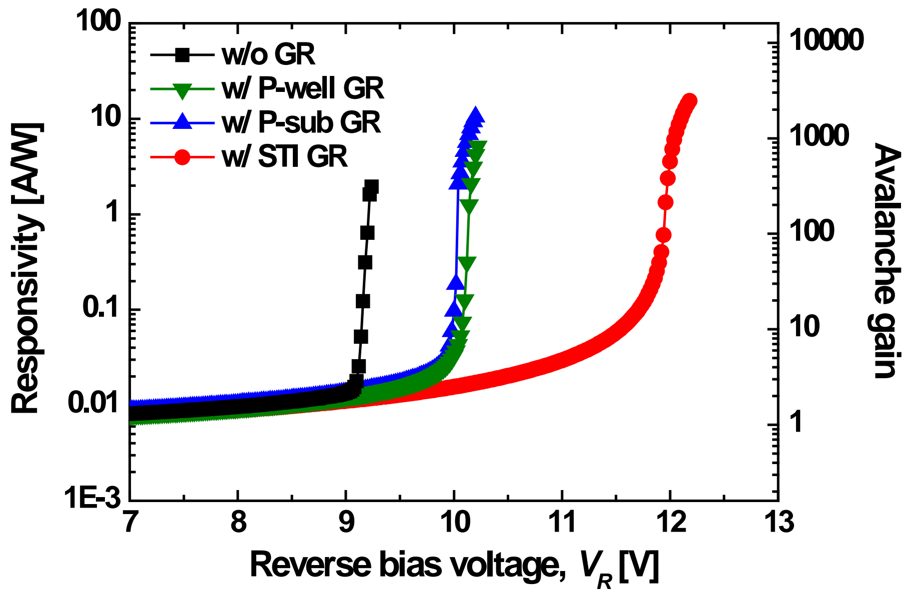


Fig. 5-4. Measured responsivities and avalanche gains for the CMOS-APDs.

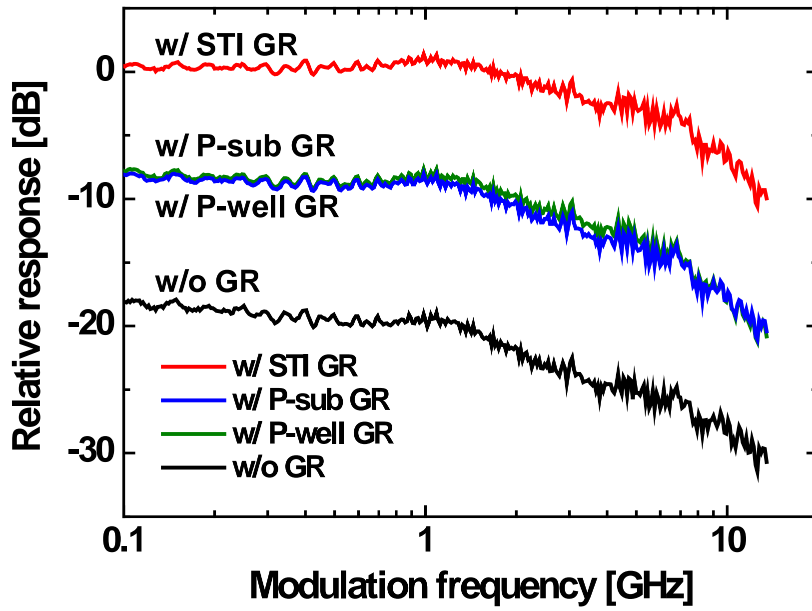


Fig. 5-5. Measured photodetection frequency responses of the CMOS-APDs.

5-1-3. Discussions

The avalanche gain M in an APD can be roughly estimated using $M = \left[1 - \frac{1}{2} \cdot W \cdot \alpha_{eff}(E_M)\right]^{-1}$ [29], where W is the depletion width, E_M is the maximum electric field, and $\alpha_{eff}(E_M)$ is the effective ionization rate at the maximum electric field. Using the above equation with W and E_M determined from the simulation and $\alpha_{eff}(E_M)$ from [25], the ratio of M between different types of CMOS-APDs can be estimated at the bias voltage about 0.1-V below the breakdown voltages as shown in Table 5-1. For the structure without GR, the simulated value of E_M at the planar junction region is used for this estimation rather than at the corner of P^+ implantation where the electric field is higher. This is because the corner region is located outside the focused beam spot when light is injected through the lensed fiber and most photogenerated carriers are generated in the planar junction region. Here, M is normalized to its respective values for the CMOS-APDs without GR in order to cancel out uncertainties due to the used approximate expression for M. The obtained results agree well with the measurement results as shown in Table 5-1. The results show that different GR structures produce different electric field magnitudes that photogenerated carriers experience, which, in turn, influence the

achievable avalanche gain. Clearly, STI provides the optimum GR structure with the largest avalanche gain in standard CMOS technology.

Table 5-1

AVALANCHE GAIN: CALCULATION AND MEASUREMENT

	W [cm]	E_M [V/cm]	$\alpha_{eff}(E_M)$ [cm^{-1}]	M_{ratio}	$M_{ratio,DC}$*	$M_{ratio,AC}$**
w/o GR	0.29×10^{-4}	3.9×10^5	2×10^4	1	1	1
P-well GR	0.30×10^{-4}	5×10^5	5×10^4	2.86	3.13	3.16
P-sub GR	0.30×10^{-4}	5×10^5	5×10^4	2.86	3.13	3.16
STI GR	0.33×10^{-4}	5.7×10^5	5.5×10^4	7.71	7.88	7.94

*Determined from measured gain characteristics shown in Fig. 5-4.
**Determined from frequency responses shown in Fig. 5-5.
(Factor of two correction made as Fig. 5-5 shows power measurement results.)

5-2. Electrode-Dependent Characteristics

In this section, the effects of electrode structures on the performance of silicon APDs fabricated with standard CMOS/BiCMOS technology will be discussed. As previously mentioned, the CMOS-APD has two PN junctions, and photocurrents are extracted from the P^+ port in the N-well region to use only the upper PN junction, resulting in higher-speed operation. To implement the P^+ port on optical window, electrode structures should be considered since they can influence on the CMOS-APD performance. Two types of electrodes for CMOS-APD output port were fabricated, and their photodetection frequency responses were measured to clarify the effects of electrodes on the performance of CMOS-APD.

5-2-1. Test Structures

For effective collection of the photogenerated carriers, multi-finger electrodes can be used in photodetectors. Fig. 5-6 shows simplified layouts of CMOS-APDs fabricated with 0.25-μm standard BiCMOS technology. The CMOS-APDs are based on the P^+/DNW junction, and

they have (a) 1.3-μm and (b) 9.6-μm spacing multi-finger electrodes on $30 \times 30\text{-}\mu m^2$ optical windows, which are implemented by blocking the salicide process for optical injection. No design rule is violated for realizing the CMOS-APDs. Although the use of the narrow-spacing multi-finger electrodes deteriorates optical coupling efficiency, as shown in Fig. 5-6(a), the lateral transit time of photogenerated carrier and the parasitic resistance can be reduced.

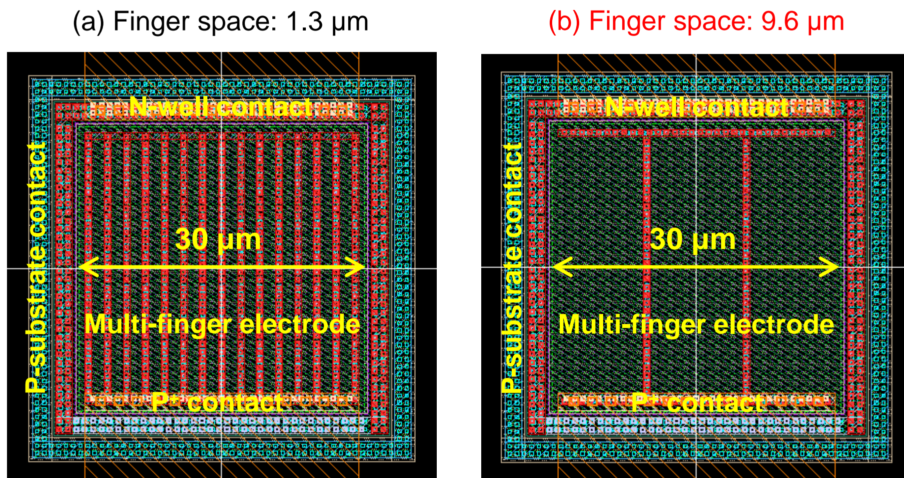


Fig. 5-6. Simplified CMOS-APD layouts with (a) 1.3-μm and (b) 9.6-μm spacing multi-finger electrodes on $30 \times 30\text{-}\mu m^2$ optical windows.

5-2-2. Experimental Results and Discussions

Fig. 5-7 shows measured photodetection frequency responses for the CMOS-APDs having (a) 1.3-μm and (b) 9.6-μm spacing multi-finger electrodes on optical windows at the optimal bias voltage for the photodetection frequency response. As shown in this figure, the photodetection frequency response using 9.6-μm spacing multi-finger electrodes is enhanced about 4 dB without photodetection bandwidth degradation. This is because the larger finger spacing, a few electrodes on optical window, gives better responsivity for the CMOS-APD due to better optical injection. Moreover, there is no degradation of photodetection-bandwidth performance because the reduced lateral transit time in the P^+ region has little influence on the bandwidth performance due to the dominant bandwidth limiting factor of the hole-diffusion time in N-well.

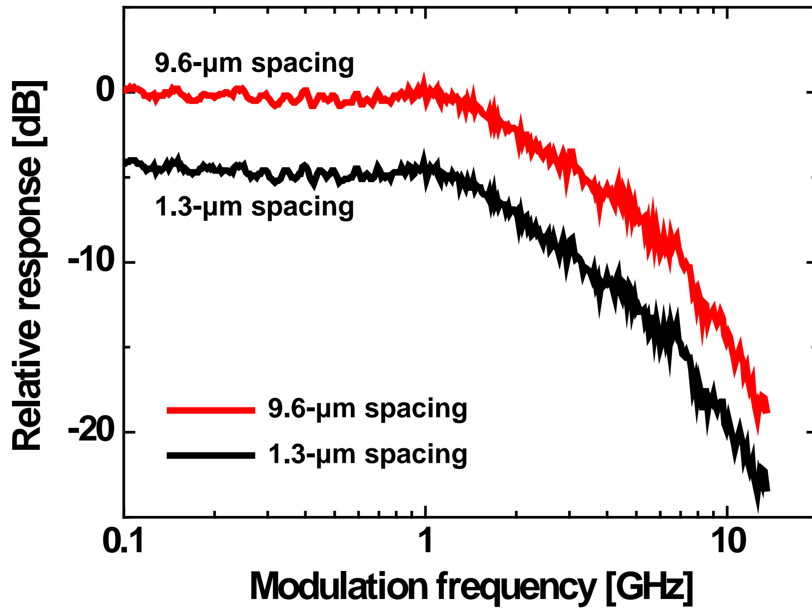


Fig. 5-7. Measured photodetection frequency responses of the CMOS-APDs having (a) 1.3-μm and (b) 9.6-μm spacing multi-finger electrodes on optical windows at the optimal bias voltage.

5-3. Silicide-Dependent Characteristics

In this section, the influences of silicide on the performance of silicon APDs fabricated with standard CMOS technology will be investigated. For the injection of optical signals into the CMOS-APD, optical window is formed by blocking the salicide process during the fabrication process. To use only the upper P^+/N-well junction, photocurrents should be extracted from the P^+ port on the optical window, and therefore the contacts for the output port are affected by the optical-window formation, which can result in performance degradation of the CMOS-APD. Two types of CMOS-APDs with and without silicide under the output contacts were fabricated, and performances were measured and analyzed with the equivalent circuit model.

5-3-1. Device Description

To implement optical window in CMOS technology, the salicide process, which is commonly implemented in CMOS technology for ohmic contacts to support interconnects, should be blocked. The

simplest way of realizing the optical window in CMOS technology is using a salicide blocking layer for all optical-window area as shown in Fig. 5-8(a). However, it causes removal of silicide under the contacts, which can result in increase of the parasitic resistance. The other way is using a salicide blocking layer for optical-window area except electrodes as shown in Fig. 5-8(b). With this, the silicide is formed under the contacts, resulting in very low parasitic resistance. To realize the salicide blocking layer except electrodes, however, optical injection loss can increase to meet the design rules for CMOS technology such as the spacing between contact and salicide blocking layer.

As mentioned in section 5-2, only a few electrodes are needed for the CMOS-APD. In addition, the optical-injection loss owing to the electrodes as well as the space between salicide blocking layer and contact becomes lower as scaling down of CMOS technology. For example, the minimum metal width and contact size is 0.16 μm, and the minimum contact to salicide block layer space is 0.2 μm, which are the design rules of a 0.13-μm standard CMOS technology. With this, the injection loss can be negligible for realizing photodetectors having over 10-μm diameter optical window.

Fig. 5-9 shows the CMOS-APDs fabricated with 0.13-μm standard CMOS technology, which are based on the same P^+/N-well junction.

The difference of the two types of CMOS-APDs is that they are realized with and without silicide under P^+ contacts as shown in Fig. 5-8. The optical-window area is 20×20 μm^2, and STI is inserted between P^+ and N^+ regions.

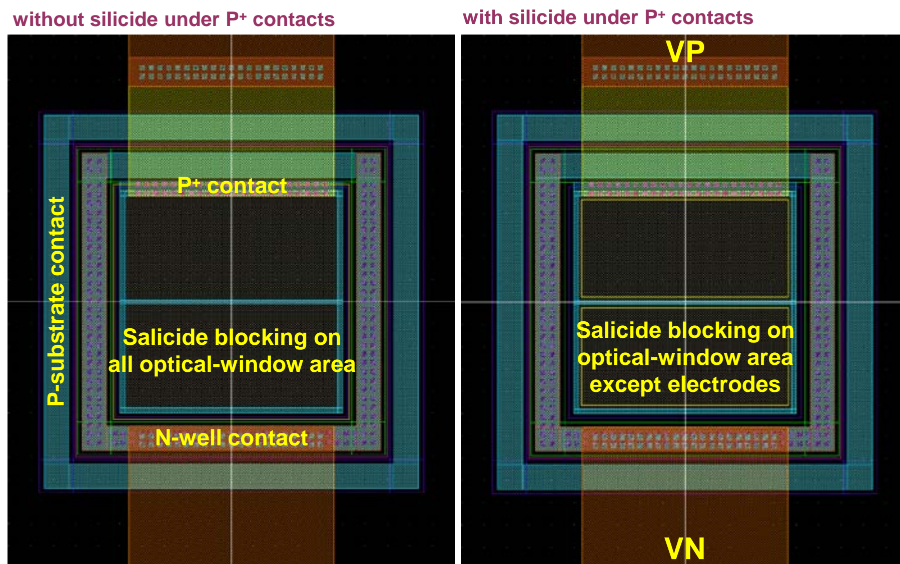
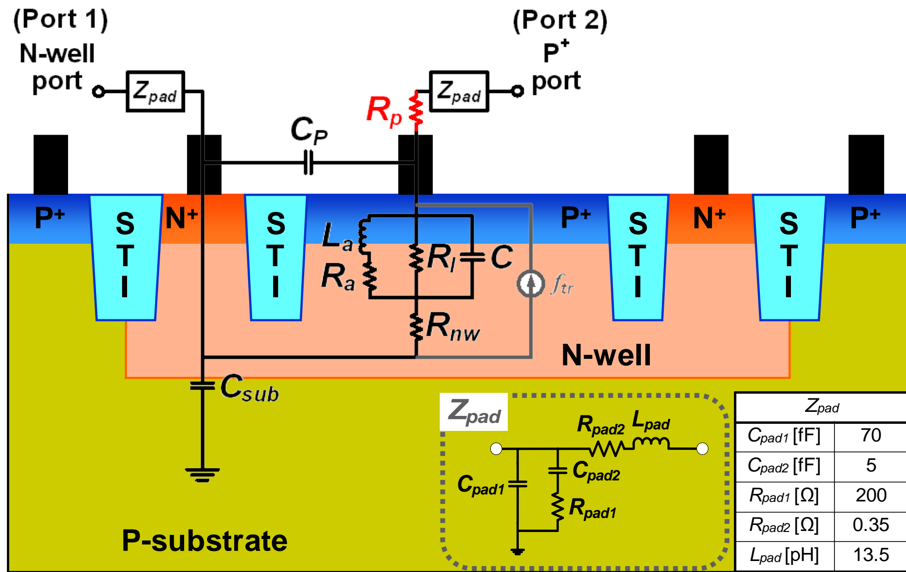


Fig. 5-8. Simplified CMOS-APD layouts (a) without silicide and (b) with silicide under P^+ contacts.



Z_{pad}	
C_{pad1} [fF]	70
C_{pad2} [fF]	5
R_{pad1} [Ω]	200
R_{pad2} [Ω]	0.35
L_{pad} [pH]	13.5

Fig. 5-9. Structure and equivalent circuit model of the fabricated CMOS-APDs with parasitic resistance, R_p, at the output P^+ port.

5-3-2. Experimental Results and Analyses With Equivalent Circuit Model

Fig. 5-10 shows measured current-voltage characteristics as well as responsivity and avalanche gain of the fabricated CMOS-APDs. As shown in the inset with a linear scale for the y-axis of Fig. 5-10, the CMOS-APD without silicide under P^+ contacts for the output port has larger parasitic resistance than with silicide. Therefore, the output currents of CMOS-APD without silicide are smaller than with silicide at the same reverse bias voltage due to the junction voltage drop caused by the parasitic resistance. Consequently, because of the parasitic resistance, the responsivity and avalanche gain of the CMOS-APD are decreased as shown in Fig. 5-10(b).

Fig. 5-11 shows measured photodetection frequency responses of the CMOS-APDs at different bias voltages (a) with silicide and (b) without silicide under P^+ contacts. The optimal bias voltage for the photodetection frequency response is increased slightly from 10.25 V to 10.30 V without the silicide, because the current-voltage curve is changed owing to the parasitic resistance as shown in the inset of Fig. 5-10.

The equivalent circuit model for the CMOS-APDs is shown in Fig.

5-9. With this, further investigation is performed for understanding the CMOS-APD impedances and performances. The parameters of the equivalent circuit model are extracted from the two-port S-parameter and photodetection frequency response measurements as described in chapter 4. Fig. 5-12 shows electrical reflection coefficients at the P^+ port from 50 MHz to 13.5 GHz for the CMOS-APDs biased at 10.25 V and 10.30 V, respectively. The measured and simulated results show good matching. The extracted parameter values for Z_{pad} are listed in Fig. 5-9, and Table 5-2 shows extracted parameter values that are used for simulation. It clearly shows that removal of silicide under the contacts results in the parasitic resistance (R_p), and then it affects the resistance of the CMOS-APD.

Fig. 5-13 shows measured and simulated photodetection frequency responses of CMOS-APDs with and without silicide under P^+ contacts. As shown in this figure, the photodetection frequency response of the CMOS-APD without silicide under P^+ contacts is decreased about 3 dB, and the photodetection bandwidth of the CMOS-APD is also decreased from 4.8 GHz to 3 GHz.

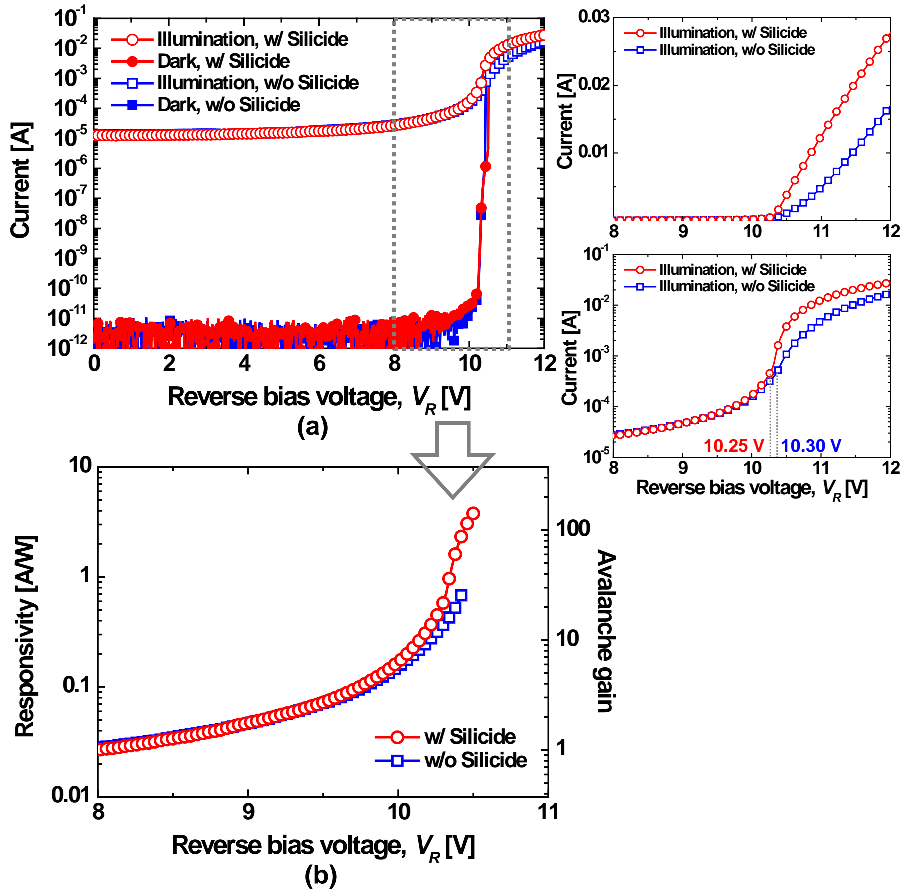


Fig. 5-10. (a) Current characteristics and (b) responsivity and avalanche gain of CMOS-APDs as a function of the reverse bias voltage with and without silicide under P^+ contacts. The insets are magnified current-voltage characteristics as a linear scale and a logarithmic scale for the y-axis.

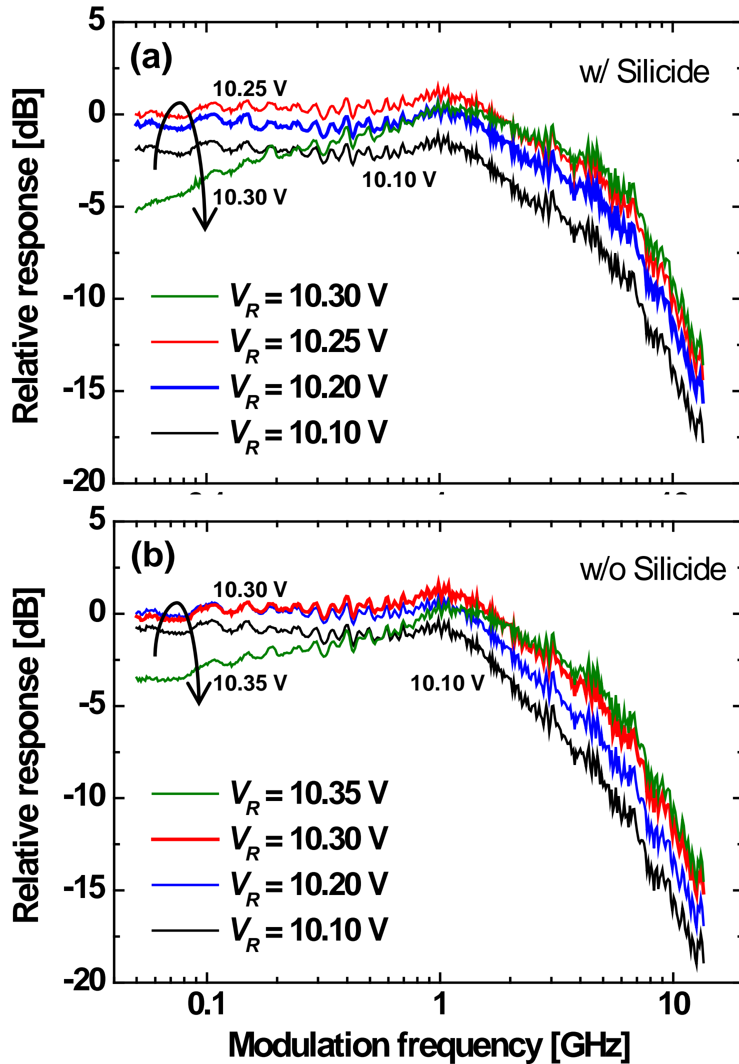


Fig. 5-11. Photodetection frequency responses of CMOS-APDs at different bias voltages (a) with silicide and (b) without silicide under P^+ contacts.

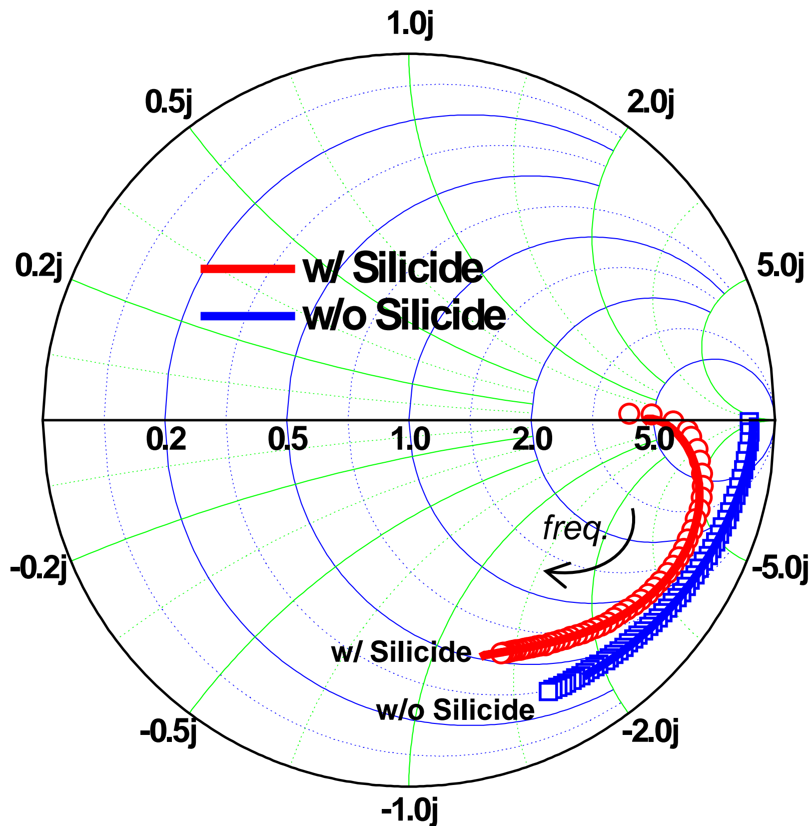


Fig. 5-12. Measured and simulated electrical reflection coefficients of CMOS-APDs from 50 MHz to 13.5 GHz with and without silicide under P^+ contacts. Hollow circles represent measured data, and solid lines represent simulated results.

Table 5-2

EXTRACTED PARAMETERS FOR CMOS-APDS
WITH AND WITHOUT SILICIDE UNDER P^+ CONTACTS

	w/ Silicide	w/o Silicide
R_p [Ω]	0	30
C_p [fF]	60	
L_a [nH]	13	
R_a [Ω]	150	1000
R_l [kΩ]	1.2	
C [fF]	140	
R_{nw} [Ω]	50	1000
C_{sub} [fF]	45	
f_{tr} [GHz]	3	

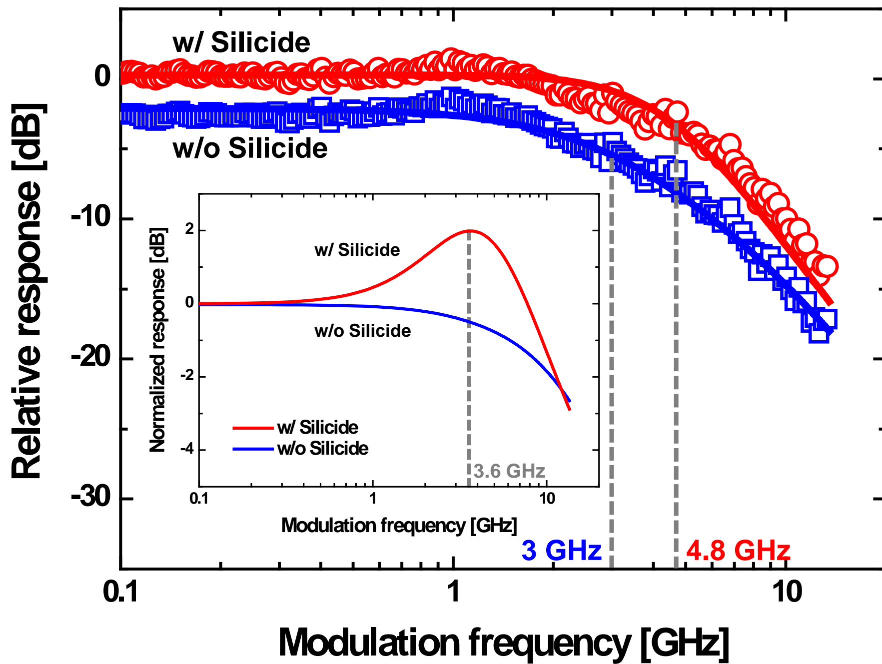


Fig. 5-13. Measured and simulated photodetection frequency responses of CMOS-APDs with and without silicide under P^+ contacts. Hollow circles represent measured data, and solid lines represent simulated results. The inset shows normalized photodetection frequency responses of CMOS-APDs without the photogenerated-carrier transit time.

5-3-3. Discussions

It seems like the photodetection bandwidth decrease is due to the increased RC time constant of the CMOS-APD because of the parasitic resistance. In order to identify the origin of the bandwidth decrease, further investigation is done using the equivalent circuit model. By using the frequency-independent current source into the equivalent circuit model (not including f_{tr} in the current source), photodetection frequency responses of CMOS-APDs determined by device RLC components and inductive-peaking effect can be clearly observed. As shown in the inset of Fig. 5-13, clear peaking in the photodetection frequency response is shown with the CMOS-APD with silicide under P^+ contacts, while there is no peaking without silicide under P^+ contacts. This is because the high series resistance, R_a, of the avalanche regime. As listed in Table 5-2 and shown in Fig. 5-12, the high parasitic resistance of the CMOS-APD without silicide increases the resistance of the CMOS-APD. Therefore the increased resistance in series with the inductor decreases the inductor quality factor of the CMOS-APD, resulting in no peaking effect. Consequently, the CMOS-APD without silicide for the output port cannot utilize the inductive-peaking effect, but the CMOS-APD with silicide can utilize the inductive-peaking

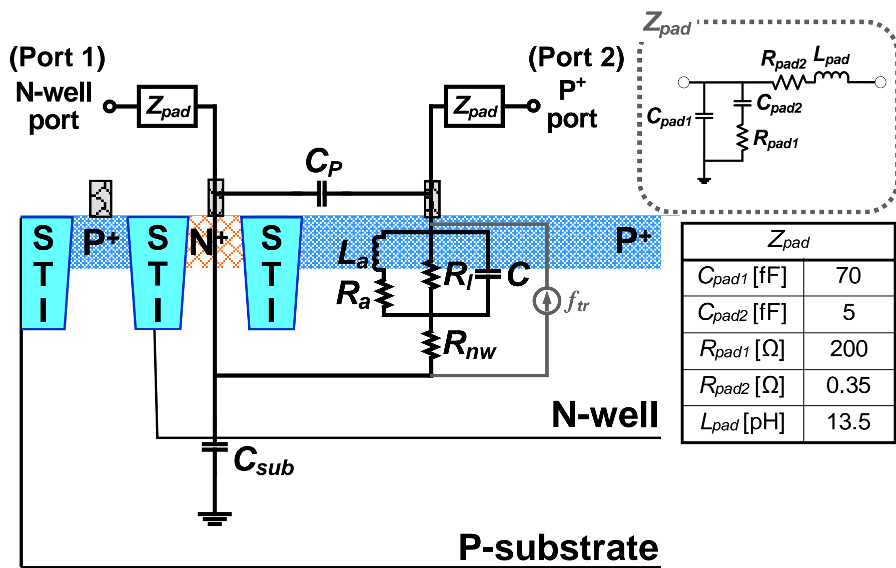
effect, which brings higher photodetection-bandwidth performance.

5-4. Area-Dependent Characteristics

In this section, area-dependent photodetection frequency responses of CMOS-APDs will be investigated for the goal of identifying the factors that influence the photodetection bandwidth and achieving the optimal photodetection bandwidth. P^+/N-well CMOS-APDs having four different device areas are realized, and their current-voltage characteristics, electrical reflection coefficients, and photodetection frequency responses are measured. Then, an equivalent circuit model is developed for each type of CMOS-APD from the measurement results. The resulting equivalent circuits are then analyzed for understanding the CMOS-APD photodetection frequency response. From this investigation, dominant factors that influence the photodetection frequency responses are identified, and their influences are clarified for different device areas. Among the investigated devices, the CMOS-APD having $10 \times 10\text{-}\mu m^2$ device area is found to have the largest 3-dB photodetection bandwidth of 7.6 GHz, which is the largest value reported for 850-nm photodetectors fabricated with standard CMOS technology.

5-4-1. Device Structure

Fig. 5-14 shows the basic structure of CMOS-APDs used in this investigation. They are based on P^+/N-well junction fabricated with 0.13-μm standard CMOS technology having 1 poly and 7 metals. Four types of CMOS-APDs having optical-window areas of 10×10, 20×20, 30×30, and 40×40 μm^2 are realized. STI is inserted as a guard ring between P^+ and N^+ regions since it provides a high uniform electric field profile without premature edge breakdown. For optical-window formation, the salicide process is blocked. 0.2-μm wide multi-finger electrodes are formed for the P^+ port located in the N-well region. Photocurrents are extracted from the P^+ port located in the N-well region so that slow diffusion currents generated in the P-substrate can be excluded. The P^+/N-well junction is reverse biased with a positive voltage applied to the N-well port and P^+ grounded. The P-substrate port is also grounded. All CMOS-APDs are fabricated without any design or layout rule violation.



Z_{pad}	
C_{pad1} [fF]	70
C_{pad2} [fF]	5
R_{pad1} [Ω]	200
R_{pad2} [Ω]	0.35
L_{pad} [pH]	13.5

Fig. 5-14. Equivalent circuit model for CMOS-APDs.

5-4-2. Experimental Results and Analyses With Equivalent Circuit Model

Fig. 5-15(a) shows current-voltage characteristics of the CMOS-APDs under illumination and dark conditions. For the measurements, light from an 850-nm laser diode was injected into the device using a lensed fiber having 10-μm spot diameter. The optical power was 1 mW measured at the end of the lensed fiber. All the CMOS-APDs exhibit low dark currents below a few nA before avalanche breakdown. The CMOS-APDs having different device areas show similar current-voltage characteristics under the illumination condition. As the reverse bias voltage approaches the avalanche breakdown voltage of about 10.45 V, currents start to increase abruptly due to avalanche gain. The responsivity is only about 0.015 A/W at the reverse bias voltage of 1 V, but the maximum responsivity is about 2 A/W at the reverse bias voltage of 10.45 V as shown in Fig. 5-15(b). When the reverse bias voltage is larger than the breakdown voltage, currents are saturated due to the series resistance and the space-charge effect [25]. Smaller devices saturate slightly earlier because they have higher parasitic resistance due to the smaller number of contacts and vias for the electrodes, but this difference is negligible at the V_R = 10.25 V used in

our investigation for optimal photodetection frequency response.

Fig. 5-16 shows photodetection frequency responses for CMOS-APDs having four different areas measured at the optimal bias voltage of 10.25 V. For all the frequency response measurements, the incident optical power had the average power of 1 mW measured at the end of the lensed fiber. As can be seen in the figure, smaller devices have larger photodetection bandwidth, reaching 7.6 GHz for the 10×10-μm^2 CMOS-APD.

To better understand CMOS-APD photodetection frequency response characteristics, equivalent circuit models for CMOS-APDs are derived. Fig. 5-14 also shows the equivalent circuit model used for this investigation. As described in chapter 4, the parameter values for the elements of the equivalent circuit model are extracted from the two-port S-parameter and photodetection frequency response measurements. Fig. 5-17 shows electrical reflection coefficients at P^+ port on Smith chart from 50 MHz to 13.5 GHz for different CMOS-APDs biased at 10.25 V, from measurement and simulation with extracted parameter values. Table 5-3 shows values for extracted parameters that are used for simulation. Z_{pad} are assumed the same for all types of devices and listed in Fig. 5-14. The extracted values for L_a, R_a, and R_l are the same for all device types. Avalanche inductor L_a does not change with the

device area at the same bias condition since all CMOS-APDs have same avalanche multiplication characteristics based on the same P^+/N-well junction and guard ring as shown in Fig. 5-15(a). R_a represents the series resistance associated with avalanche inductor L_a and determines the avalanche inductor quality factor, which is not directly related to the device area [27]. R_l is defined to the voltage-to-current ratio in the vicinity of 0 V, and all CMOS-APDs have similar slope of the current-voltage curve as shown in Fig. 5-15(a), resulting in the same R_l for all device types. The junction capacitance C is proportional to the device area. C_{sub} and C_p also increase with the device area, but R_{nw} does not change very much because the increase in lateral resistance compensates the decrease in vertical resistance with larger devices. Fig. 5-18 shows normalized measured and simulated photodetection frequency responses for CMOS-APDs having different device areas at the reverse bias voltage of 10.25 V. Also shown in each figure is the value of f_{tr} that gives the best fitting between measurement and simulation. The fitted f_{tr} value decreases as the device area increases due to the increase of the lateral diffusion path.

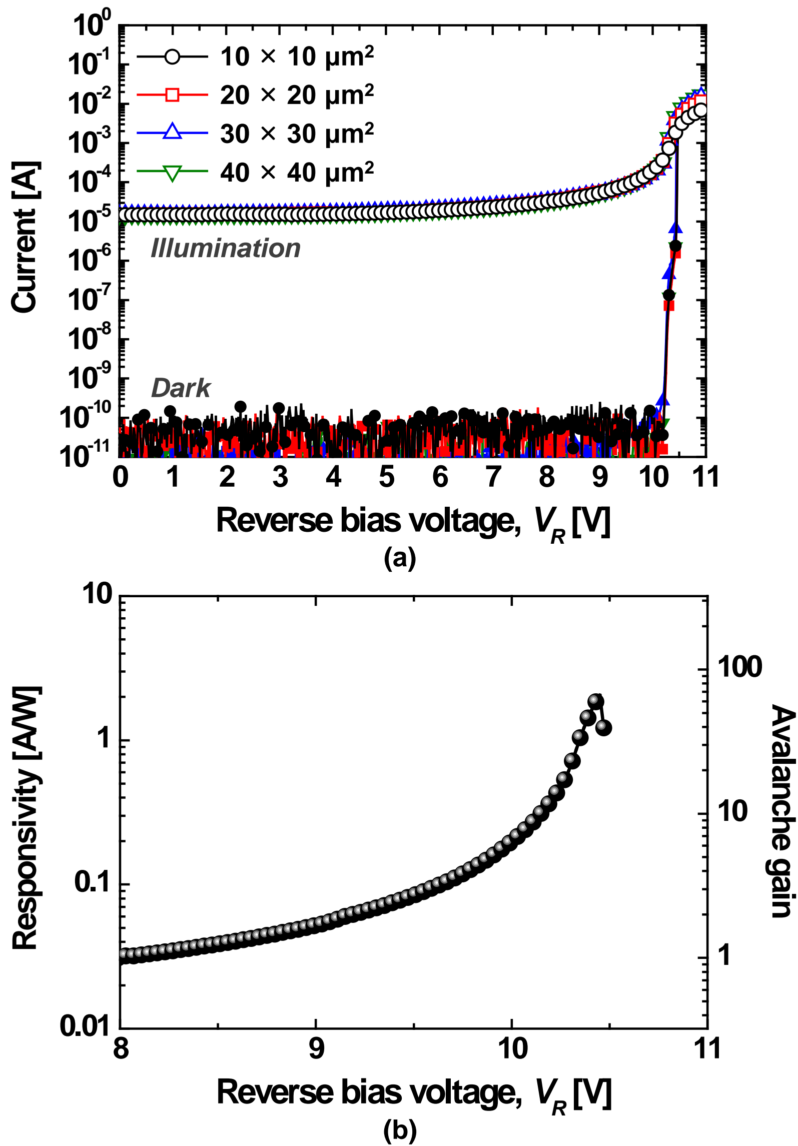


Fig. 5-15. (a) Current-voltage characteristics of CMOS-APDs and (b) responsivity and avalanche gain of 10 × 10-μm^2 CMOS-APD as function of reverse bias voltage.

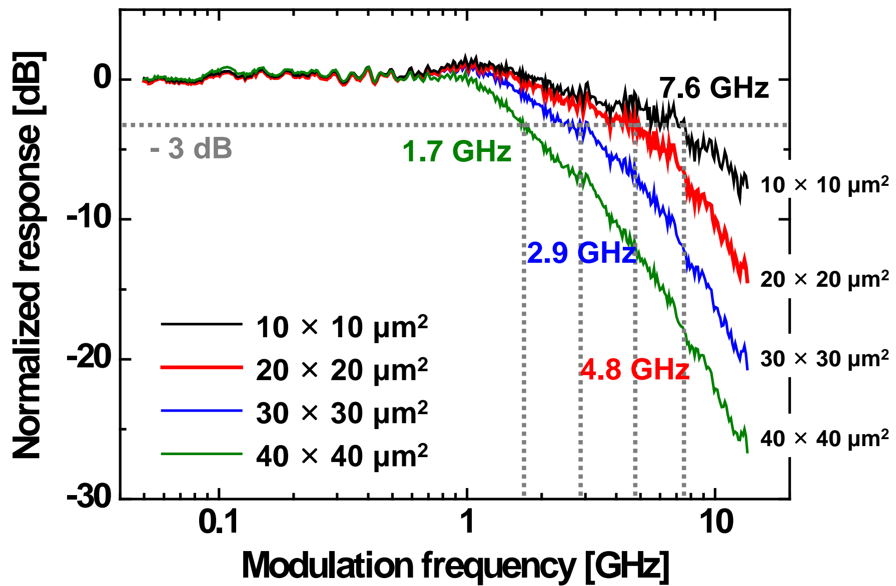


Fig. 5-16. Normalized photodetection frequency responses of the CMOS-APDs having different device areas.

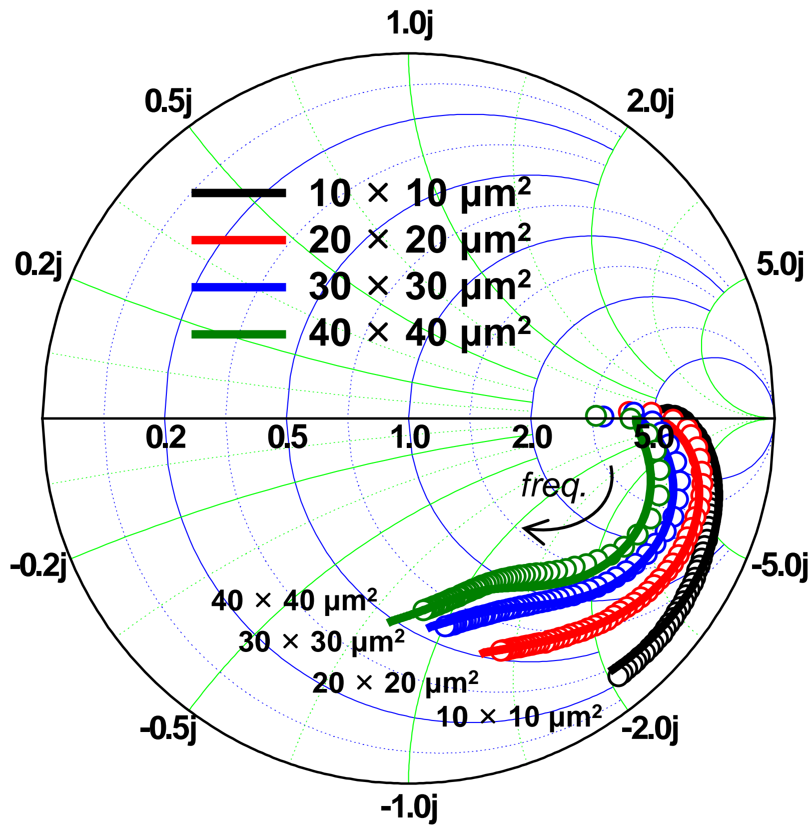


Fig. 5-17. Measured and simulated electrical reflection coefficients for different CMOS-APDs at the reverse bias voltage of 10.25 V. Hollow circles represent the measured data and solid lines as the simulated results.

Table 5-3

EXTRACTED PARAMETERS FOR CMOS-APDS
ACCORDING TO DEVICE AREAS

Area [μm^2]	10 × 10	20 × 20	30 × 30	40 × 40
L_a [nH]	13			
R_a [Ω]	150			
R_l [kΩ]	1.2			
C [fF]	35	140	315	560
R_{nw} [Ω]	60	50	40	30
C_{sub} [fF]	15	45	90	150
C_p [fF]	20	60	120	180

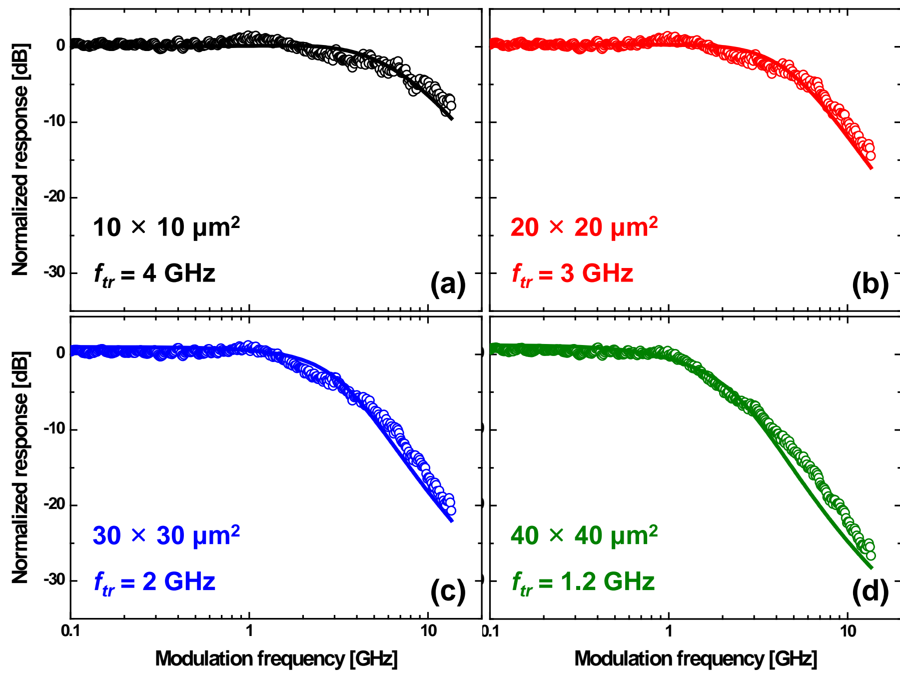


Fig. 5-18. Measured and simulated photodetection frequency responses for different CMOS-APDs at the reverse bias voltage of 10.25 V. Hollow circles represent the measured data and solid lines as the simulated results.

5-4-3. Discussions

The photodetection frequency response of an APD can be influenced by four different factors: transit time of photogenerated carriers, device RC time constant, inductive-peaking effect, and parasitics. In order to identify how each of these factors influences the CMOS-APDs, only certain factors among these four are considered at a time and the resulting photodetection frequency responses are compared. This can be easily done by simulating the photodetection frequency response with an equivalent circuit in which certain circuit elements are intentionally left out.

Fig. 5-19 shows simulated photodetection frequency responses of CMOS-APDs having different device areas at the reverse bias voltage of 10.25 V under various conditions. For each type of device, four different simulation results are shown: one that considers only the photogenerated-carrier transit time (not including L_a, R_a, R_l, C, R_{nw}, C_{sub}, and C_p), another that considers only the RC time constant (not including f_{tr} in the current source as well as L_a and R_a), third that considers the inductive-peaking effect (not including f_{tr} in the current source), and fourth that includes all the factors which are also shown in Fig. 5-18. In Fig. 5-19, it can be observed that the transit time is the

dominant bandwidth-limiting factor. Even with this limitation, however, higher total bandwidth can be achieved because inductive peaking provides high-frequency boosting. The 10 × 10-μm^2 CMOS-APD has 7.6-GHz photodetection bandwidth with the inductive-peaking effect at 6.5 GHz while its f_{tr} is 4 GHz.

Fig. 5-20 compares the influence of each effect for devices with different device areas. Fig. 5-20(b) shows that smaller devices have higher inductive-peaking frequencies. This is because capacitance becomes smaller with the decreasing device area and the inductive-peaking frequency is inversely proportional to the square root of capacitance. Fig. 5-20(c) and (d) show that photodetection frequency responses for the RC time constant and the transit time have larger bandwidth as the device area decreases. This is due to decrease in the capacitance for the RC time constant and lateral diffusion path for the transit time.

Fig. 5-21 shows the simulated photodetection frequency responses with and without the parasitics. For simulation without the parasitics, C_{sub}, C_p, and Z_{pad} are not included. Although the parasitics affect photodetection frequency responses for the inductive-peaking effect and RC time constant, they do not affect the total response very much as the limiting factor for the devices is the photogenerated-carrier

transit time.

As a summary, the photodetection frequency response is limited by the transit time of holes photogenerated in the charge-neutral N-well region, but this is somewhat compensated by inductive peaking provided by the inductive component in avalanche region. In addition, smaller devices have larger bandwidth because their hole transit time is smaller and inductive-peaking frequency is higher with smaller capacitance.

Performances of various silicon photodetectors fabricated with standard CMOS technology are compared in Table 5-4. Based on the meshed SMPD [15], 6.9 GHz of photodetection bandwidth was achieved, but it has very low responsivity. In contrast, the $10 \times 10\text{-}\mu m^2$ CMOS-APD shows the best photodetection bandwidth performance of 7.6 GHz along with high responsivity.

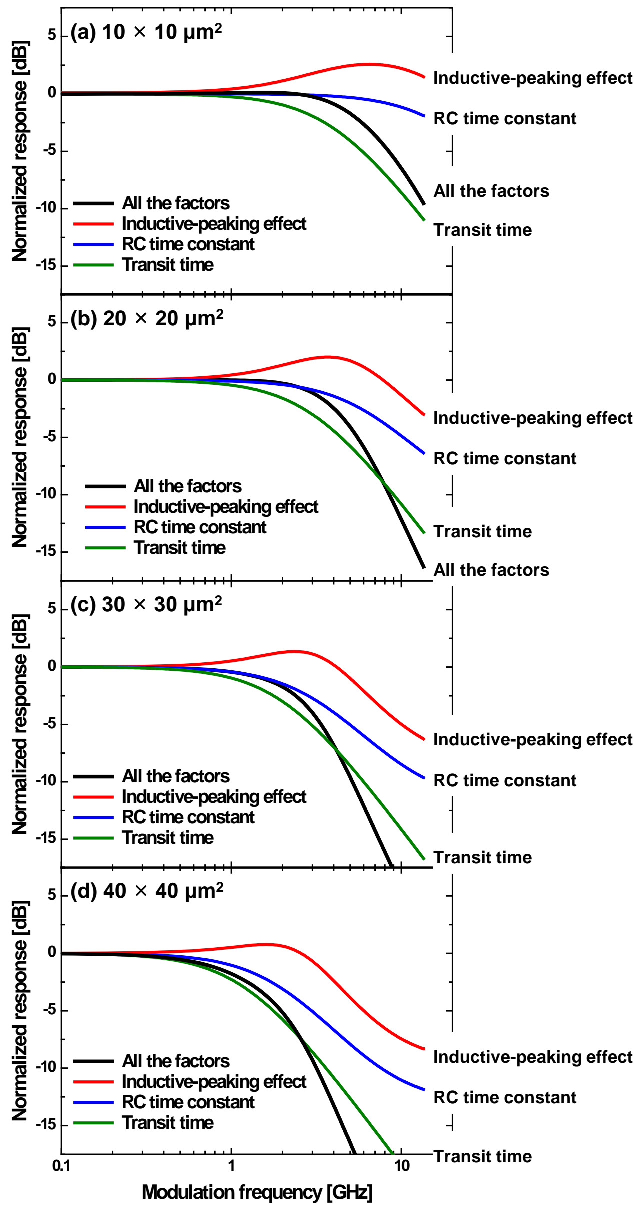


Fig. 5-19. Normalized photodetection frequency responses of CMOS-APDs for the photogenerated-carrier transit time, the RC time constant, the inductive-peaking effect, and all the factors according to device areas.

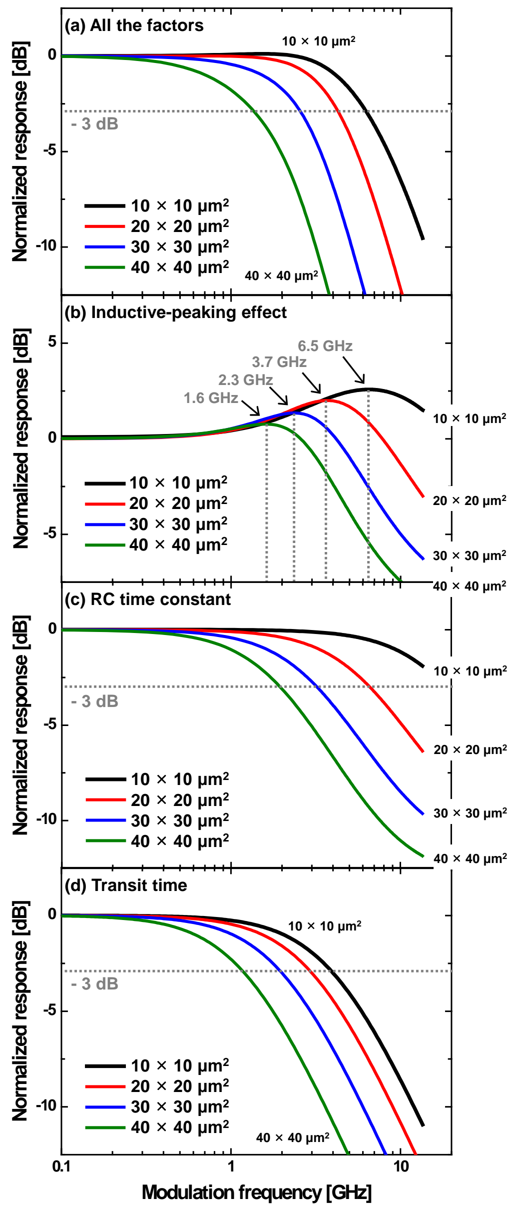


Fig. 5-20. Normalized photodetection frequency responses of CMOS-APDs having different device areas for (a) all the factors, (b) the inductive-peaking effect, (c) the RC time constant, and (d) the photogenerated-carrier transit time.

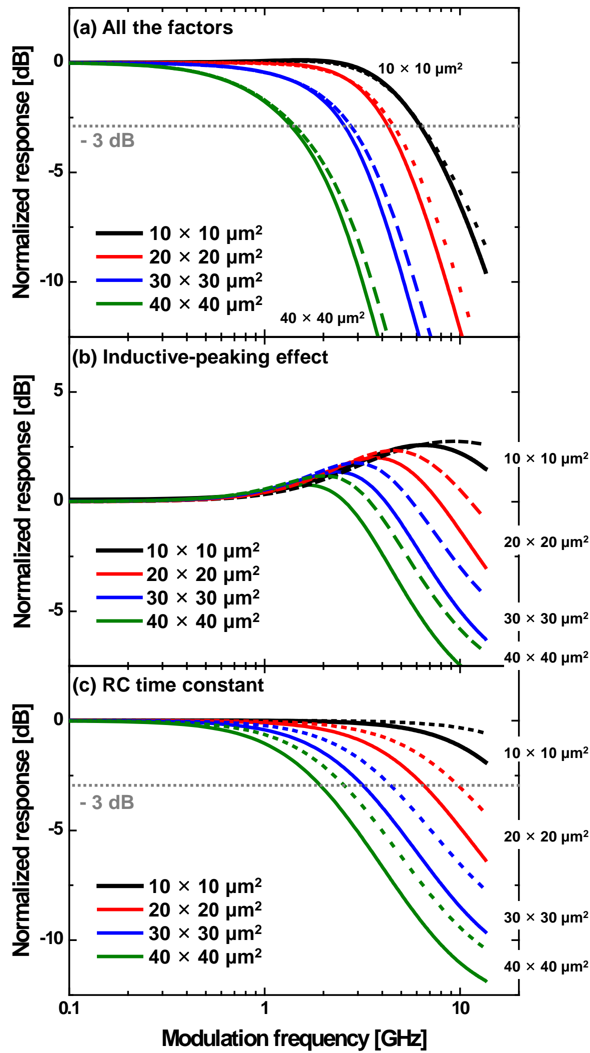


Fig. 5-21. Normalized photodetection frequency responses of the CMOS-APDs having different device areas with and without the parasitics for (a) all the factors, (b) the inductive-peaking effect, and (c) the RC time constant. Solid and dotted lines represent the simulated responses with and without the parasitics, respectively.

Table 5-4

PERFORMANCE COMPARISON OF SILICON PHOTODETECTORS FABRICATED WITH STANDARD CMOS TECHNOLOGY

	[16]	[12]	[15]		This work	
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS	0.13-μm CMOS
Structure	Multiple p^+-p-n APD	$P^+/P^-/N^+$ lateral PIN	Strip SMPD*	Meshed SMPD*	P^+/N-well APD	P^+/N-well APD
R	0.74 A/W	0.073 A/W	0.057 A/W	0.029 A/W	0.48 A/W	0.48 A/W
BW	1.6 GHz	1.9 GHz	1.8 GHz	6.9 GHz	1.7 GHz	7.6 GHz
C_{PD}	345 fF	1600 fF	213 fF	206 fF	560 fF	35 fF
A	50 × 50 μm^2 (Square)	50 × 50 μm^2 (Square)	55 × 55 μm^2 (Octagon)	55 × 55 μm^2 (Octagon)	40 × 40 μm^2 (Square)	10 × 10 μm^2 (Square)
V_R	14.3 V	6 V	14.2 V	14.2 V	10.25 V	10.25 V

*SMPD: spatially modulated photodetector

R: responsivity, *BW*: bandwidth, C_{PD}: intrinsic photodetector capacitance, *A*: optical-window area, V_R: reverse bias voltage

5-5. Junction-Dependent Characteristics (1)

As mentioned in section 2-2, the PN junctions in CMOS technology affect the CMOS-APD performance. In this section, the performance of the CMOS-APDs based on three different types of PN junctions, N-well/P-substrate, P^+/N-well, and N^+/P-well, will be investigated.

5-5-1. Device Structures

Fig. 5-22 shows the CMOS-APDs based on (a) N-well/P-substrate, (b) P^+/N-well, and (c) N^+/P-well junctions. If triple wells including DNW can be available in standard CMOS technology, the CMOS-APD based on N^+/P-well is possible, in which the influence of the P-substrate can be excluded using the DNW. All CMOS-APDs include STI between P^+ and N^+ regions. For the P^+/N-well and N^+/P-well CMOS-APDs, photocurrents are extracted from P^+ and N^+ ports located inside N-well and P-well, respectively. The P^+ port for the P-substrate is tied to ground, and the N^+ port for the DNW of the N^+/P-well CMOS-APD is also tied to ground. For all three types, optical windows having the area of 30 × 30 μm^2 are formed by blocking the salicide

process. These CMOS-APDs can be realized without violating any design rules for the CMOS process technology.

Although it is preferred to use one identical CMOS technology for comparing three different types, two different CMOS technologies available to this investigation had to be used. The N-well/P-substrate CMOS-APD was implemented by 0.13-μm standard CMOS technology and the N^+/P-well CMOS-APD by 65-nm standard CMOS technology. The P^+/N-well CMOS-APDs were fabricated with both CMOS technologies, and these two are distinguished in this paper with the notation of P^+/N-well_130 and P^+/N-well_65.

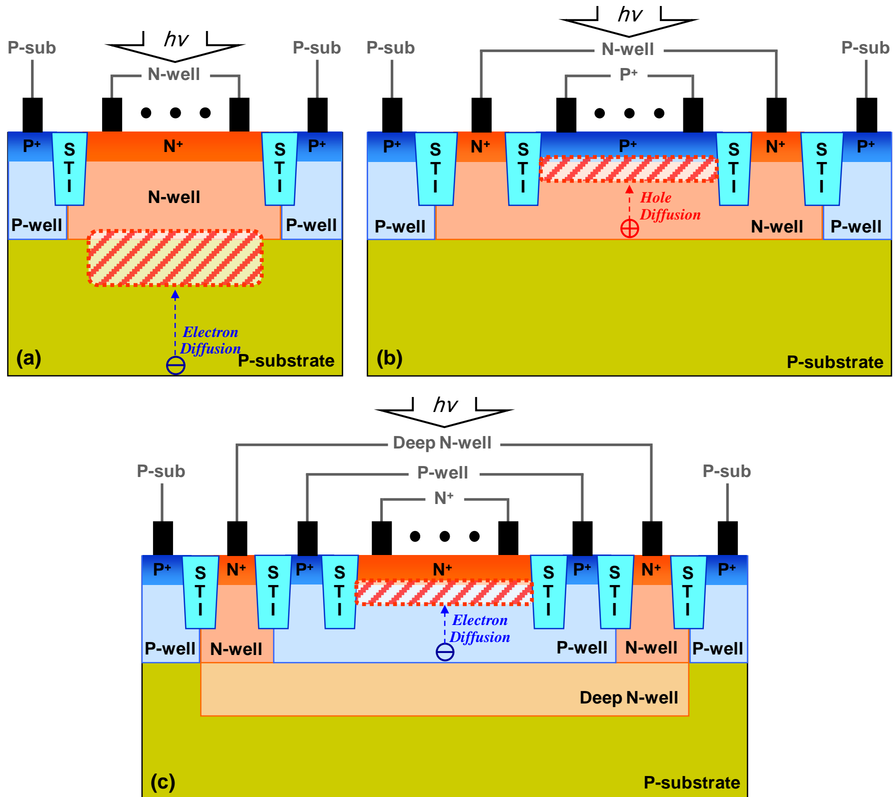


Fig. 5-22. Cross sections of the fabricated CMOS-APDs: (a) N-well/P-substrate, (b) P^+/N-well, and (c) N^+/P-well CMOS-APDs.

5-5-2. Experimental Results

Fig. 5-23 shows measured current-voltage characteristics of the fabricated CMOS-APDs with and without optical illumination. The avalanche breakdown voltages of N-well/P-substrate, P^+/N-well_130, P^+/N-well_65, and N^+/P-well CMOS-APDs are about 16.9, 10.15, 9.8, and 10.65 V, respectively. The difference in breakdown voltages is mostly due to the difference in doping concentrations. The doping concentration for P-substrate is less than N-well or P-well, resulting in larger breakdown voltage for the N-well/P-substrate CMOS-APD. The discrepancy between P^+/N-well_130 and P^+/N-well_65 CMOS-APDs can be explained by the difference in N-well doping concentration between two CMOS technologies, and the discrepancy between P^+/N-well_65 and N^+/P-well CMOS-APDs by the difference in doping concentration between N-well and P-well. When the bias voltage is small, the N-well/P-substrate CMOS-APD has much higher photogenerated currents. For example, at the reverse bias voltage of 1 V, the N-well/P-substrate CMOS-APD has photogenerated current of about 9.5 μA, whereas P^+/N-well and N^+/P-well CMOS-APDs have about 0.45 μA. This is because the N-well/P-substrate CMOS-APD has larger drift currents with larger depletion width due to lower doping

concentration for P-substrate as well as larger diffusion currents from larger volume of the charge neutral region in P-substrate than P^+/N-well and N^+/P-well CMOS-APDs. All CMOS-APDs exhibit low dark currents below a few nA before avalanche breakdown.

With the increasing reverse bias voltage, responsivity dramatically increases at the avalanche regime owing to the avalanche multiplication process. Fig. 5-24 shows responsivity and avalanche gain of the CMOS-APDs as a function of the reverse bias voltage. The photocurrent is determined by subtracting the dark current from the photogenerated current, and the gain is determined by the ratio of photocurrent at a given bias to that at the reference voltage, 1 V. As can be seen in Fig. 5-24, responsivities become higher for P^+/N-well and N^+/P-well CMOS-APDs as the reverse bias voltage increases. While the maximum responsivity of the N-well/P-substrate CMOS-APD is about 4.7 A/W, the P^+/N-well and N^+/P-well CMOS-APDs have high maximum responsivities over 10 A/W. The difference is due to the influence of STI on the junction breakdown. In the N-well/P-substrate CMOS-APD, breakdown occurs at the edges of the PN junction where the local electric field becomes higher due to junction curvature, because STI does not penetrate deep enough to these junction edges. This premature edge breakdown prevents photogenerated carriers from

having sufficient avalanche gain. However, in the P^+/N-well and N^+/P-well CMOS-APDs, STI having much higher breakdown field strength surrounds the junction edge [25], and consequently, breakdown occurs at the planar PN junction, resulting in higher breakdown field than the N-well/P-substrate CMOS-APD. Therefore, more avalanche gain can be obtained for P^+/N-well and N^+/P-well CMOS-APDs, resulting in higher responsivity than the N-well/P-substrate CMOS-APD as can be seen in Fig. 5-24.

To examine the photodetection bandwidths of the CMOS-APDs, photodetection frequency responses were measured. Fig. 5-25 shows photodetection frequency responses of four different CMOS-APDs at the bias voltage that gives the maximum photodetection frequency response for each type. As can be seen in this figure, P^+/N-well and N^+/P-well CMOS-APDs have much better photodetection bandwidth performances than the N-well/P-substrate CMOS-APD. This is because in the N-well/P-substrate CMOS-APD, many photons are absorbed in the charge neutral P-substrate region where no electric field exists and photogenerated carriers reach the electrode by slow diffusion process, which severely limits the photodetector speed. P^+/N-well and N^+/P-well CMOS-APDs, however, have better performances since slow diffusion photogenerated carriers in the P-substrate region are excluded. The

charge neutral N-well and P-well regions are much smaller and, consequently, carrier transport by diffusion takes less time, resulting in better bandwidth performances. In addition, the N^+/P-well CMOS-APD has higher bandwidth than the P^+/N-well CMOS-APD, because electrons move faster in P-well than holes in N-well.

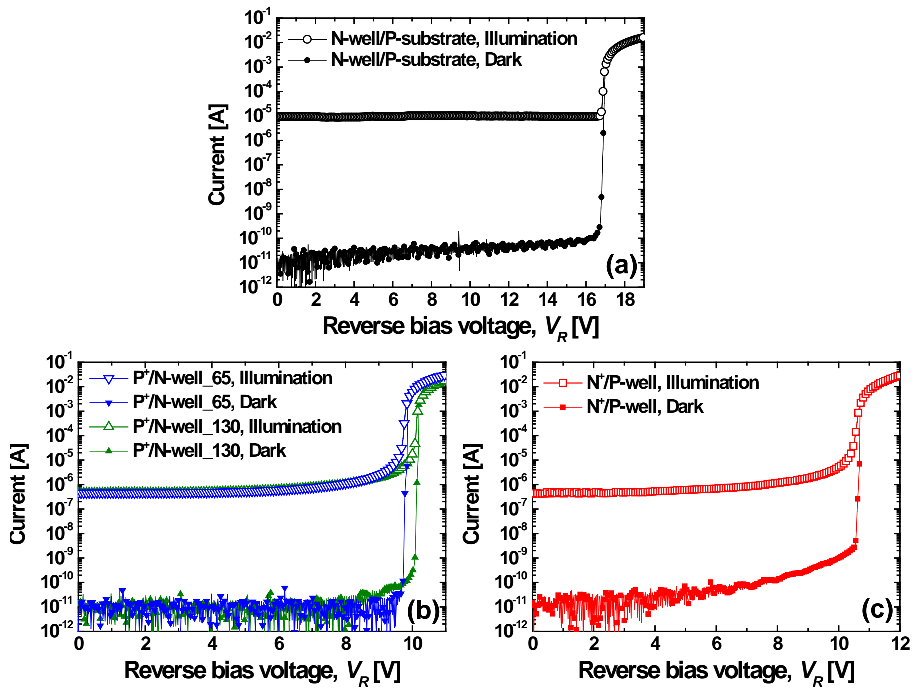


Fig. 5-23. Current-voltage characteristics of the CMOS-APDs under illumination and dark conditions: (a) N-well/P-substrate, (b) P^+/N-well, and (c) N^+/P-well CMOS-APDs.

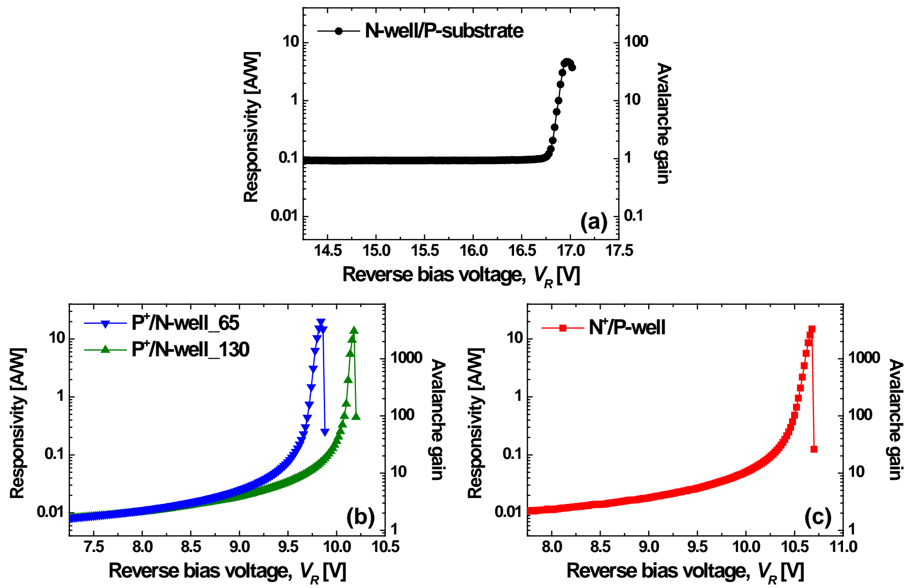


Fig. 5-24. Responsivities and avalanche gains of the CMOS-APDs as a function of the reverse bias voltage: (a) N-well/P-substrate, (b) P^+/N-well, and (c) N^+/P-well CMOS-APDs.

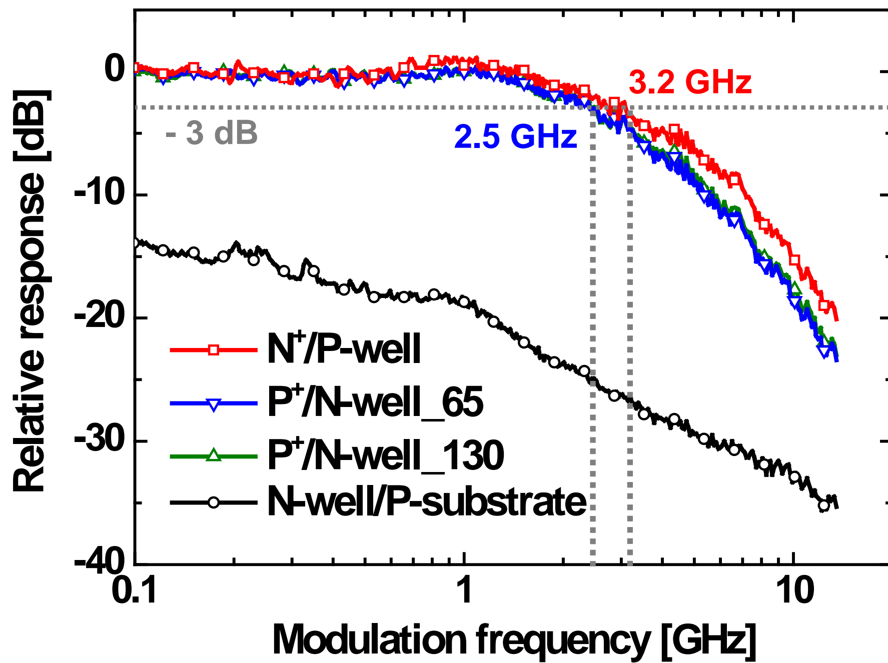


Fig. 5-25. Relative photodetection frequency responses of the CMOS-APDs.

5-5-3. Discussions

Fig. 5-26 shows measured 3-dB bandwidth of the N^+/P-well CMOS-APD as a function of measured avalanche gain. The increase in 3-dB bandwidth for gain larger than about 200 is due to the enhanced peaking effect in the photodetection response [18], [26]. Due to this, the CMOS-APD does not show the decreasing 3-dB bandwidth with the increasing gain as has been observed in other APDs. The maximum gain-bandwidth product achieved is about 1820 GHz with corresponding avalanche gain of 569 and 3-dB bandwidth of 3.2 GHz at the reverse bias voltage of 10.6 V. At this bias, the photogenerated current is about 300 μA and the dark current is about 0.3 μA.

Table 5-5 compares various published results of silicon avalanche photodetectors in standard CMOS technology with this work. The electron-injection-type APD reported by Iiyama et al. [30] has the same junction structure as the CMOS-APD, but the CMOS-APD from this investigation has much better performance due to the STI which allows much higher field across junction before breakdown. To the best of my knowledge, this work achieves the highest gain-bandwidth product reported for silicon photodetectors fabricated with standard CMOS technology.

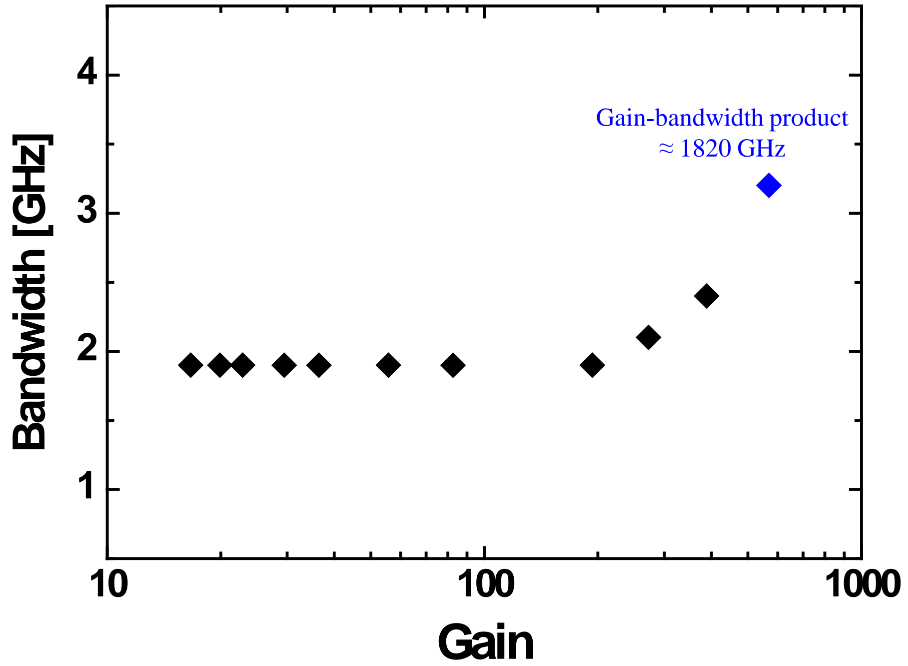


Fig. 5-26. Gain-bandwidth characteristic of the N^+/P-well CMOS-APD.

Table 5-5

PERFORMANCE COMPARISON OF

SILICON AVALANCHE PHOTODETECTORS

FABRICATED WITH STANDARD CMOS TECHNOLOGY

	[16]	[17]*	[30]**		This work
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS		65-nm CMOS
Structure	Multiple p^+-p-n APD	Multiple p^+-p-n APD with body contact	Hole-injection-type APD	Electron-injection-type APD	N^+/P-well APD
R	0.74 A/W	0.085 ~ 0.38 A/W	0.4 ~ 2.2 A/W	0.6 ~ 2.3 A/W	2.94 A/W
M	2	3 ~ 7	45 ~ 260	72 ~ 280	569
BW	1.6 GHz	2.8 ~ 1.4 GHz	2 ~ 0.35 GHz	2.4 ~ 0.65 GHz	3.2 GHz
GBP	3.2 GHz	8.4 ~ 9.8 GHz	90 GHz	180 GHz	1820 GHz

R: responsivity, M: avalanche gain, BW: bandwidth, GBP: gain-bandwidth product
* Estimated from data shown in Fig. 1 and Fig. 2 of ref. 17
** Estimated from data shown in Fig. 3 and Fig. 5 of ref. 30

5-6. Junction-Dependent Characteristics (2)

As mentioned in section 2-1, PN junctions for photodetectors can be implemented by Base/Collector junction in BiCMOS technology. In this section, the performances of the CMOS-APD based on the P^+/N-well junction and the HBT-compatible APD (HBT-APD) based on the P^+ SiGe Base/Collector junction will be compared.

5-6-1. Device Structures

Fig. 5-27 shows the CMOS-APD based on P^+/N-well junction and the HBT-APD based on P^+ SiGe Base/Collector junction fabricated with 0.25-μm standard BiCMOS technology. The junctions have STI GR, and all APDs include STI between P^+ and N^+ regions. Photocurrents are extracted from P^+ ports located inside N-well and Base ports, respectively. The junctions are reverse biased with a positive voltage applied to the N-well and Collector ports, and P^+ and Base ports are grounded. The P^+ port for the P-substrate is tied to ground. For all types, optical windows having the area of 30×30 μm^2 are formed by blocking the salicide process. These APDs can be

realized without violating any design rules for the BiCMOS process technology.

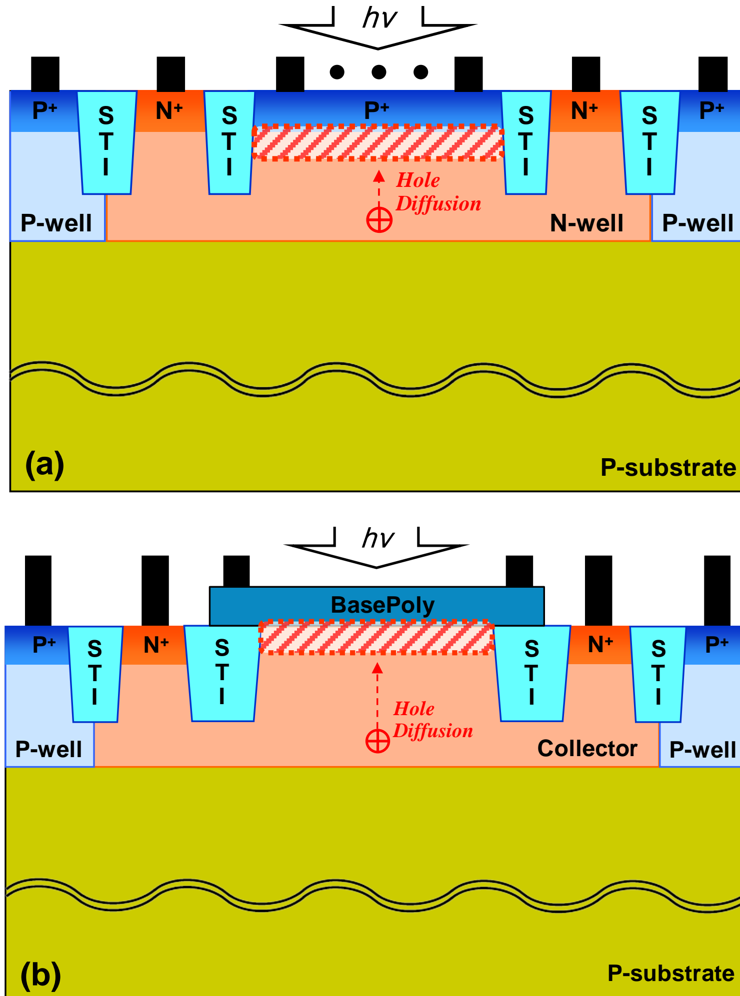


Fig. 5-27. Cross sections of two types of APDs based on (a) P^+/N-well and (b) Base/Collector junctions.

5-6-2. Experimental Results and Discussions

Fig. 5-28 shows measured photodetection frequency responses for the CMOS-APD and HBT-APD at the bias voltage that gives the maximum photodetection frequency response for each type. Both APDs have no appreciable difference in responsivity because the N-well and Collector regions are almost same and STI GR is utilized for each junction [23]. However, the HBT-APD shows lower photodetection bandwidth than the CMOS-APD due to the increase of the hole-diffusion time in Collector. Since the Base region is deposited on the Collector region, the hole-diffusion path in Collector is longer than in N-well as shown in Fig. 5-27.

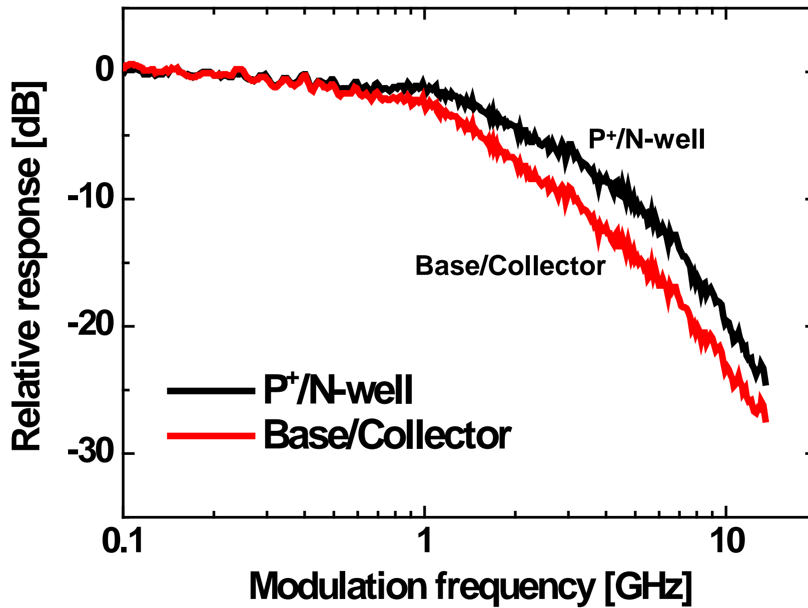


Fig. 5-28. Measured photodetection frequency responses of the CMOS-APD and HBT-APD based on P^+/N-well and Base/Collector junctions, respectively.

6. Considerations about Optimal Conditions for Silicon APDs

In this section, considerations about optimal operating conditions of CMOS-APDs will be investigated, which are the reverse bias voltage and incident optical power. Current-voltage characteristics, responsivities, avalanche gains, electrical reflection coefficients, and photodetection frequency responses of CMOS-APDs will be measured at different bias voltages and incident optical power. Then, the characteristics depending on the reverse bias voltage and incident optical power will be analyzed with equivalent circuit models. From the analyses, factors that influence the CMOS-APD performances will be identified with the goal of achieving the optimal operating conditions.

6-1. Bias-Voltage-Dependent Characteristics

In this section, the effects of bias-voltage conditions on the performance of CMOS-APDs will be discussed. Current-voltage characteristics, responsivities, avalanche gains, electrical reflection coefficients, and photodetection frequency responses of the CMOS-

APD were measured at different bias voltages, and then characteristics of CMOS-APDs were analyzed with the equivalent circuit model. From these investigations, dominant limiting factors that influence the performances of CMOS-APDs will be identified, and then the optimal operating bias-voltage condition will be clarified.

6-1-1. Device Structure and Equivalent Circuit Model

Fig. 6-1 shows the structure of the CMOS-APD based on the P^+/N-well junction. It has optical-window area of $10 \times 10\ \mu m^2$, and the optical window is formed by blocking the salicide process. STI is included between P^+ and N^+ regions. The P^+/N-well junction is reverse biased for photodetection, and the P-substrate port is tied to ground. Photocurrents are extracted from the P^+ port located in the N-well region to exclude the slow diffusion current in the P-substrate region. The CMOS-APD was fabricated with 0.13-μm standard CMOS technology without any design or layout rule violation. More details are mentioned in section 3-1.

Also shown in Fig. 6-1 is an equivalent circuit model for the CMOS-APD. The equivalent circuit model includes an inductor with series

resistor and a parallel resistor and a capacitor for the P^+/N-well junction in the avalanche regime. R_{nw} and C_{sub} represent N-well resistance and N-well/P-substrate junction capacitance, respectively. C_p is parasitic capacitance between N^+ and P^+ electrodes, and Z_{pad} represents the equivalent circuit for the pad and the metal interconnect. f_{tr} represents the 3-dB bandwidth of the current source, which determined by the transit time of photogenerated carriers in the charge-neutral region of N-well and avalanche buildup time. More details are described in section 4-1.

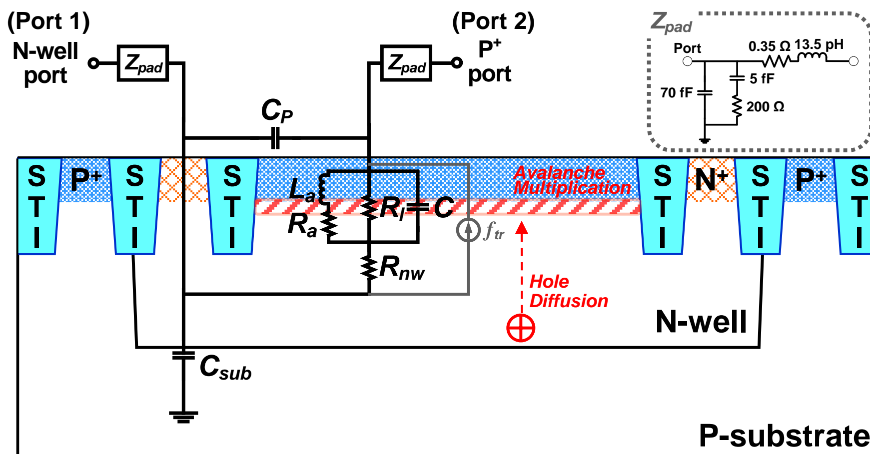


Fig. 6-1. Structure and equivalent circuit model of the fabricated CMOS-APD.

6-1-2. Experimental Results and Analyses With Equivalent Circuit Model

Fig. 6-2 shows measured current-voltage characteristics as well as responsivity and avalanche gain of the fabricated CMOS-APD. The CMOS-APD exhibits low dark currents below a few nA. With the reverse bias voltage approaching the avalanche breakdown voltage, the photogenerated currents start to increase dramatically with internal gain provided by the avalanche multiplication process. Therefore, responsivity dramatically increases at the avalanche regime owing to the high avalanche gain of the CMOS-APD.

Fig. 6-3 shows measured photodetection frequency responses of the CMOS-APD at different bias voltages. As the reverse bias voltage increases, the photodetection frequency response initially increases due to avalanche gain. However, with a too large bias voltage, the low frequency response starts to decrease. Therefore, the optimal bias voltage, 10.25 V for this CMOS-APD, can be easily obtained by photodetection frequency response measurements.

To better understand the effects of bias-voltage conditions on the performance of CMOS-APDs, equivalent circuit models are derived for CMOS-APDs. The parameters of the equivalent circuit models are

extracted from the two-port S-parameter and photodetection frequency response measurements as described in chapter 4. Fig. 6-4 shows measured and simulated electrical reflection coefficients at the P^+ port of the CMOS-APD on Smith chart from 50 MHz to 13.5 GHz at different bias voltages, and Fig. 6-5 shows measured and simulated photodetection frequency responses of the CMOS-APD at the same conditions. These show that the measured and simulated results show good matching. The extracted values of equivalent-circuit parameters for the bias-dependent simulations are listed in Table 6-1. All parameters for Z_{pad} and C_p assumed the same. C, R_{nw}, and C_{sub} should change very little in the range of bias voltages, and they are also assumed the same. Inductance L_a decreases with the reverse bias voltage since it is inversely proportional to the current, and R_a and R_l decrease with the increase of the reverse bias voltage since they tend to reduce along with the increase of the current, which is similar to the results in [27]. At the reverse bias voltage of 10.10 V, the f_{tr} is 6 GHz because the avalanche multiplication time is relatively low. As the reverse bias voltage increases above 10.20 V, the avalanche buildup time increases and has an influence on the transit-time constant, and therefore f_{tr} decreases with the increase of bias voltage.

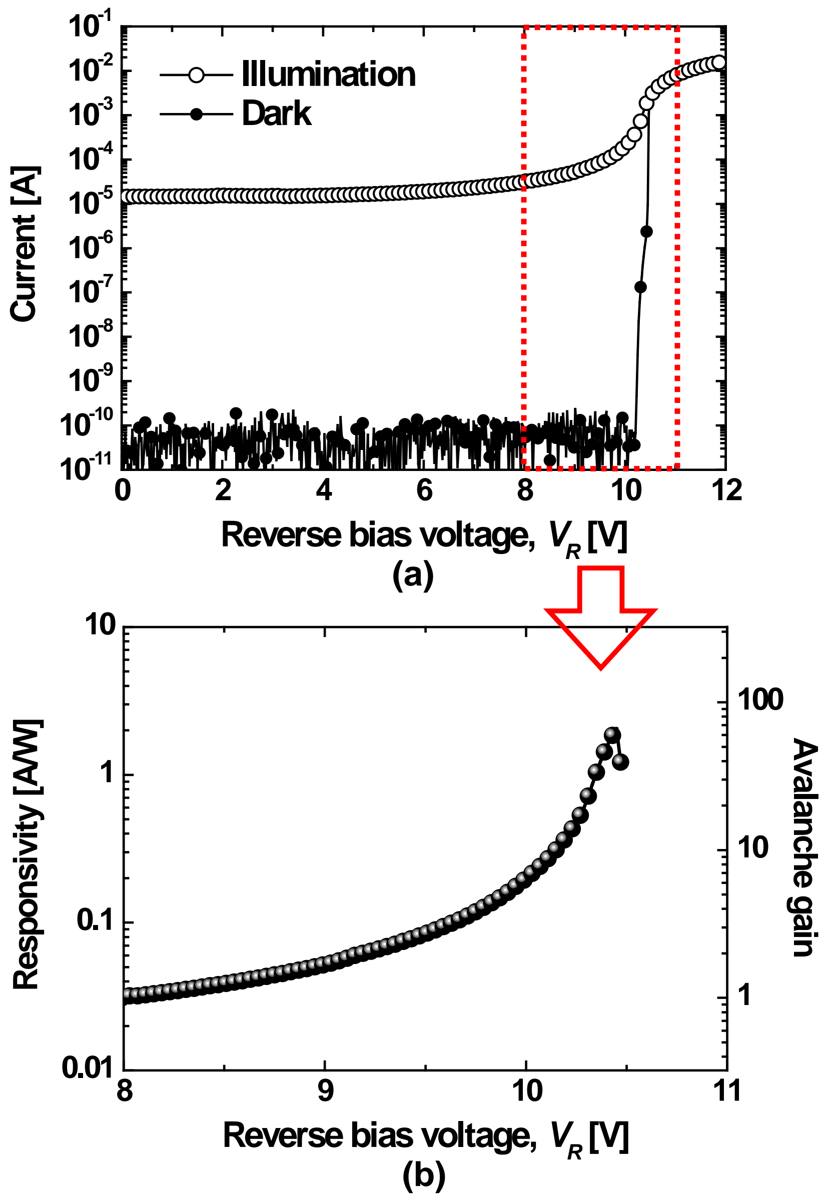


Fig. 6-2. (a) Current characteristics and (b) responsivity and avalanche gain of the CMOS-APD as a function of the reverse bias voltage.

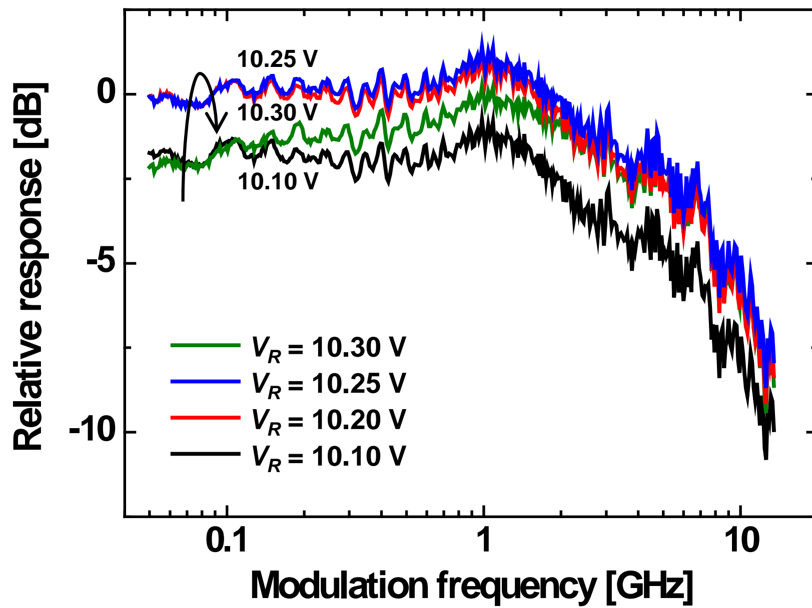


Fig. 6-3. Photodetection frequency responses of the CMOS-APD at different bias voltages.

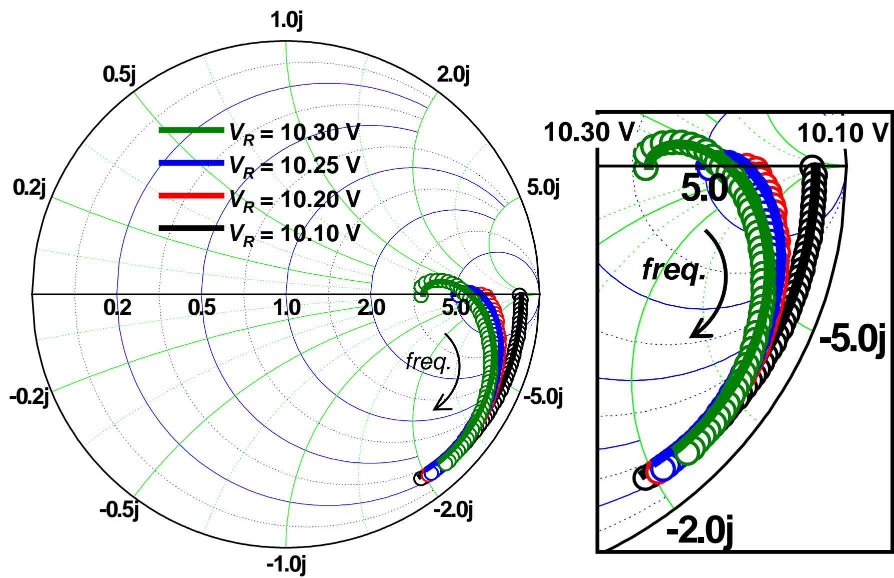


Fig. 6-4. Measured and simulated electrical reflection coefficients of the CMOS-APD from 50 MHz to 13.5 GHz. Hollow circles represent the measured data and solid lines as the simulated results. The inset shows magnified images of the electrical reflection coefficients.

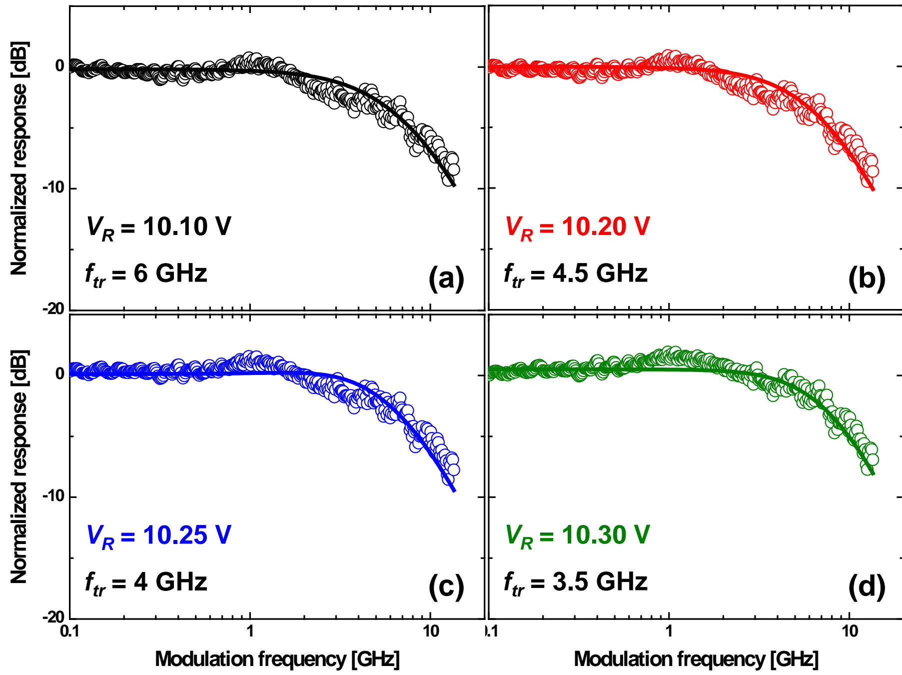


Fig. 6-5. Measured and simulated photodetection frequency responses of the CMOS-APDs. Hollow circles represent the measured data and solid lines as the simulated results.

Table 6-1

EXTRACTED PARAMETERS FOR THE CMOS-APD AT DIFFERENT BIAS VOLTAGES

	10.10 V	10.20 V	10.25 V	10.30 V
L_a [nH]	24.4	16.7	13	6
R_a [Ω]	1800	350	150	60
R_l [kΩ]	4	1.5	1.2	1.1
C [fF]	35			
R_{nw} [Ω]	60			
C_{sub} [fF]	15			
C_p [fF]	20			
f_{tr} [GHz]	6	4.5	4	3.5

6-1-3. Discussions

Fig. 6-6(a) shows the simulated photodetection frequency responses at different bias voltages without the transit-time effect (i.e., no frequency-dependent current source used in simulation). As can be seen in this figure, clear peaking develops when reverse bias voltage becomes large due to the inductive component of avalanche regime. Since the value of L_a decreases with the bias increase, and the peaking frequency is inversely proportional to the square root of inductance, the peaking frequency increases with the bias voltage. One of the most important characteristics of the avalanche inductor is its quality factor, Q_L, which is determined by dividing the imaginary part of the impedance by its real part [31]. In the avalanche regime, there is a resistance in series with the inductor, and it affects the inductor quality factor, producing a lower peak. Fig. 6-6(b) shows simulated values of inductor quality factors for four bias conditions. The inductor quality factor at the reverse bias voltage of 10.10 V is still very low in the GHz frequency range due to the high series resistance, R_a, of the avalanche regime, resulting in no peak as shown in Fig. 6-6(a). However, as the reverse bias voltage increases, the quality factors become larger in the GHz frequency range, producing the higher peak, because the L_a / R_a

ratio becomes larger with the bias voltage as shown in the inset of Fig. 6-6(b). Consequently, at the reverse bias voltage above 10.20 V, the photodetection bandwidth of the CMOS-APD can become larger than that at the reverse bias voltage of 10.10 V with the inductive-peaking effect in spite of the lower f_{tr}.

Fig. 6-7 shows photodetection frequency responses of the CMOS-APD for all the factors, RLC components, and photogenerated-carrier transit time at different bias voltages. It is obvious that the photogenerated-carrier transit time is a photodetection bandwidth limiting factor because photogenerated carriers outside the depletion region must diffuse to the junction, resulting in considerable time delay. In addition, we can clearly see that the photodetection bandwidth of the CMOS-APD is actually better than the speed limitation of the transit time due to the inductive-peaking effect in the CMOS-APD. Moreover, it can be observed that with the increase of bias voltage, the photodetection bandwidth becomes larger with the high inductive-peaking effect at higher peaking frequency in spite of lower f_{tr}.

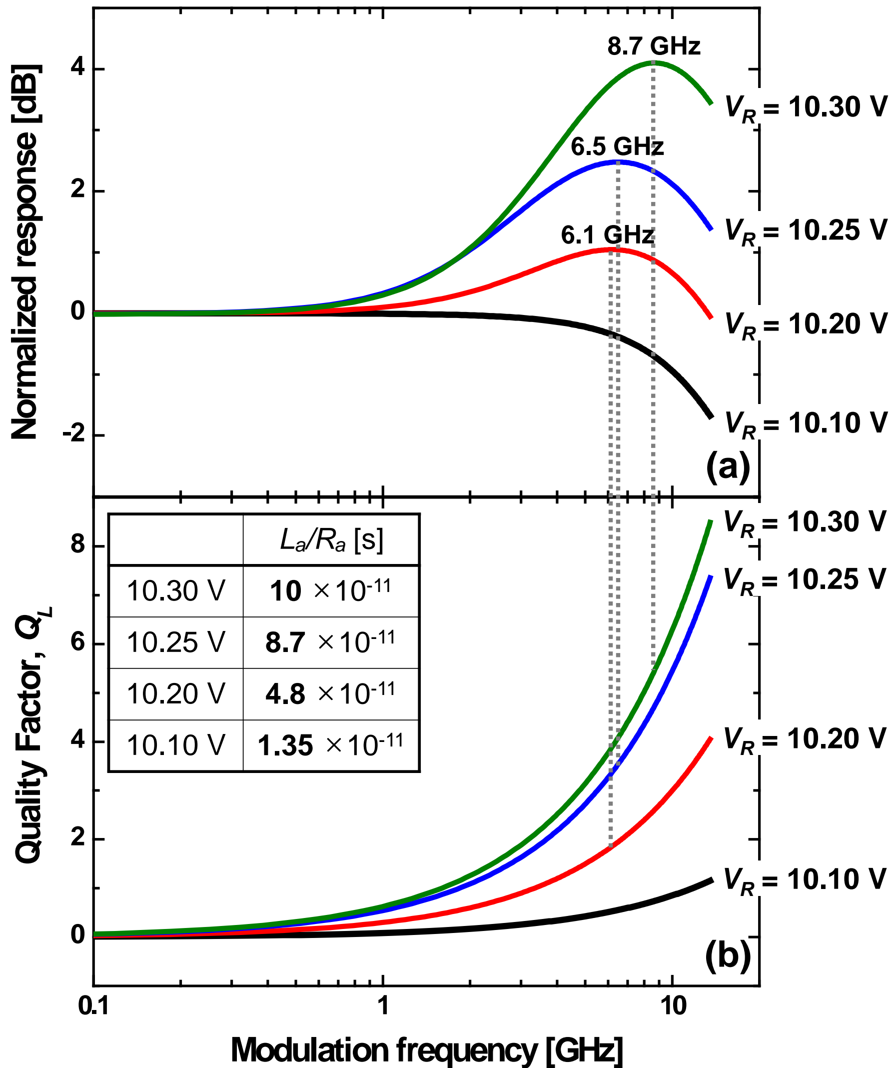


Fig. 6-6. (a) Normalized photodetection frequency responses without the photogenerated-carrier transit time and (b) inductor quality factors as a function of the frequency for the CMOS-APD at different bias voltages.

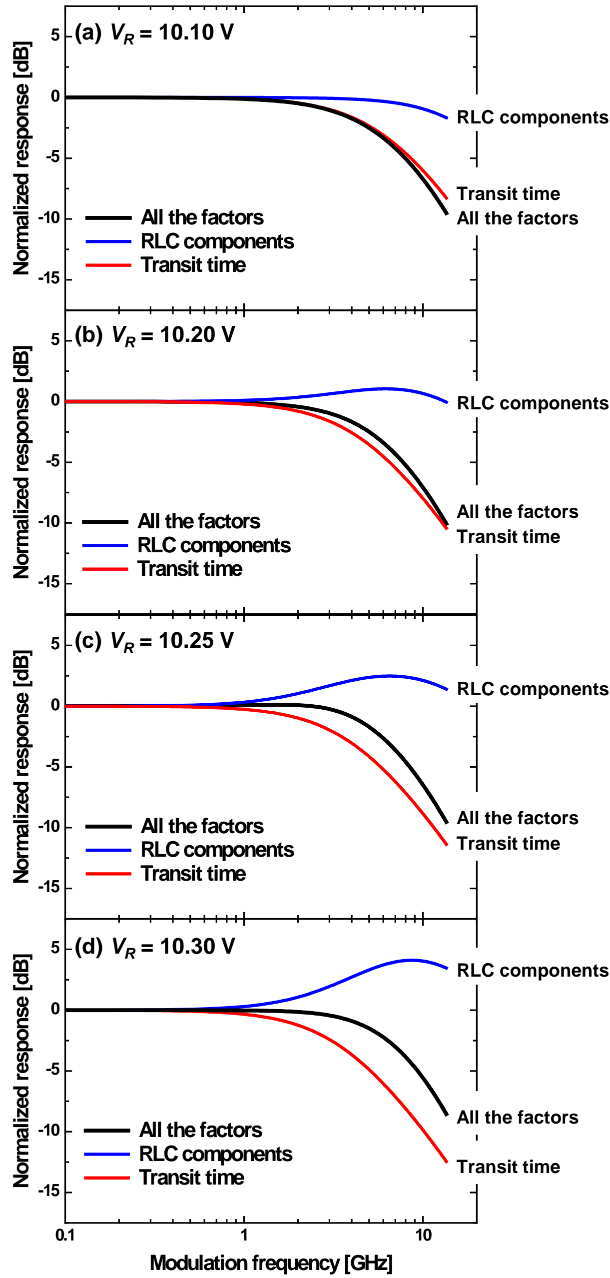


Fig. 6-7. Simulated photodetection frequency responses of the CMOS-APD for photogenerated-carrier transit time, RLC components, and all the factors according to bias voltages.

6-2. Optical-Power-Dependent Characteristics

In this section, the effects of optical-power conditions on the performance of CMOS-APDs will be discussed. Current-voltage characteristics, responsivities, avalanche gains, electrical reflection coefficients, and photodetection frequency responses of the CMOS-APD were measured at different optical power, and then characteristics of CMOS-APDs were analyzed with the equivalent circuit model. From these investigations, dominant limiting factors that influence the performances of CMOS-APDs will be identified, and then the optimal operating optical-power condition will be clarified.

6-2-1. Device Structure and Equivalent Circuit Model

Fig. 6-8 shows the structure of the CMOS-APD based on the P^+/N-well junction. It has optical-window area of $10 \times 10\ \mu m^2$, and the optical window is formed by blocking the salicide process. STI is included between P^+ and N^+ regions. The P^+/N-well junction is reverse biased for photodetection, and the P-substrate port is tied to ground. Photocurrents are extracted from the P^+ port located in the N-well

region to exclude the slow diffusion current in the P-substrate region. The CMOS-APD was fabricated with 0.25-μm standard CMOS technology without any design or layout rule violation. More details are mentioned in section 3-1.

Also shown in Fig. 6-8 is an equivalent circuit model for the CMOS-APD. The equivalent circuit model includes an inductor with series resistor and a parallel resistor and a capacitor for the P^+/N-well junction in the avalanche regime. R_{nw} and C_{sub} represent N-well resistance and N-well/P-substrate junction capacitance, respectively. C_p is parasitic capacitance between N^+ and P^+ electrodes, and Z_{pad} represents the equivalent circuit for the pad and the metal interconnect. f_{tr} represents the 3-dB bandwidth of the current source, which determined by the transit time of photogenerated carriers in the charge-neutral region of N-well and avalanche buildup time. More details are described in section 4-1.

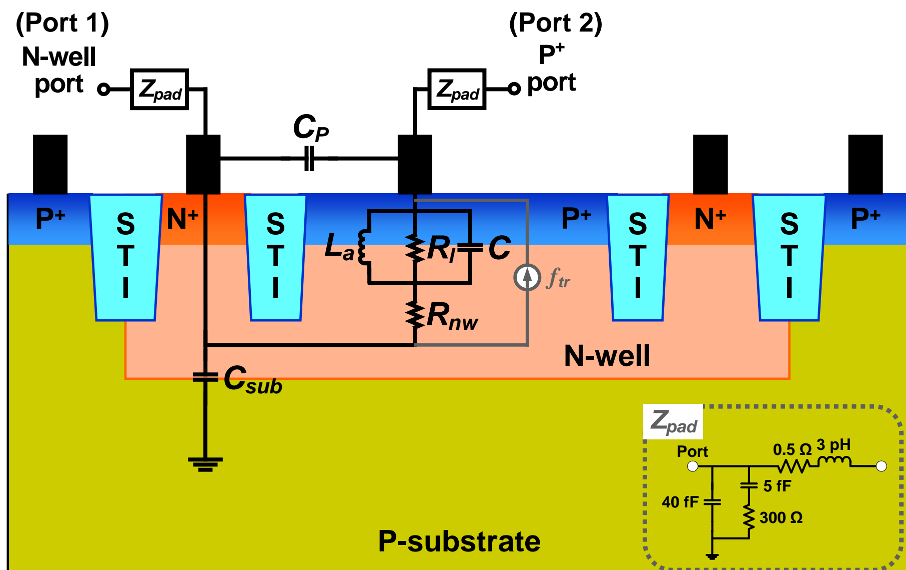


Fig. 6-8. Structure and equivalent circuit model of the fabricated CMOS-APD.

6-2-2. Experimental Results and Analyses With Equivalent Circuit Model

Fig. 6-9 shows measured current-voltage characteristics as well as responsivity and avalanche gain of the fabricated CMOS-APD at different incident optical power. As shown in this figure, photogenerated currents decrease linearly with reduced optical power. However, at the avalanche range, responsivity and avalanche gain increase with reduced optical power, because the currents are saturated at the same level. Therefore, much higher responsivity is obtained at the lower incident optical power.

Fig. 6-10(a) shows measured photodetection frequency responses of the CMOS-APD at different bias voltages when the incident optical power is 1 mW. For this CMOS-APD, the optimal bias voltage is about 12.3 V. Fig. 6-10(b) shows measured photodetection frequency responses of the CMOS-APD at optimal bias voltage according to the incident optical power. In general PD, when the optical power is dropped to its -10 dB, the corresponding electrical power is dropped to its -20 dB, because the photocurrent is proportional to optical power, and electrical power is proportional to the square of the current. However, the CMOS-APD shows higher response with the decrease of

incident optical power due to increased avalanche gain. When the optical power is dropped to its -10 dB, the corresponding electrical power is dropped to its -12 dB, and when the optical power has dropped to its -20 dB, the corresponding electrical power is dropped to its -32 dB. On the other hand, the photodetection bandwidth is decreased from 4.7 GHz to 2.2 GHz with the decrease of incident optical power as shown in Fig. 6-10(c).

To better understand the effects of optical-power conditions on the performance of CMOS-APDs, equivalent circuit models are derived for CMOS-APDs. The parameters of the equivalent circuit models are extracted from the two-port S-parameter and photodetection frequency response measurements as described in chapter 4. Fig. 6-11 and Fig. 6-12 show measured and simulated electrical reflection coefficients and photodetection frequency responses of the CMOS-APD, respectively, at optimal bias voltage according to the incident optical power. The measured and simulated results show good matching. The extracted values of equivalent-circuit parameters for the optical-power-dependent simulations are listed in Table 6-2. All parameters for Z_{pad} and C_p assumed the same, and R_l, C, R_{nw}, and C_{sub} should change very little at the optimal bias condition with the decrease of incident optical power. On the other hand, L_a increases due to decreased photocurrents, and f_{tr}

decreases due to increased avalanche buildup time.

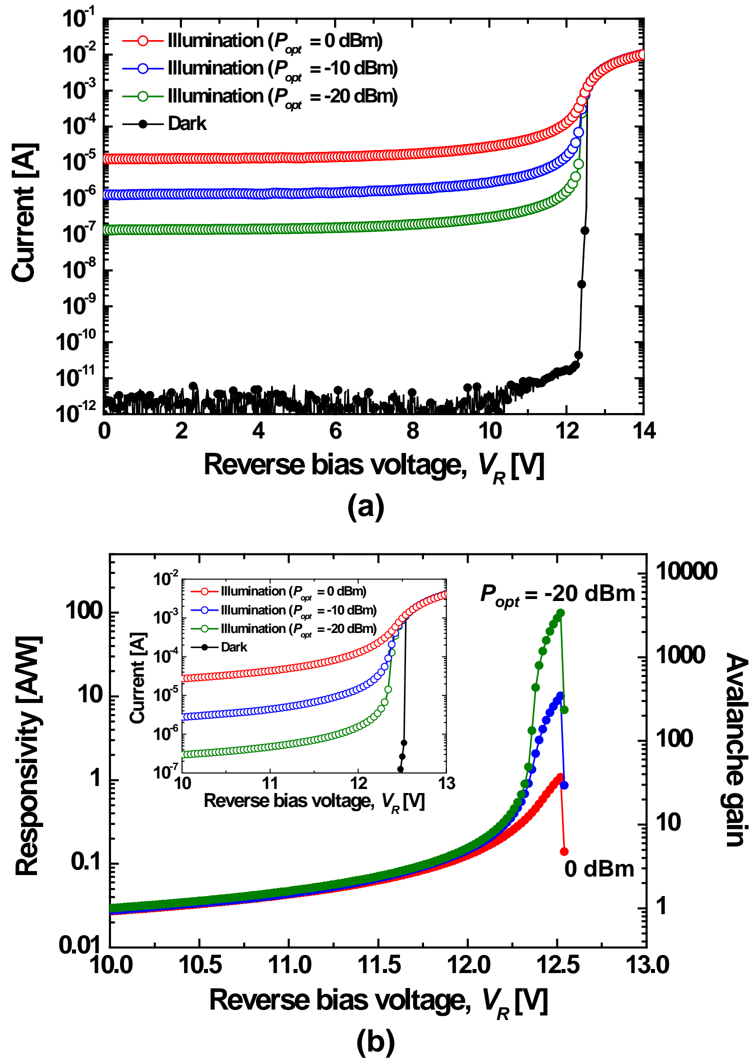


Fig. 6-9. (a) Current characteristics and (b) responsivity and avalanche gain of the CMOS-APD as a function of the reverse bias voltage at different incident optical power.

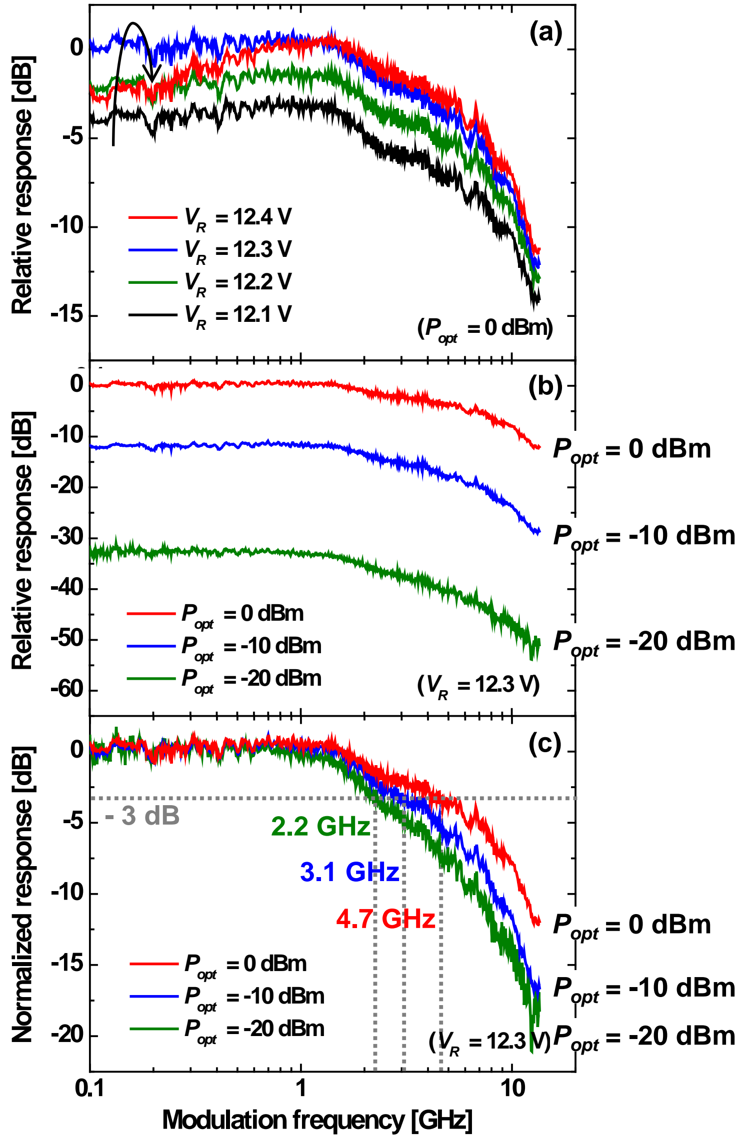


Fig. 6-10. (a) Photodetection frequency responses of the CMOS-APD at different bias voltages when the incident optical power is 0 dBm. (b) Photodetection frequency response of the CMOS-APD at different incident optical power when the reverse bias voltage is 12.3 V. (c) Normalized response of the CMOS-APD at different incident optical power when the reverse bias voltage is 12.3 V.

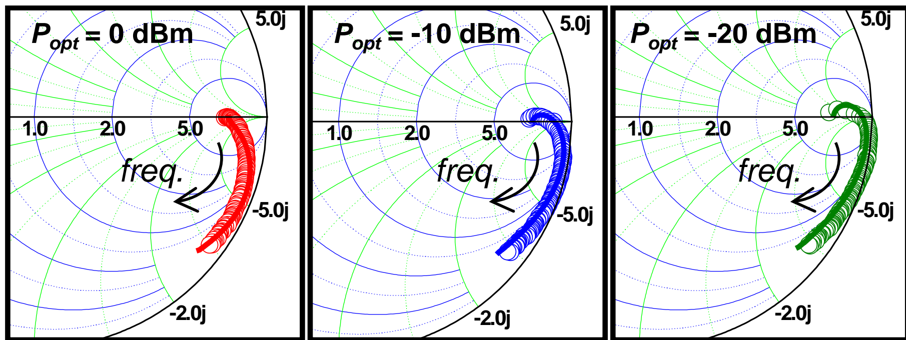


Fig. 6-11. Measured and simulated electrical reflection coefficients of CMOS-APDs from 50 MHz to 13.5 GHz at different incident optical power when the reverse bias voltage is 12.3 V. Hollow circles and solid lines represent measured data and simulated results, respectively.

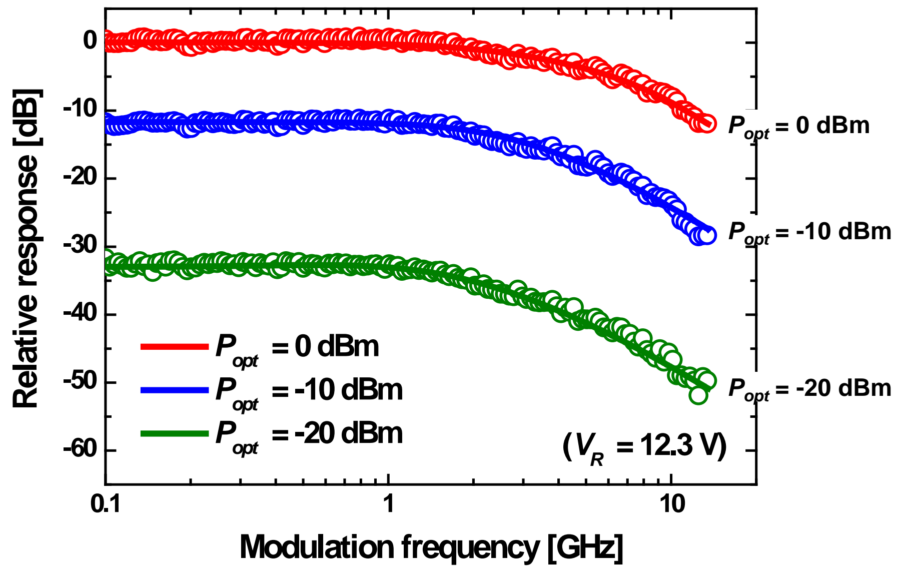


Fig. 6-12. Measured and simulated photodetection frequency responses of the CMOS-APD at different incident optical power when the reverse bias voltage is 12.3 V. Hollow circles represent measured data, and solid lines represent simulated results.

Table 6-2

EXTRACTED PARAMETERS FOR THE CMOS-APD
AT DIFFERENT INCIDENT OPTICAL POWER

	P_{opt} = 0 dBm	P_{opt} = -10 dBm	P_{opt} = -20 dBm
L_a [nH]	15	55	130
R_l [kΩ]		5	
C [fF]		21	
R_{nw} [Ω]		500	
C_{sub} [fF]		25	
C_p [fF]		35	
f_{tr} [GHz]	3.5	2.3	1.8

6-2-3. Discussions

Fig. 6-13 shows photodetection frequency responses of the CMOS-APD for all the factors, RLC components, and photogenerated-carrier transit time according to incident optical power. It can be observed that the photogenerated-carrier transit time is a photodetection bandwidth limiting factor, and the photodetection bandwidth becomes smaller with the decrease of incident optical power due to decreased f_{tr} because of increased avalanche buildup time. Despite this limitation, however, higher bandwidth than the limitation of the f_{tr} is achieved because of the decreased inductive-peaking frequency due to the increased L_a.

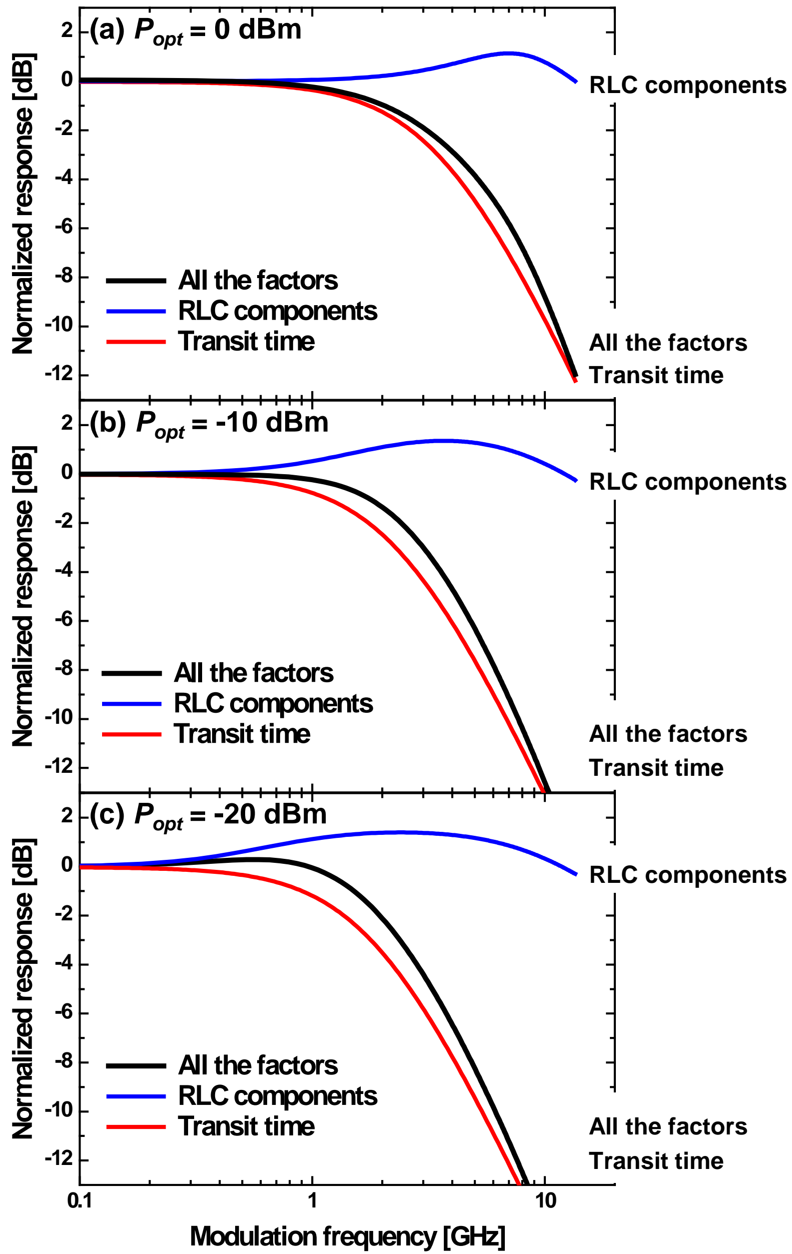


Fig. 6-13. Simulated photodetection frequency responses of the CMOS-APD for photogenerated-carrier transit time, RLC components, and all the factors according to incident optical power.

7. Summary

In this dissertation, high-performance silicon APDs are developed in standard CMOS/BiCMOS technology. For the goal of identifying the factors that influence the APD performances and realizing the optimal CMOS-APD, various types of CMOS-APDs having different GR, electrode, silicide, area, and junction structures realized in several standard CMOS/BiCMOS technologies are compared and analyzed. Their current-voltage characteristics, responsivities, avalanche gains, electrical reflection coefficients, and photodetection frequency responses are measured and analyzed. It is demonstrated that the CMOS-APD with STI GR can provide the largest electric field at the planar junction, and consequently, provides the maximum avalanche gain. Furthermore, it is clarified that only a few electrodes are needed for the optical window of the CMOS-APD because they give better responsivity without degradation of photodetection-bandwidth performance due to better optical injection and the dominant bandwidth limiting factor of the hole-diffusion time in N-well, respectively. In addition, it is clearly observed that the CMOS-APD having silicide under output contacts can utilize the inductive-peaking effect, which brings higher photodetection-bandwidth performance, while the

CMOS-APD without silicide cannot utilize the inductive-peaking effect. Also, by reducing the device area up to $10 \times 10\,\mu m^2$, the photodetection bandwidth of the CMOS-APD is enhanced to 7.6 GHz due to the decreased transit time and higher inductive-peaking frequency. Moreover, it is demonstrated that P^+/N-well and N^+/P-well CMOS-APDs have much better photodetection bandwidth performances than the N-well/P-substrate CMOS-APD, and the N^+/P-well CMOS-APD has higher bandwidth than the P^+/N-well CMOS-APD because electrons move faster in P-well than holes in N-well. Furthermore, it is observed that the HBT-APD based on P^+ SiGe Base/Collector junction shows lower photodetection bandwidth than the CMOS-APD based on P^+/N-well junction due to the increase of the hole-diffusion time in Collector. From these investigations, the optimized CMOS-APD shows the highest gain and photodetection bandwidth performances among CMOS-compatible photodetectors reported until now. Table 7-1 shows overview of design considerations for performance enhancement of the APDs.

With the optimized CMOS-APD, optimal operating conditions of CMOS-APDs are investigated, which are the reverse bias voltage and incident optical power. Current-voltage characteristics, responsivities, avalanche gains, electrical reflection coefficients, and photodetection

frequency responses of CMOS-APDs are measured at different bias voltages and incident optical power. Then, the characteristics depending on the reverse bias voltage and incident optical power are analyzed with equivalent circuit models. From the analyses, it is obvious that with the increase of bias voltage, the photodetection bandwidth becomes larger with the high inductive-peaking effect at higher peaking frequency in spite of lower f_{tr}. In addition, it can be observed that the photodetection bandwidth becomes smaller with the decrease of incident optical power due to decreased f_{tr} because of increased avalanche buildup time and higher bandwidth than the limitation of the f_{tr} is achieved because of the decreased inductive-peaking frequency due to the increased L_a. From these investigations, dominant factors that influence the CMOS-APD performances are identified, and then the optimal operating conditions are clarified.

The high-performance CMOS-APD developed by optimizing several considerations can allow over 10-Gb/s CMOS integrated optical receivers. It is expected that the high-performance CMOS-APD can play an important role in silicon-photonics applications to achieve cost reduction of systems by enabling monolithic electronic-photonic integrated circuits based on the mature CMOS technology. In addition, the equivalent-circuit analysis can be very useful for realizing and

understanding monolithically integrated optical receivers having germanium avalanche photodetectors as well as silicon avalanche photodetectors.

Table 7-1
OVERVIEW OF DESIGN CONSIDERATIONS
FOR SILICON-APD-PERFORMANCE ENHANCEMENT

Design Considerations	***Test Structures***	***Best Structures***	***Enhanced Performance***
Guard Ring	w/o GR, P-well GR P-sub GR, STI GR	**STI GR**	Avalanche gain, Responsivity
Electrode	1.3-μm, 9.6-μm spacing multi-finger electrodes	**9.6-μm spacing multi-finger electrodes**	Responsivity
Silicide	w/o silicide, w/ silicide under output contacts	**w/ silicide under output contacts**	Responsivity, Photodetection bandwidth
Area	10 × 10, 20 × 20, 30 × 30, 40 × 40 μm^2	**10 × 10 μm^2**	Photodetection bandwidth
Junction	N-well/P-substrate, P^+/N-well, N^+/P-well	**N^+/P-well**	Avalanche gain, Responsivity, Photodetection bandwidth
Junction	P^+/N-well, Base/Collector	**P^+/N-well**	Photodetection bandwidth

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Awards

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[2] ***IEEE Student Paper Contest*** (**Grand Paper Award**): "Determination of Photodetection Bandwidth Limiting Factors in CMOS-Compatible Avalanche Photodetectors With Equivalent-Circuit Analysis," IEEE Seoul Section, Dec. 2012.

[3] ***Yonsei University Best Paper Award***: "Effects of Guard-Ring Structures on the Performance of Silicon Avalanche Photodetectors Fabricated With Standard CMOS Technology," Yonsei University, Seoul, Korea, May 2012.

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