An Analog/Digital Hybrid Phase-Locked Loop Circuit having Optimum Loop Dynamics over Wide Frequency Range

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An Analog/Digital Hybrid Phase-Locked Loop Circuit having Optimum Loop Dynamics over Wide Frequency Range

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ABSTRACT

An Analog/Digital Hybrid Phase-Locked Loop Circuit having Optimum Loop Dynamics over Wide Frequency Range

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Phase-locked loops (PLLs) are used to generate clock signals in various fields including communications, controls, instrumentations, sensors and system-on-chips (SoCs). They are traditionally designed using charge-pump-based analog circuits. Recently, as semiconductor technology advances and fabrication process become very suitable for digital design, all-digital PLLs (ADPLLs) are replacing traditional analog PLLs in several applications. However, conventional ADPLLs have some limits. First, a wide frequency range is hard to be realized without several complex digital-to-analog converters (DACs) for a digitally-controlled oscillator (DCO). Second, a wide-range DCO is usually imple-

mented using a multi-band tuning with an automatic frequency calibration (AFC) technique, which guarantees monotonicity only for a narrow fine-tuning range. It induces a risk that phase-lock can be broken when the fine tuning loop runs out of the narrow range. Third, loop dynamics are not free from process, voltage, and temperature (PVT) variations because the DCO characteristics are very sensitive to PVT.

In this dissertation, a novel analog/digital dual-loop PLL architecture is proposed. In the main digital loop, DCO has a high resolution for the PLL jitter performance, but has a very narrow frequency range for simple implementation. Insufficient DCO frequency range is greatly improved with assistance from a simple analog AFC. As a result, a very wide frequency range can be realized without any complex DACs. Moreover, the proposed DCO has a frequency gain which is proportional to the oscillation frequency, making the PLL dynamics adaptive to the frequency dividing ratio variation. A prototype PLL chip is implemented in 180-nm CMOS technology. The implemented DCO can provide a very wide frequency range from 15MHz to 1.88GHz even though the DCO control code has only 5 bits. It is equivalent to the conventional 12-bit DCO. It is also verified that the implemented PLL can operate within a very wide output frequency range from 50MHz to 1.6GHz without any calibration circuit for loop stabilization.

However, unfortunately, the implemented PLL shows an abnormal behavior that the main digital loop is turned off unintentionally due to the DCO frequency drift. How to solve this problem is proposed in the last part of this dissertation with behavioral verifications. Furthermore, an improving method of making the PLL additionally adaptive to PVT variations and the reference frequency variation is also proposed. For this, a simple resolution calibrator circuit for a time-to-digital converter is proposed. As a result, the

improved PLL can always have an optimum loop dynamics without any possibility for instability, which are insensitive to PVT, the dividing ratio, and the reference frequency variations.

Key words : Phase-locked loop, all-digital phase-locked loop, automatic frequency calibration, wide output frequency range, loop dynamics optimization

Chapter 1

Introduction

Phase-locked loops (PLLs) are used to generate clock signals that are phase-locked by the external input signals, such as reference clock signals. They are essential in various fields including communications, controls, instrumentations, sensors and system-on-chips (SoCs). Especially, PLLs in SoC applications are becoming more significant because SoC market size keeps increasing. Global Industry Analysts (GIA), Inc. reported that the global SoC market will reach US$48.8 billion by 2017 [1].

The key design issues for PLLs in SoCs are summarized below:

1. PLL chip area occupation should be minimized in order to be easily amenable to integration. Therefore, LC-type oscillators are unsuitable for PLLs in SoCs.

2. PLL output frequency range should be wide. Many SoC applications such as interface circuits, memories or micro-processors require a broad operation frequency range. The PLL used for these applications should cover the mandatory frequency range even if process, voltage and temperature (PVT) conditions are varied.

3. PLL dynamics such as loop bandwidth, jitter peaking and stability should be in-

sensitive to PVT variations. As CMOS technology advances, the power supply voltage becomes smaller, and PVT variations can have more serious influences on the circuit analogue characteristics [2], which should be minimized as much as possible.

4. PLL should have a good immunity to supply noises because large current spikes in SoC environments produce large power supply noises.

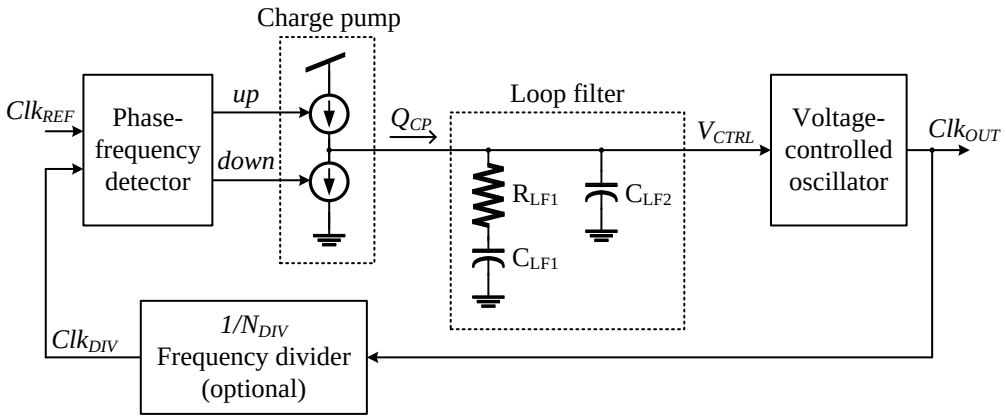
5. Fundamental PLL performances such as power consumption, phase noises and reference spurs should be optimized.

Conventional PLLs for SoCs can be categorized into two groups; PLLs based on mixed-signal circuits, called mixed-signal PLLs (MSPLLs), and PLLs working with digital signals, called all-digital PLLs (ADPLLs). MSPLLs have been widely used in the past decades. Recently, as CMOS technology advances and fabrication processes become very suitable for digital design, ADPLLs are replacing traditional MSPLLs in several applications. In this chapter, the two types of PLLs are briefly described considering the design issues mentioned above, and the goal and outline of this dissertation are given.

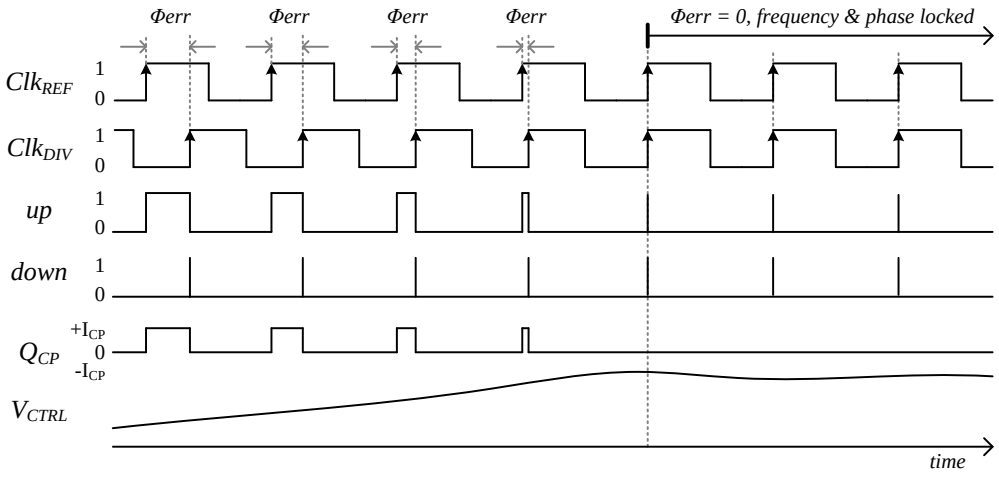
1.1 Mixed-Signal PLLs

The most widely used MSPLLs are based on phase-frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO) and frequency divider (FD) as shown in Figure. 1.1(a), which are called charge pump PLLs (CPPLLs) [3]. Note that FD is required only when the PLL is expected to work as a frequency synthesizer.

The PLL locking process is graphically summarized in Figure. 1.1(b). PFD compares two input clock phases (Clk_{REF}, Clk_{DIV}) and generates two pulses ($up, down$). The pulse width difference between up and $down$ pulses is equal to the phase error (Φ_{err}) between Clk_{REF} and Clk_{DIV}. CP generates a current pulse signal (Q_{CP}) having an amplitude of I_{CP} corresponding to PFD output pulses. LF accumulates the CP output and make a control voltage, V_{CTRL}. VCO produces a clock signal (Clk_{OUT}) having a frequency which is proportional to V_{CTRL} with gain of K_{VCO}. FD receives Clk_{OUT} and generates a clock signal (Clk_{DIV}) whose period is N_{DIV} times of the Clk_{OUT} period. By the negative feedback, the phase error between Clk_{REF} and Clk_{DIV} converges to zero, and the frequency and phase of the PLL output signal (Clk_{OUT}) are locked to the reference signal (Clk_{REF}), where the output frequency is multiplied by N_{DIV} from the reference frequency.



(a)



(b)

Figure 1.1: (a) Block-diagram, (b) locking process of CPPLLs

CPPLLs have been traditionally used due to its structural simplicity. It does not require a high-gain high-linear OP-amp for a voltage integrator. Furthermore, realizing the wide output frequency range is relatively easy because a wide-tuning-range VCO can be easily implemented. However, CPPLLs have several limitations making it unsuitable for recent advanced CMOS technologies as explained below:

1. The burden of LF chip area has been growing because LF passive components are hard to be scaled down. For example, Figure. 1.2 shows a conventional CPPLL chip layout implemented in 130nm CMOS process. It synthesizes 400-MHz clock from 12.5-MHz reference clock. The core area contains all PLL circuits except LF, and LF occupies most of total chip area due to low reference frequency.

2. LF capacitors are often realized with MOS-FET capacitors (MOSCAPs). However, for large capacitance, MOSCAPs are designed using thin gate-oxide, having large gate-tunneling leakage currents in the advanced CMOS technologies [4]. The influence of the leakage current on CPPLLs can be expressed as two static currents, I_{leak1} and I_{leak2} in Figure. 1.3(a). In the locked-state, VCO control voltage (V_{CTRL}) decreases until the next reference clock arrives, inducing large V_{CTRL} ripples as shown in Figure. 1.3(b), and degrading PLL jitter performance. This problem becomes more serious with a lower reference frequency. The use of metal-insulator-metal (MIM) capacitors or vertical natural capacitors [5] can resolve the problem, but they require a much lager chip area than MOSCAPs.

3. Because CP charging and discharging currents (Q_{CP_UP} and Q_{CP_DN}) are generated by PMOS and NMOS, respectively, they have different switching time [6].

It can be expressed as a delay mismatch between up and $down$ signals ($2\Delta_D$) in Figure. 1.3(a). This switching time mismatch produces a static phase offset and V_{CTRL} ripples as shown in Figure. 1.3(c), inducing the PLL reference spur.

4. Like the timing mismatch mentioned above, the current amplitude mismatch between Q_{CP_UP} and Q_{CP_DN}, which is expressed as $2\Delta_{CP}$ in Figure. 1.3(a), produces a static phase offset and V_{CTRL} ripples as shown in Figure. 1.3(d). In general, the current mismatch induces larger reference spurs than the timing mismatch.

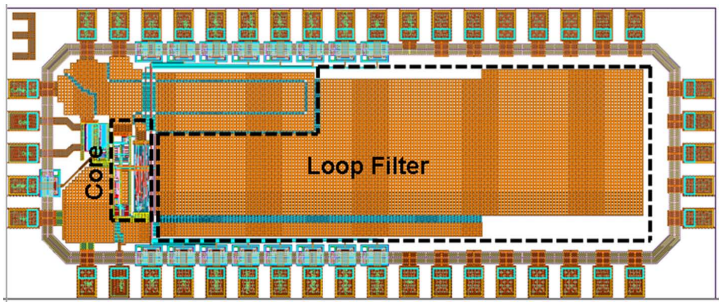


Figure 1.2: Conventional CPPLL layout example

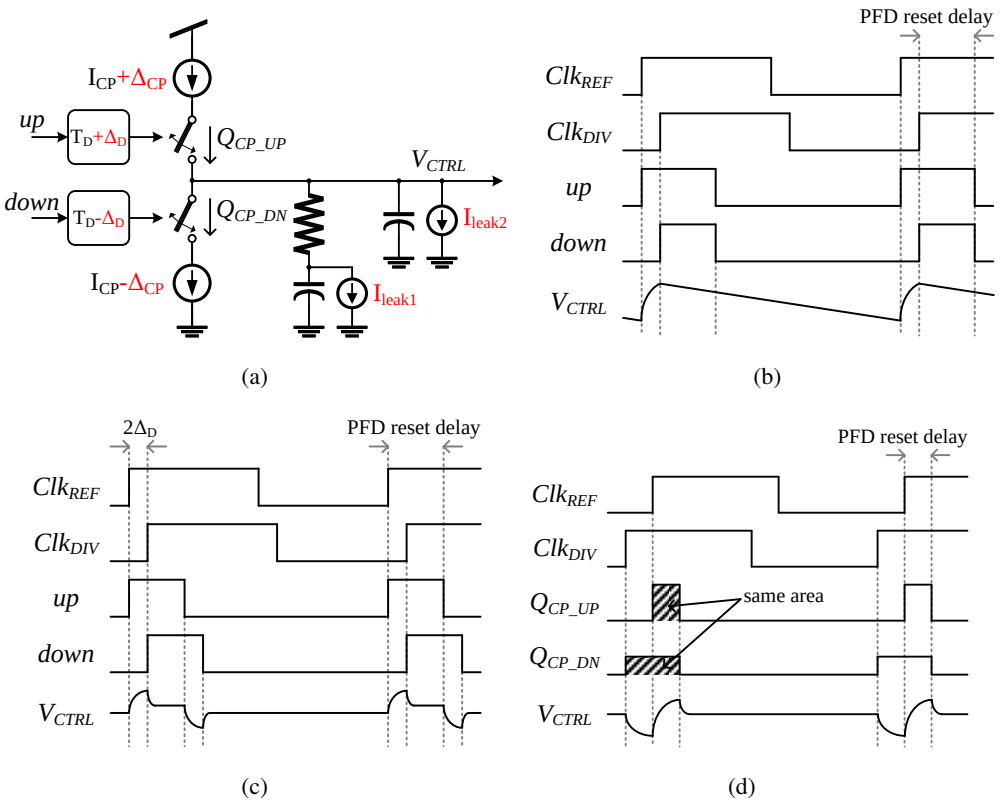


Figure 1.3: (a) CPPLL non-ideality model, effect of (b) gate-tunneling leakage current, (c) timing mismatch, (d) current mismatch

1.2 All-Digital PLLs

Compared with CPPLLs, the most important features of ADPLLs are that the analog LF in CPPLLs is replaced by a digital loop filter (DLF), and all the analog signals in CPPLLs such as Q_{CP} and V_{CTRL} are digitized [7]. For these, CP is replaced by a time-to-digital converter (TDC) which converts Φ_{err} to a digital signal (C_{TDC}), and VCO is replaced by a digitally-controlled oscillator (DCO) which is corresponding a digital signal (C_{DCO}) as shown in Figure. 1.4.

Recently, ADPLLs are replacing traditional CPPLLs rapidly because they have several advantages over CPPLLs as summarized below:

1. ADPLLs do not require large passive components that occupy a large chip area. Therefore, ADPLLs are much suitable to be integrated with recent CMOS processes than CPPLLs.

2. DLF can resolve such problems of CPPLLs mentioned above as leakage currents, timing mismatch, and current mismatch.

3. DLF has inherent noise immunity of digital circuits.

4. Figure. 1.5 shows the ADPLL small-signal loop dynamics model [8], where T_{REF} is the inverse of the reference frequency, Δ_{TDC} is the TDC resolution in time and K_{DCO} is the DCO gain in Hz/code. As opposed to CPPLLs, the reference frequency influences the loop dynamics. Therefore, the PLL design of which loop dynamics are adaptive to the reference frequency variation is possible.

5. Except K_{DCO}, all the circuit parameters such as Δ_{TDC} and $Z(s)$ for the PLL dynamics can be insensitive to PVT variations.

However, ADPLLs also have some limitations. First, wide-range DCOs are hard to realize. In contrast with VCOs having continuous frequency controllability, DCOs have quantized frequencies, which causes orbit-cycling through a few frequencies around the intended frequency, and the PLL peak-to-peak jitter is bounded as shown in Figure. 1.6. Consequently, DCO resolution should be very fine in order to achieve good jitter performance. However, the DCO having fine resolution over wide tuning range is hard to realize simply because it requires too many control bits. Moreover, monotonically increasing frequency according to the control signal (C_{DCO}) over a wide range is very difficult. Therefore, the wide-range DCO is usually implemented using a multi-band tuning with an automatic frequency calibration (AFC) technique, which guarantees monotonicity only for a small range as shown in Figure. 1.7(a) [9]. However, there is a risk that phase-lock can be broken because DCO characteristics can be changed by voltage and temperature variations depending on time. Figure. 1.7(b) shows an example of DCO curve variation. As time changes from t_0 to t_1, C_{DCO} moved from $C_{DCO}@t_0$ to $C_{DCO}@t_1$ for the target frequency. In this process, the band is changed and the phase-lock is broken. Second, PLL dynamics are still related to PVT variations due to K_{DCO} variation. Against TDC and DLF, it is very hard to design DCO to be perfectly insensitive to PVT variations.

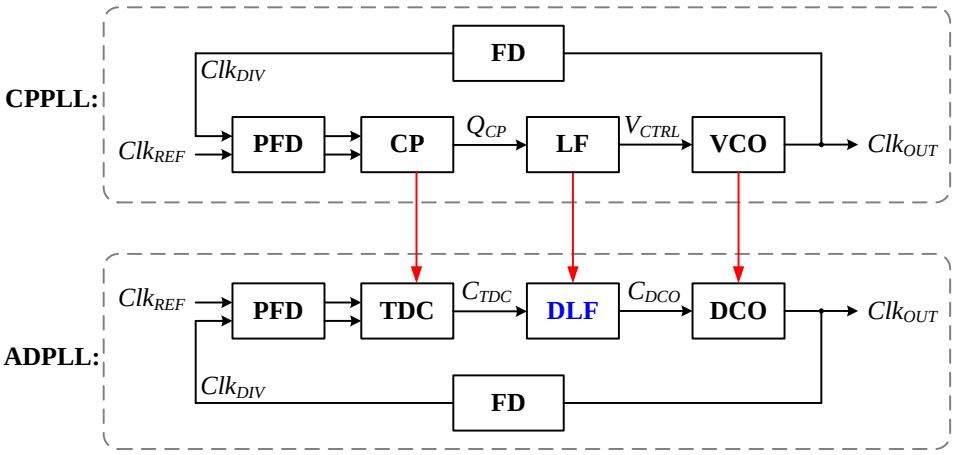


Figure 1.4: Block-diagram comparison between CPPLLs and ADPLLs

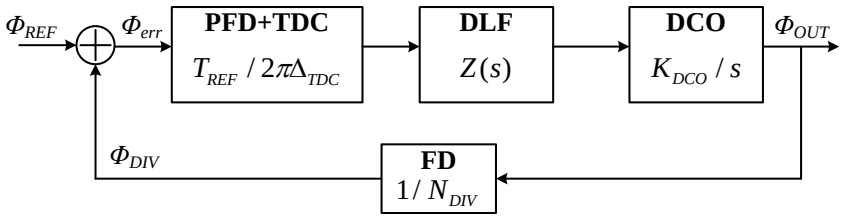


Figure 1.5: ADPLL small-signal model

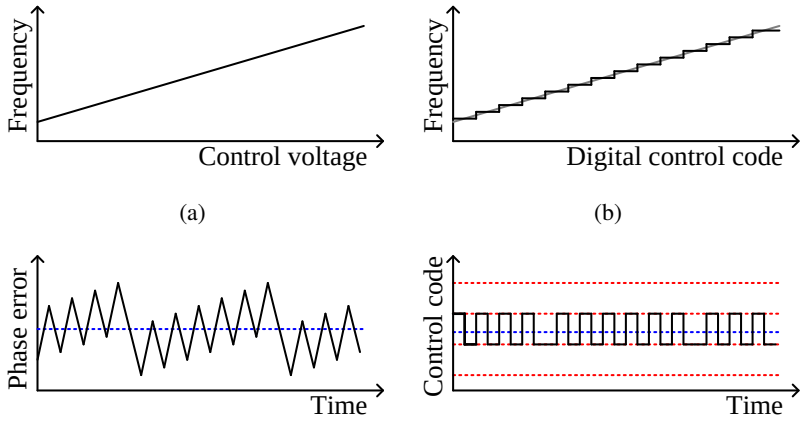


Figure 1.6: Examples of (a) VCO frequency curve, (b) DCO frequency curve, (c) AD-PLL phase error transitions and (d) DCO control code transitions in locked-state

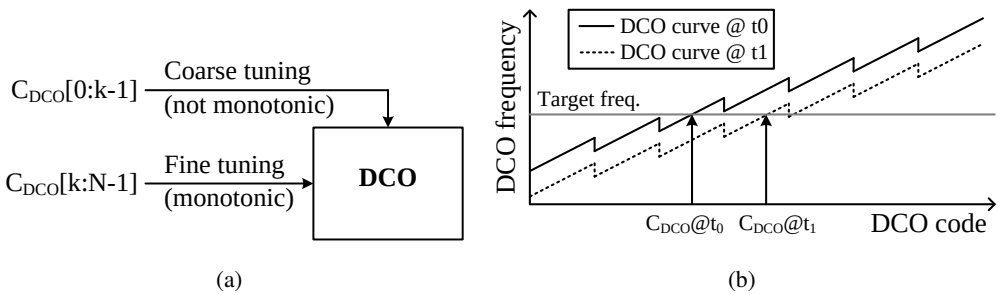


Figure 1.7: (a) Multi-band DCO, (b) example of DCO frequency curve variation depending on the time

1.3 Goal and Outline of Dissertation

The goal of this dissertation is design of a wide-range ADPLL using a simple DCO and a simple TDC. For this, a novel analog/digital dual-loop PLL structure is proposed. In contrast to existing wide-range ADPLLs using digital AFC, the proposed architecture adopts an analog AFC consisting of a CPPLL having very low loop bandwidth and, consequently, the ADPLL problems mentioned above can be resolved even with a DCO having a very narrow frequency range and a TDC having a very narrow dynamic range. Furthermore, the proposed PLL has several advantages as summarized below:

1. DCO has PVT-insensitive gain, and TDC has PVT-independent resolution. Therefore, the PLL loop dynamics are insensitive to PVT variations.

2. The PLL loop bandwidth can be adaptive to the reference frequency and the frequency dividing ratio. Therefore, the PLL can always have an optimum loop bandwidth, which is proportional to the reference frequency, even though the reference frequency and the dividing ratio are not previously known.

3. Supply noises can be compensated by the use of a supply regulator.

This dissertation is organized as follows. In chapter 2, a simple ADPLL architecture with a novel analog AFC for wide frequency range is proposed. The proposed PLL dynamics can be adaptive to the frequency dividing ratio. In chapter 3, measurement results of a prototype chip fabricated in 0.18μm CMOS process are analyzed. In chapter 4, how to reduce observed problems of the prototype PLL is discussed. An improving method of making the PLL dynamics additionally adaptive to PVT variations and the

reference frequency variation is also proposed in chapter 4. Improved version is verified by transistor-level simulation. Finally, conclusion of this works is given in chapter 5. Some behavioral circuit models and some analyses of the proposed PLL are additionally described in appendix.

Chapter 2

Proposed PLL Architecture

2.1 Simple ADPLL with a Novel Analog AFC

As mentioned in Chapter 1, the wide-range fine-resolution DCO is usually implemented using an AFC with a multi-band DCO [9]. However, it has the risk of phase-lock-breaking problem, and furthermore, it requires very complex circuitry. For example, [9] uses a DCO having 8-bit fine-tuning control codes and 10-bit AFC codes for the tuning range of 0.6$\sim$2GHz with the resolution of 0.3MHz/code. It requires several complex digital-to-analog converters (DACs) and, consequently, occupies a large chip area as shown in Figure. 2.1.

In order to resolve this problem, a novel dual-loop PLL having simple ADPLL with an analog AFC is proposed. Figure. 2.2 shows the block-diagram of the proposed PLL, where LDO is a low-drop-out supply regulator and MLCP is a multi-level charge pump working as a current DAC. In this architecture, DCO has control code (C_{DCO}) of a few bit and fine resolution (small K_{DCO}), resulting in the very narrow digital-tuning range. To overcome the range limit, the DCO supply voltage ($V_{DD;DCO}$) is controlled

by an analog AFC which is made up of a MLCP, a capacitor (C_{LF}) for a loop filter, and a supply regulator which controls $V_{DD;DCO}$ in accordance with V_{CTRL}. At the beginning of PLL operation, $V_{DD;DCO}$ is adjusted for frequency-locking through the analog loop as shown by the gray solid line in Figure. 2.2, while C_{DCO} is saturated at its maximum or minimum value. After the DCO frequency approaches the near of the intended frequency, C_{DCO} is adjusted for phase-locking through the digital loop as shown by the gray dotted line. As a result, a wide frequency range can be easily realized with simple DCO circuit having no complex DACs because the DCO supply voltage ($V_{DD;DCO}$) extremely changes the DCO oscillation frequency.

In addition, even if voltage or temperature is varied as time goes on and the DCO frequency characteristic is also varied, phase-lock is never broken because AFC continuously compensate $V_{DD;DCO}$ for the target frequency. And the harmful influence for the jitter performance due to external supply noises can be effectively reduced by the use of a supply regulated tuning technique [10][11].

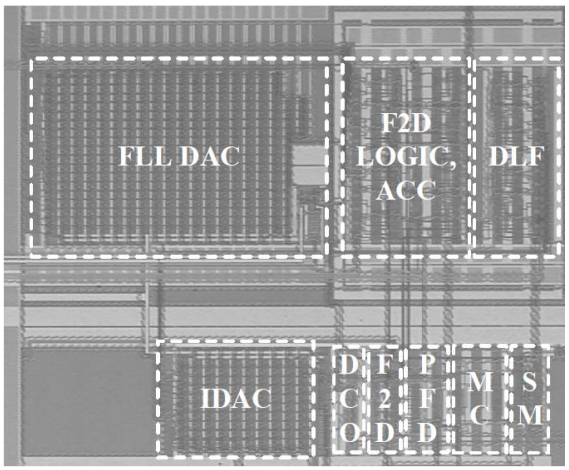


Figure 2.1: Layout example of a conventional wide-range ADPLL [9]. Total chip area is 0.27mm^2, where DCO and DACs occupy an area of more than half.

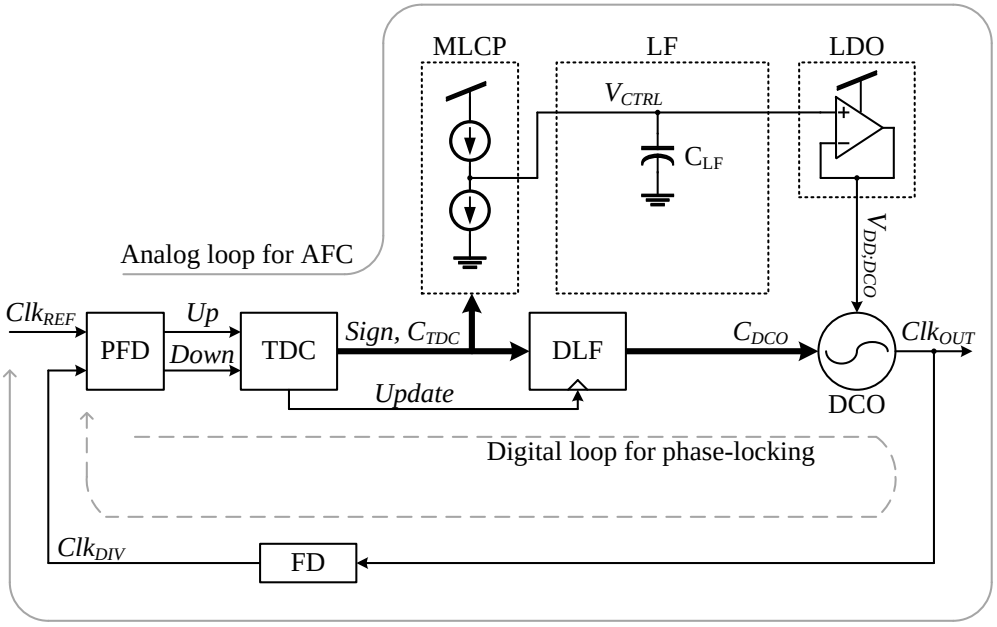


Figure 2.2: Block-diagram of proposed PLL

The operation of each building blocks is explained below in detail.

PFD, TDC Figure. 2.3 shows the timing diagram to explain the operation of PFD and TDC. PFD compares two input clock phases (Clk_{REF}, Clk_{DIV}) and generates two pulses ($Up, Down$). The pulse width difference between Up and $Down$ pulses is equal to the phase error (Φ_{err}) between Clk_{REF} and Clk_{DIV}. Up and $Down$ have a pulse width at least D_{RST}, which is called the PFD reset delay. TDC measures and quantizes Φ_{err}. $Sign$ signal signifies whether Φ_{err} is positive or negative, and C_{TDC} is the quantized digital code which is proportional to the absolute value of Φ_{err} with the resolution of Δ_{TDC}. Because TDC capture range is restricted in reality, C_{TDC} is restricted to C_{TDC_max}. In this work, C_{TDC_max} is set to 31 (5-bit TDC) for simplicity. The TDC output is changed at the falling edge of $Update$ pulse which is generated by the NAND operation between Up and $Down$ pulses having an update delay of D_{update}. $Update$ pulse will be used to activate DLF.

MLCP MLCP generates a current signal corresponding to the TDC output codes (C_{TDC} and $Sign$) having an amplitude of $I_{CPunit} \times C_{TDC}$, where I_{CPunit} is the current magnitude per the least significant bit (LSB).

LF LF generates the DCO coarse-tuning control voltage (V_{CTRL}) in accordance with the transfer function of $V_{CTRL}(s) = \frac{1}{C_{LF}s} \cdot I(V_{CTRL})$, where $I(V_{CTRL})$ is the incoming current signal to the V_{CTRL} node. Because the AFC loop bandwidth should be very low, a very large capacitor is required which are hard to be integrated. Therefore, an off-chip capacitor is used for LF. Why AFC should have

very low loop bandwidth is explained in the next section.

LDO LDO plays two roles. First, it provides the DCO supply voltage ($V_{DD;DCO}$) which follows V_{CTRL}. Second, it makes DCO to be isolated from external supply noises.

DLF Conventional CPPLLs have three poles. The third pole is required to attenuate the control voltage ripple inducing reference spurs. In ADPLLs, this problem does not exist, and a second-order PLL is sufficient. Figure. 2.4 shows the DLF operation, where α is the proportional path gain, and β is the integral path gain. It is activated when the $Update$ pulse arises. Because DCO has a limited number of control bits, the DLF output code (C_{DCO}) is restricted to C_{DCO_max}. In this work, DCO has only 5-bit control code for simplicity. Therefore, C_{DCO_max} is 15, which means that C_{DCO} is larger than or equal to -15, and smaller than or equal to 15. The z-domain transfer function of DLF is given by

$$C_{DCO}(z) = \left(\alpha + \beta\frac{1}{1-z^{-1}}\right) C_{TDC}(z). \tag{2.1}$$

DCO DCO generates a clock signal whose frequency is proportional to V_{CTRL} and C_{DCO}. In the proposed PLL, DCO is designed to have K_{DCO} which is approximately proportional to the DCO oscillation frequency. From this feature, the proposed PLL can get an important advantage. It is explained detailedly in the next section. How this feature can be realized is explained in section 3.

FD In the prototype chip of the proposed PLL, a simple programmable FD is used. The dividing ratio can be chosen from 8 cases (2, 4, 8, 16, 32, 64, 128, 256) by external toggle switches.

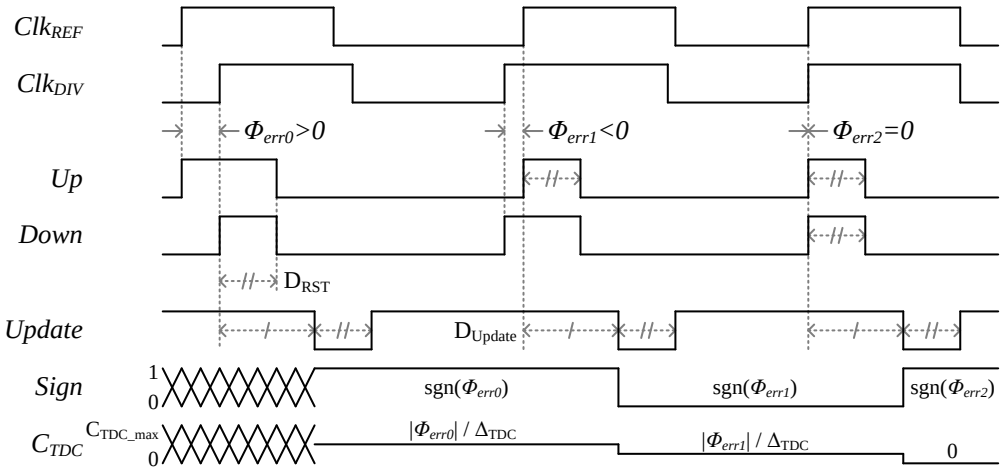


Figure 2.3: Timing diagram showing the operation of PFD and TDC

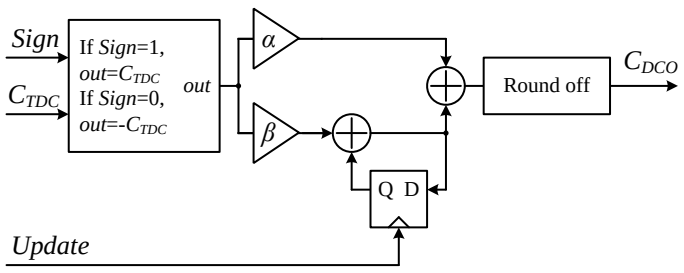


Figure 2.4: Block-diagram showing the DLF operation and linearized model

2.2 Loop Dynamics Analysis

The PLL is discrete-time system in reality because PFD, TDC, DLF, and MLCP are only activated when the reference clock pulse arrives. However, if the loop bandwidth is low enough, PLL can be treated approximately as a continuous-time linear time-invariant (LTI) system, and the small-signal model is shown in Figure. 2.5 (a), where K_{VCO} is the DCO gain for V_{CTRL} (Hz/V), K_{DCO} is the DCO gain for C_{DCO} (Hz/LSB), and N_{DIV} is the FD dividing ratio, which are intrinsic circuit characteristics. LF transfer function is

$$Z_{LF}(s) = \frac{1}{C_{LF}s}, \tag{2.2}$$

and DLF transfer function can be obtained from the parameters of an equivalent analog loop filter by using the bilinear transform as shown in Figure. 2.5 (b) [8], which is

$$\begin{aligned} Z_{DLF}(s) &= \frac{R_{DLF}C_{DLF}s + 1}{C_{DLF}s}, \\ R_{DLF} &= \alpha + \beta/2, \qquad C_{DLF} = \frac{1}{\beta \cdot f_{REF}}. \end{aligned} \tag{2.3}$$

For numerical analysis, Figure. 2.5 (a) is divided into two loops as shown in Figure. 2.5 (c) and (d). From these, loop filter coefficients (C_{LF}, α, β) are decided as the following procedure.

Given a specification of the unit-gain bandwidth (ω_n) for the AFC loop dynamics, the capacitor in LF (C_{LF}) can be calculated as

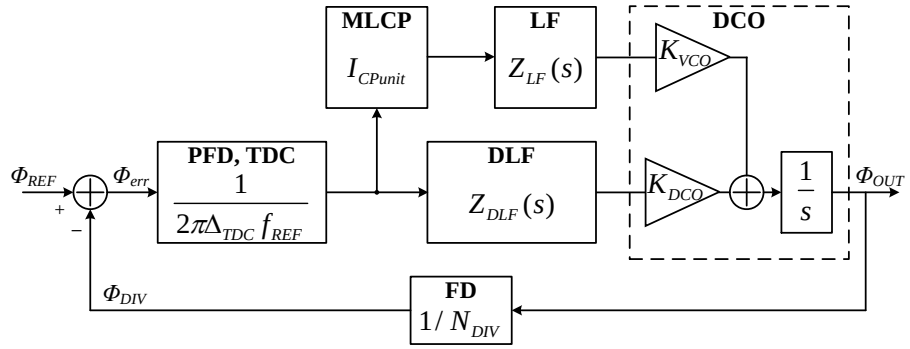
$$C_{LF} = \frac{I_{CPunit}T_{REF}}{\Delta_{TDC}} \times \frac{K_{VCO}}{\omega_n^2 N_{DIV}} \tag{2.4}$$

Similarly, DLF coefficients (α, β) can be calculated. Given a set of specifications, which include the unit-gain bandwidth (ω_{ugbw}) and the phase margin (θ_{mD}) for the digital loop

dynamics, α and β can be calculated as

$$
\begin{aligned}
&I_{CPD} \triangleq \frac{T_{REF}}{\Delta_{TDC}}, \qquad \omega_z \triangleq \frac{\omega_{ugbw}}{\tan\theta_{mD}}, \\
&R_{DLF} = \frac{N_{DIV}}{I_{CPD}K_{DCO}} \cdot \frac{\omega_{ugbw}^2}{\sqrt{\omega_z^2 + \omega_{ugbw}^2}}, \quad C_{DLF} = \frac{\tan\theta_{mD}}{R_{DLF} \cdot \omega_{ugbw}}, \\
&\alpha = R_{DLF} - \frac{T_{REF}}{2C_{DLF}}, \qquad \beta = \frac{T_{REF}}{C_{DLF}}.
\end{aligned} \tag{2.5}
$$

To sum up, filter coefficients (C_{LF}, α, β) are decided in accordance with 4 circuit characteristics (I_{CPunit}, K_{VCO}, Δ_{TDC}, K_{DCO}) and 5 design parameters (F_{REF}, N_{DIV}, ω_n, θ_{mD}, ω_{ugbw}).



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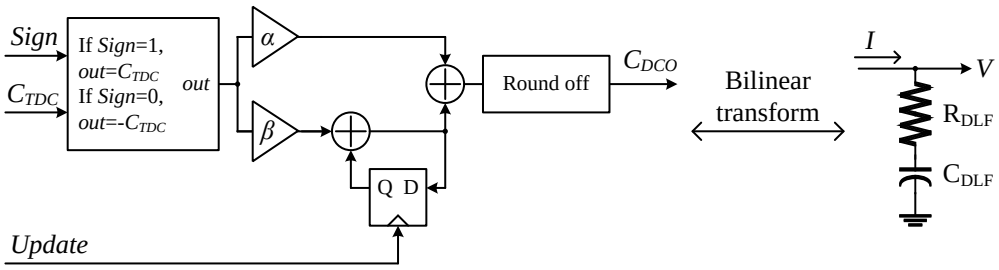

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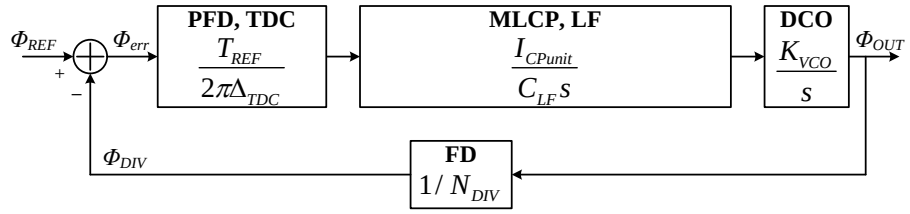
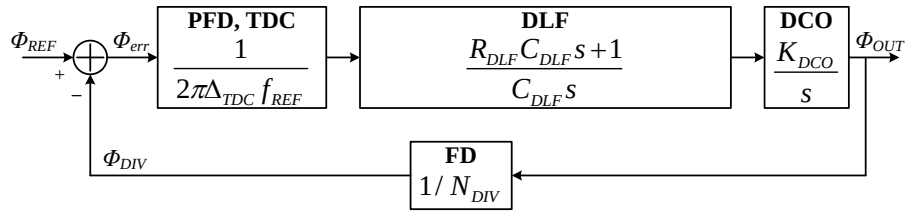


(c)



(d)

Figure 2.5: (a) Small-signal model of proposed dual-loop PLL, (b) linearized DLF model, (c) AFC loop only, (d) digital loop only

In order for the digital loop to be stable, the phase margin (θ_{mD}) must be larger than zero, and the loop bandwidth is restricted in accordance with the reference frequency. And, in order for the jitter performance, the loop bandwidth should be maximized in so far as the stability is maintained. Therefore, in the proposed PLL, θ_{mD} is fixed to $2\pi/6$ in radian (= 60°) for guaranteeing a stability and minimizing the input jitter peaking, and ω_{ugbw} is decided to $2\pi \cdot 0.1 \cdot f_{REF}$ for filtering the DCO phase noises as far as possible. As a result, Eq. 2.5 can be simplified as

$$\begin{aligned}
\alpha &= \frac{N_{DIV}\Delta_{TDC}f_{REF}^2}{K_{DCO}} \times \frac{2\pi \cdot 0.1}{\sqrt{\frac{1}{T^2}+1}}\left(1 - \frac{2\pi \cdot 0.1}{2T}\right), \\
\beta &= \frac{N_{DIV}\Delta_{TDC}f_{REF}^2}{K_{DCO}} \times \frac{(2\pi \cdot 0.1)^2}{\sqrt{T^2+1}}
\end{aligned} \tag{2.6}$$

, where $T = \tan\theta_{mD}$.

If K_{DCO} is proportional to the DCO oscillation frequency (=$f_{REF} \cdot N_{DIV}$) as mentioned in the previous section, α and β can be independent to the dividing ratio while target design parameters (θ_{mD}, ω_{ugbw}) are satisfied because Eq. 2.6 can be simplified once more as

$$\begin{aligned}
K_{DCO} &= K_{dg}f_{REF}N_{DIV}, \\
\alpha &= \frac{\Delta_{TDC}f_{REF}}{K_{dg}} \times \frac{2\pi \cdot 0.1}{\sqrt{\frac{1}{T^2}+1}}\left(1\text{-}\frac{2\pi \cdot 0.1}{2T}\right), \\
\beta &= \frac{\Delta_{TDC}f_{REF}}{K_{dg}} \times \frac{(2\pi \cdot 0.1)^2}{\sqrt{T^2+1}}
\end{aligned} \tag{2.7}$$

, where K_{dg} is the proportional constant for the DCO gain. From these equations, we can see that the digital loop dynamics are independent to N_{DIV} variations even though α and β are fixed to certain values. This feature is unique to the proposed PLL, which is

hard to be realized in conventional CPPLLs or conventional ADPLLs.

In the case of conventional CPPLLs, the loop filter consists of passive components having fixed capacitance or resistance. Therefore, N_{DIV} variations significantly affect PLL dynamics. Figure. 2.6 shows the small-signal model simulation results of conventional CPPLL with N_{DIV} variations from 4 to 32. In these simulations, loop filter coefficients are calculated for a natural frequency of $2\pi\times$2.5MHz, a damping factor of 1, a phase margin of 60°, and N_{DIV} of 16. If N_{DIV} is increased from 16, both the phase margin and the loop bandwidth are decreased as shown in Figure. 2.6 (c), resulting a large jitter peaking and large DCO-induced phase noises. If N_{DIV} is decreased from 16, the phase margin is also decreased, resulting a large jitter peaking. And the loop bandwidth is increased, which is inversely proportional to N_{DIV}. The PLL can be unstable easily if N_{DIV} is decreased excessively and the loop bandwidth exceeds $0.1f_{REF}$. Therefore, conventional CPPLLs are not suitable for a very wide-range frequency synthesizer even though VCO can provide a very wide frequency range.

In the case of conventional ADPLLs, adaptation for N_{DIV} variations is possible because N_{DIV} is a known value, and DLF coefficients (α, β) can be digitally controlled. However, in general, K_{DCO} is varied according to the DCO oscillation frequency, which is hard to be estimated due to the DCO non-linearity and PVT variations. Therefore, several complex calibration circuits such as a K_{DCO} measuring circuit and a DLF controller circuit are required.

In the case of the proposed PLL, AFC has N_{DIV}-sensitive loop dynamics like conventional CPPLLs. However, if the AFC loop bandwidth is low enough, it has a negligible effect on overall PLL dynamics. Overall PLL dynamics are decided only by the

digital loop in the proposed PLL, which has N_{DIV}-insensitive loop dynamics as theoretically verified in Eq. 2.7. Figure. 2.7 shows the small-signal model simulation results of the proposed PLL with N_{DIV} variations from 4 to 32. When the AFC unit gain bandwidth (ω_n) is f_{REF}/20, overall PLL dynamics are severely affected by N_{DIV} variations as shown in Figure. 2.7 (b) and (d). However, when ω_n is f_{REF}/400, overall PLL dynamics are almost identical to the case of digital loop only as shown in Figure. 2.7 (a) and (c). The phase margin and the 3-dB bandwidth are also insensitive to N_{DIV} as shown in Figure. 2.7 (e).

Therefore, in the proposed PLL, AFC is designed to have very low loop bandwidth. The loop filter capacitance in AFC (C_{LF}) is decided using Eq. 2.4 with f_{REF} of 25MHz and ω_n of $2\pi\times$80kHz. I_{CPunit}, K_{VCO}, Δ_{TDC}, and N_{DIV} are assumed to be 3μA, 3GHz/V, 7.5ps, and 16, respectively. Decided C_{LF} is 10.3μF. Because a very large capacitor is required, LF is hard to be integrated on chip. Thus, LF in AFC is realized using an off-chip ceramic capacitor.

In reality, several analog circuit characteristics such as I_{CPunit}, K_{VCO} are very sensitive to PVT variations. Thus, AFC loop dynamics are varied in accordance with these variations due to the fixed capacitance in LF, which are hard to be estimated. However, because AFC has a negligible effect on overall PLL dynamics as mentioned above, the proposed PLL can be insensitive to I_{CPunit}, K_{VCO} variations in the same manner as N_{DIV} variations.

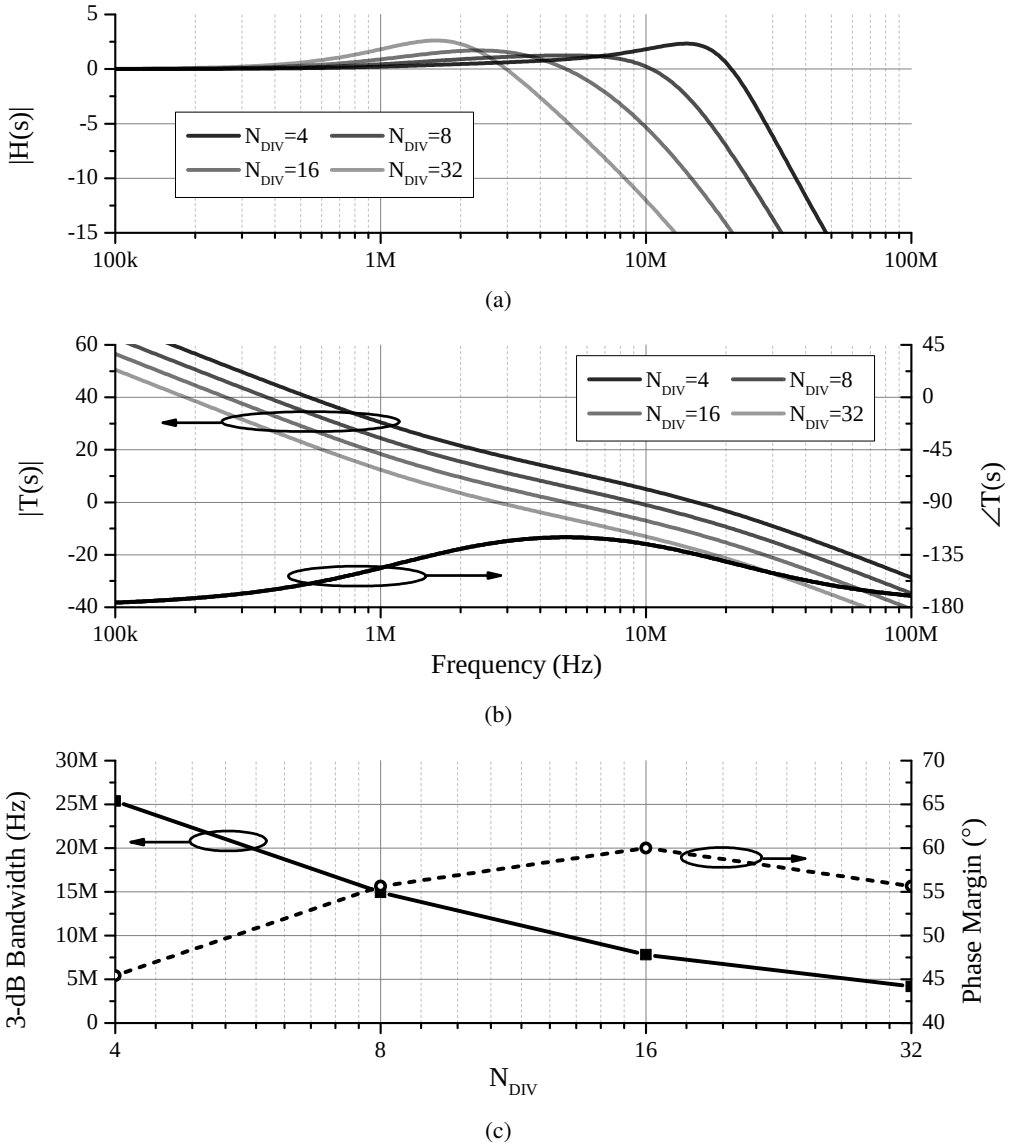


Figure 2.6: Small-signal model simulation results of conventional CPPLL using fixed loop filter with N_{DIV} variations, (a) closed-loop magnitude response, (b) open-loop magnitude and phase responses, (c) 3-dB bandwidth and phase margin variations

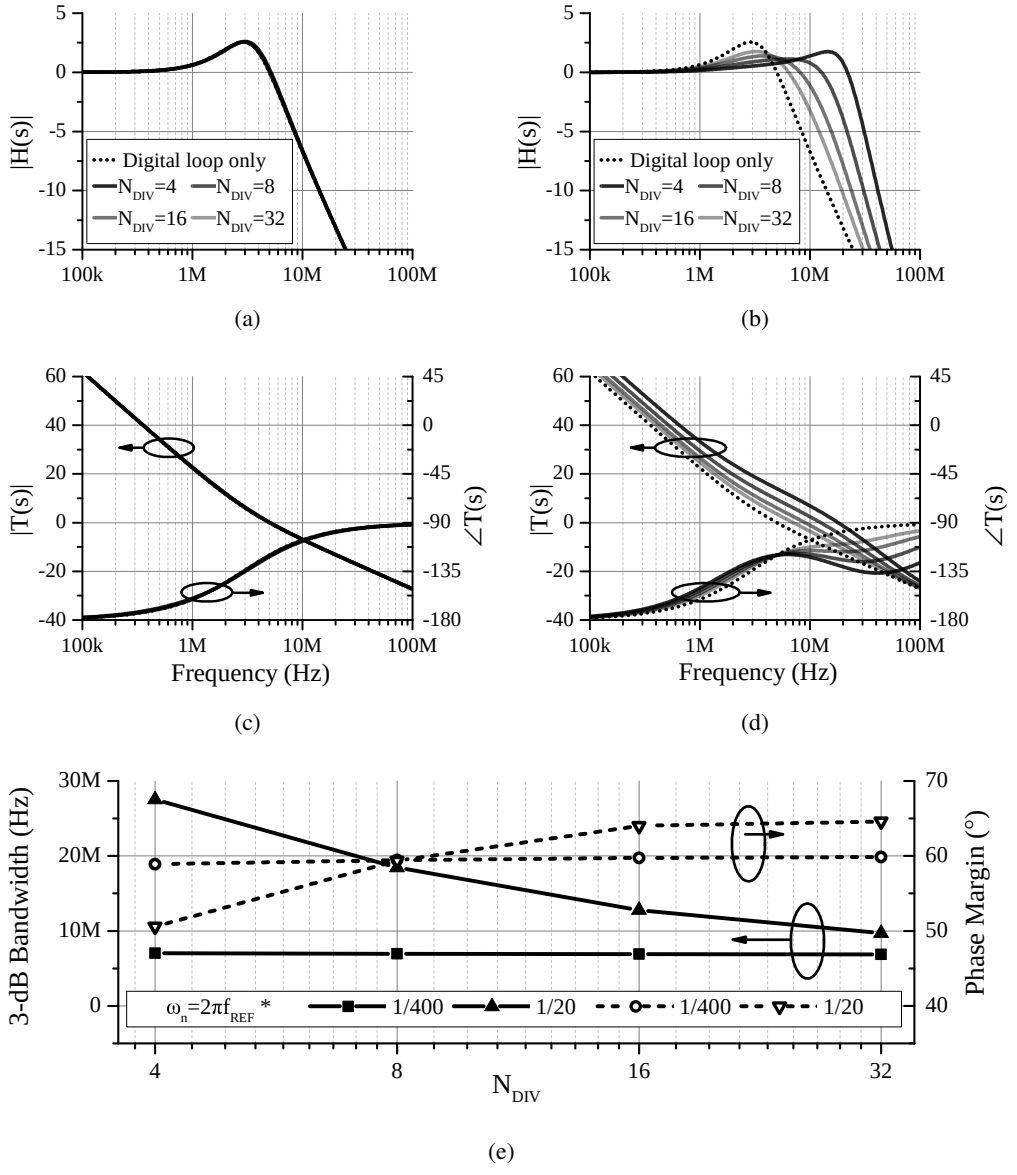


Figure 2.7: Small-signal model simulation results of proposed PLL with N_{DIV} variations, (a) closed-loop magnitude response with low ω_n (=$2\pi f_{REF}/400$), (b) with high ω_n (=$2\pi f_{REF}/20$), (c) open-loop magnitude and phase responses with low ω_n, (d) with high ω_n, (e) 3-dB bandwidth and phase margin variations

2.3 Implementation - DCO

The major issue in the DCO design is maintaining the proportional relation between the DCO gain and the DCO oscillation frequency ($K_{DCO} = K_{dg} f_{DCO}$) in order for satisfying Eq. 2.7 over a wide frequency range. Moreover, in order for the proposed PLL to have PVT-tolerant loop dynamics, K_{dg} should be insensitive to PVT variations.

In conventional DCOs, its frequency curve is strongly related to several circuit parameters such as parasitic capacitances, MOS threshold voltages (V_{th}), MOS transconductances (g_m) as shown in Figure. 2.8. Because these PVT-sensitive unknown variables influence the DCO frequency curve in combination, the DCO gain is hard to be estimated.

In order to reduce the number of unknown variables influencing K_{DCO} to 1, a novel phase interpolator-based DCO architecture is proposed as shown in Figure. 2.9 (a). Two delay stages having different delay time (D_{slow}, D_{fast}) are connected in parallel. Two outputs of these delay paths are combined using a digitally-controlled phase interpolator. Combination weights for the slow path and the fast path are 0.5-γ and 0.5+γ, respectively, where γ is a digitally-controlled variable. The output of the interpolator is inverted and fed-back to the input node for delay stages. Therefore, the DCO oscillation period (P_{DCO}) is decided as $P_{DCO} = D_{slow}(0.5 - \gamma) + D_{fast}(0.5 + \gamma)$.

If two delay stages are made up of identical delay cells, and the delay time of each delay stage is decided by the number of delay cells, the ratio between D_{slow} and D_{fast} can be insensitive to PVT variations because all delay cells are identically influenced by PVT variations. Therefore, the slope of the DCO oscillation period curve can vary over

PVT, but the x-axis intercept points of the curve are the same across PVT as shown in Figure. 2.9 (b). From this, the DCO oscillation frequency can be calculated as

$$\begin{aligned} P_{DCO} &= D_{slow}(0.5-\gamma) + D_{fast}(0.5+\gamma) \\ &= KD_{fast}(0.5-\gamma) + D_{fast}(0.5+\gamma) \\ &= D_{fast}\{0.5(1+K) + \gamma(1-K)\} \\ f_{DCO} &= \frac{1}{P_{DCO}} = \frac{1}{D_{fast}\{0.5(1+K)+\gamma(1-K)\}} \end{aligned} \tag{2.8}$$

, where K is PVT-insensitive proportional constant. In this equation, only D_{fast} is a PVT-sensitive parameter. The frequency variation according to γ can be calculated as

$$\frac{\Delta f_{DCO}}{\Delta \gamma} = -\left(\frac{1}{D_{fast}\{0.5(1+K)+\gamma(1-K)\}}\right)^2 D_{fast}(1-K). \tag{2.9}$$

If γ has a small value near zero,

$$\begin{aligned} f_{DCO}|_{\gamma=0} &= \frac{1}{D_{fast}}\frac{1}{0.5(1+K)} \\ \left.\frac{\Delta f_{DCO}}{\Delta \gamma}\right|_{\gamma=0} &= -\frac{1}{D_{fast}^2}\frac{D_{fast}(1-K)}{\{0.5(1+K)\}^2} = \frac{1}{D_{fast}}\frac{K-1}{0.25(1+K)^2}. \end{aligned} \tag{2.10}$$

The ratio between the frequency variation and the frequency at γ=0 can be simplified as

$$\left.\frac{\Delta f_{DCO}/\Delta\gamma}{f_{DCO}}\right|_{\gamma=0} = \frac{K-1}{0.5(K+1)}. \tag{2.11}$$

From this equation, when $|\gamma|$ is small enough, we can see that the ratio is almost independent to PVT variations due to the elimination of D_{fast} in the equation. If γ is proportional to the DCO control code (C_{DCO}) with a small proportional constant ϵ, γ is always near zero because DCO has only 5 control bits and $|C_{DCO}|$ cannot exceed 15. Threfore, the DCO gain (K_{DCO}) can be calculated as

$$\gamma = \epsilon C_{DCO}, \qquad K_{DCO} = \frac{\Delta f_{DCO}}{\Delta C_{DCO}} \approx \frac{\epsilon(K-1)}{0.5(K+1)} f_{DCO}|_{\gamma=0}. \tag{2.12}$$

While the PLL is locked, $f_{DCO}|_{\gamma=0}$ is approximately equal to the product of f_{REF} and N_{DIV}. Therefore,

$$\begin{aligned} K_{DCO} &\approx \frac{\epsilon(K-1)}{0.5(K+1)} \times f_{REF} N_{DIV} \\ &= K_{dg} f_{REF} N_{DIV}, \qquad K_{dg} = \frac{\epsilon(K-1)}{0.5(K+1)} \end{aligned} \tag{2.13}$$

, where ϵ and K are intrinsic circuit parameters which are insensitive to PVT variations. As a result, Eq. 2.7 can be satisfied, and the PLL can be adaptive to the N_{DIV} variation regardless of PVT variations.

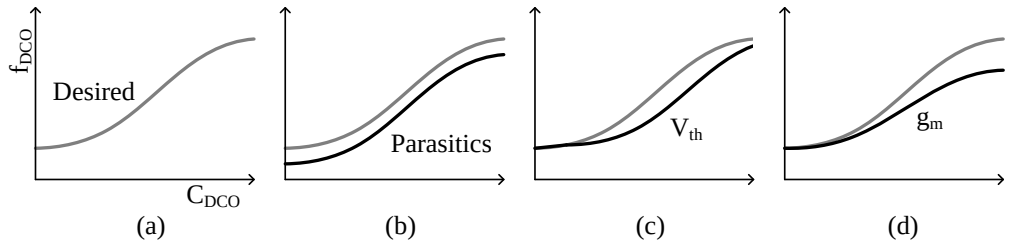


Figure 2.8: Examples of PVT-sensitive circuit parameters influencing DCO frequency curve

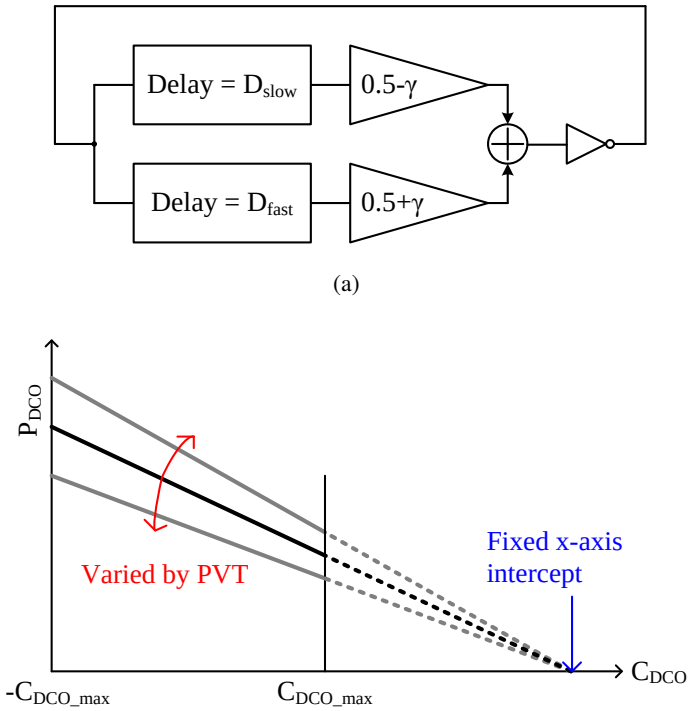


Figure 2.9: (a) Conceptional block-diagram of proposed DCO, (b) oscillation period curve examples with PVT variations

Figure. 2.10 shows the transistor-level schematics of the oscillator part in the proposed DCO for realizing Figure. 2.9. The slow path delay time is larger by 2×inverter-delay than the fast path delay time. A phase interpolator has two inverter arrays made up of 31 switched inverters and a large inverter which are connected in parallel. Inputs of these two inverter arrays are connected to the output of slow path and fast path, respectively. And outputs of two inverter arrays are combined. The number of turned-on switched inverters of each inverter array is digitally controlled by 31 control signals ($C_{[0:30]}$), adjusting combination weights of two delay paths. In order to prevent too large weight difference (large $|\gamma|$), a large inverter which is always turned on is attached to the inverter array. As the size of this inverter is larger, the influences of switched inverters for the weight difference becomes smaller, resulting small ϵ and fine K_{DCO}. In this work, this inverter size is 98-times larger than the switched inverter size.

All delay cells and the phase interpolator in the proposed DCO are based on inverters of which delay time is severely varied in accordance with the DCO supply voltage, $V_{DD;DCO}$. Process and temperature variations also affect them. However, because all inverters are identically affected by process, temperature, and $V_{DD;DCO}$ variations, the proportional relation between delay times of two delay paths are slightly varied, and Eq. 2.13 can be approximately satisfied. DCO measurement results of several fabricated chips show that the proportional constant K_{dg} in Eq. 2.13 has the error margin of only $\pm$10% over a very wide frequency range from 15MHz to 1.88GHz. Measurement results are described in detail in the next chapter.

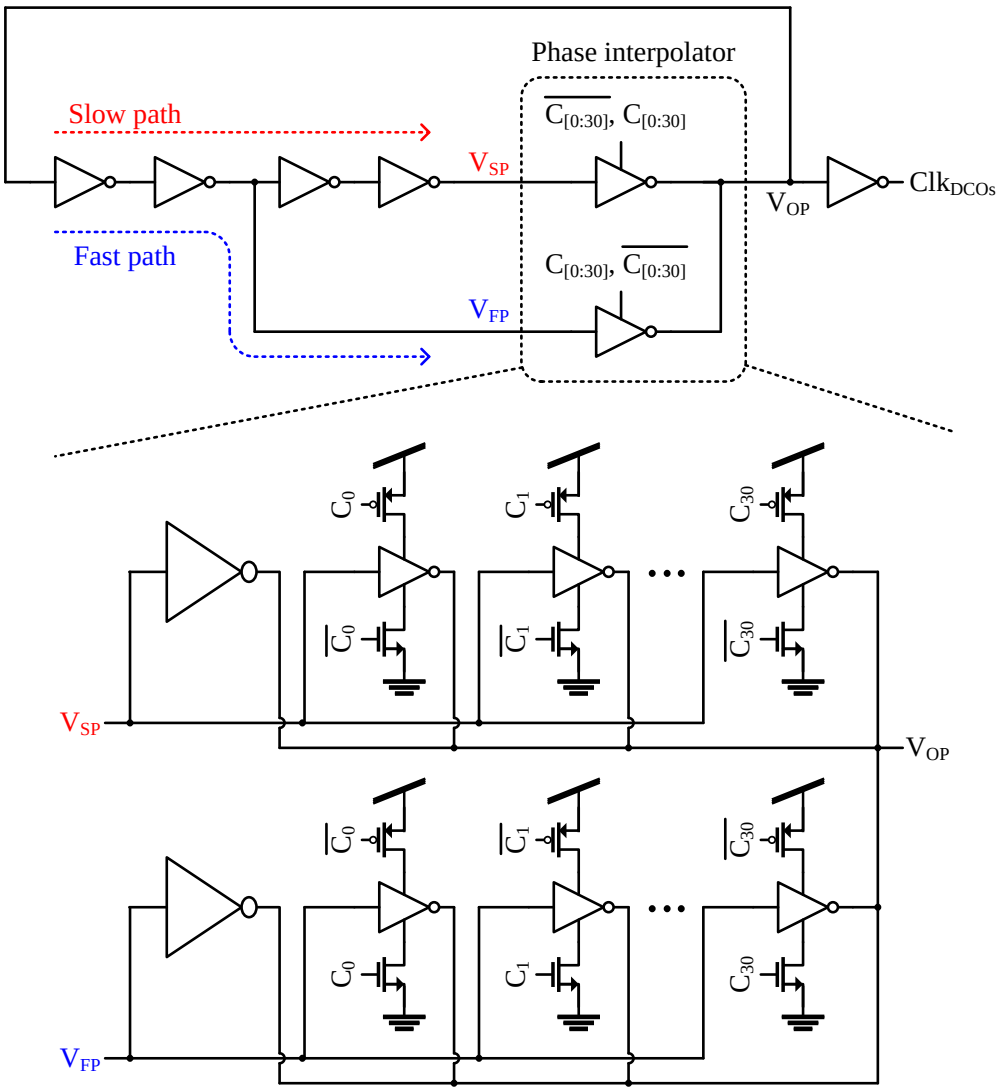


Figure 2.10: Schematics of proposed DCO - oscillator part

Because the DCO is made up of inverter-based circuits, and the DCO supply voltage is lower than the overall PLL supply voltage ($V_{DD;DCO} < V_{DD}$), the DCO output clock (Clk_{DCOs} in Figure. 2.10) swing is smaller than V_{DD}. If the PLL target frequency is very low, required $V_{DD;DCO}$ is also very low, and Clk_{DCOs} swing becomes too small, which is hard to be used to drive a frequency divider directly. On the other hand, the DLF output signals (C_{DCO}) have a full voltage swing. However, the phase interpolator control signals ($C_{[0:30]}$ in Figure. 2.10) should have a voltage swing as much as the phase interpolator supply voltage, $V_{DD;DCO}$. Therefore, C_{DCO} cannot be connected to the phase interpolator directly.

To overcome these problem, a level down converter (LDC) is attached at $C_{DCO[0:30]}$ in order to generate $C_{[0:30]}$ which have a voltage swing of $V_{DD;DCO}$, and a level up converter (LUC) is attached at Clk_{DCOs} in order to generate full-swing clock (Clk_{DCO}) as shown in Figure. 2.11 (a). Figure. 2.11 (b) shows the block-diagram of LDC. In order to prevent the oscillator core from the switching noises generated by LDC, a small LDO is used. The LDO generates $V'_{DD;DCO}$ of which voltage is equal to $V_{DD;DCO}$, driving a LDC cell array which consists of 31 cells. The schematics of the LDC cell is shown in Figure. 2.11 (c). Because C_{DCO} switching speed is low (=f_{REF}), LDC consumes very small currents, and the LDO can be designed to have small size. The schematics of LUC is shown in Figure. 2.11 (d). Pseudo-differential clock signals (ip, in) having a voltage swing of 0$\sim V_{DD;DCO}$ are generated by two inverters. And then, the voltage difference between ip and in is amplified by a differential-to-single (D2S) circuit. Because this D2S has a PMOS input pair and a large voltage gain, it can generate a full-swing clock signal even though $V_{DD;DCO}$ is very low.

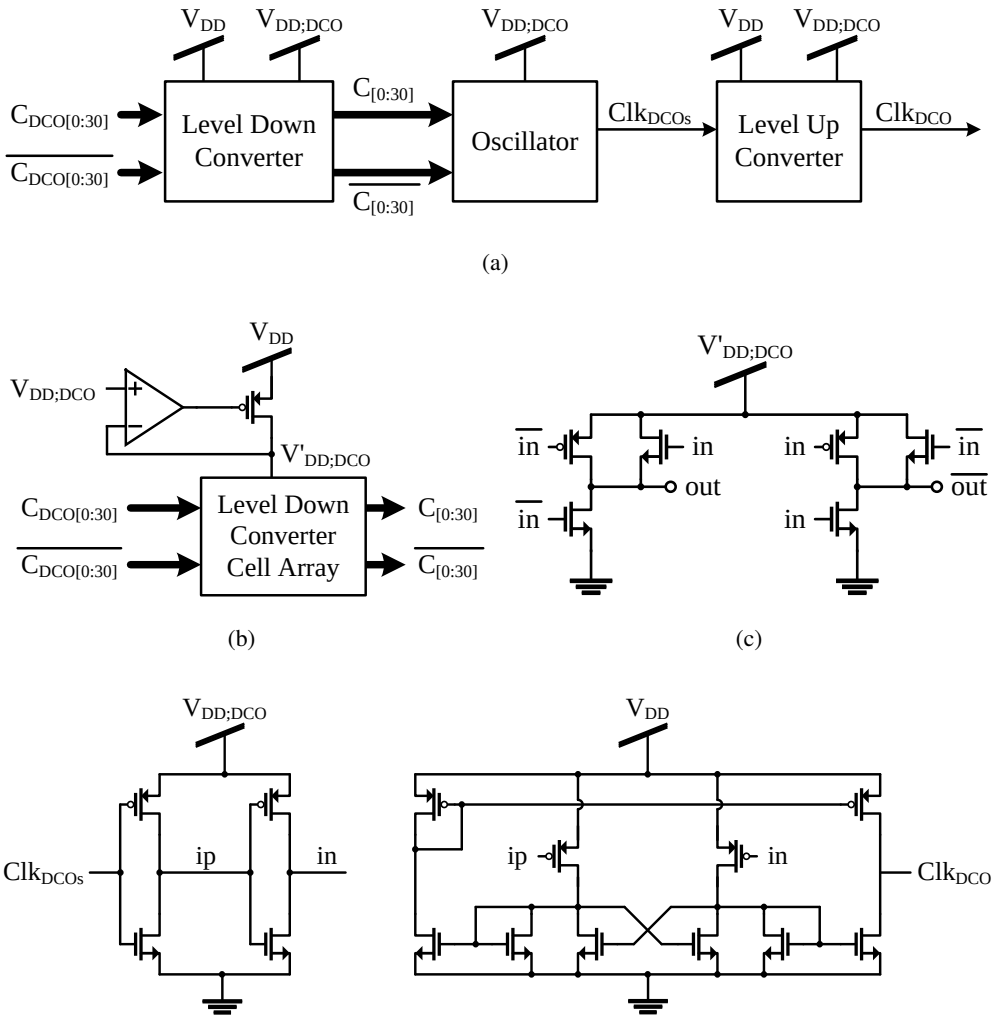


Figure 2.11: (a) Block-diagram of proposed DCO with input and output level converters, (b) level down converter, (c) schematics of level down converter cell, (d) schematics of level up converter

2.4 Implementation - PFD and TDC

ADPLLs suffer from deterministic jitters due to quantization noises in digitized phase and frequency signals. In order to minimize these, very fine resolution is required for the phase-to-digital converter (P2D) which senses the phase difference between the reference clock (Clk_{REF}) and the divided DCO output (Clk_{DIV}), and produces a corresponding digital signal [12]. There are several different ways of implementing high-resolution P2D. A popular method is using a conventional PFD followed by a high-resolution TDC [8][13][14][15]. This P2D architecture has an expanded frequency lock range even with a limited TDC input dynamic range [8]. Furthermore, it can mitigate influence of TDC non-linearity.

Conventional implementations for the P2D are shown in Figure. 2.12 (a) [13][14]. They uses an OR gate or a XOR gate in order to overlap PFD output pulses (UP, DN) and generate a pulse (V_X) whose width is proportional to the absolute value of the phase difference ($|\Delta_T|$) between PFD input signals (Clk_{REF}, Clk_{DIV}). The width of V_X is digitized by TDC and an L-bit output (C_{TDC}) is produced. The sign of the phase difference is decided by UP/DN sensor which detects which of UP or DN rising edge comes earlier.

[13] used an OR gate. However, the pulse width of V_X contains PFD reset delay (D_{RST}) as shown in Figure. 2.12 (b), where V_{X_OR} is the output of the OR gate. If the TDC resolution (Δ_{TDC}) is smaller than D_{RST}, P2D has a static offset of D_{RST}/Δ_{TDC} as shown by the solid line in Figure. 2.12 (c). This offset can corrupt PLL loop dynamics because the P2D seems to have bang-bang characteristic when $|\Delta_T|$ is small. This offset

is hard to be eliminated by post-TDC calibration because D_{RST} is very sensitive to PVT variations. On the other hand, [14] used an XOR gate instead of an OR gate. V_{X_XOR} in Figure. 2.12 (b) shows the output of XOR gate whose pulse width is equal to $|\Delta_T|$. From this, D_{RST} can be ignored and no offset is produced. However, when $|\Delta_T|$ is small, the V_X pulse width becomes too narrow to be measured by TDC, which results in a dead-zone as shown by the dotted line in Figure. 2.12 (c). This dead-zone aggravates the PLL jitter performance.

As a solution, [15] introduces an offset and dead-zone-free P2D architecture as shown in Figure. 2.13. The 1st phase decision circuit (PDC) determines and saves which one is the faster pulse between UP and DN, and produces Sign signal. Two delay buffers are attached after PFD in order to wait the 1st PDC input-to-Q delay. Next, two MUXs select the faster pulse for the Start signal and the slower pulse for the Stop signal. A start-stop TDC which is composed of vernier delay line (VDL) and PDCs [16] digitizes the time difference (Δ_{T2}) between Start and Stop and produces L-bit C_{TDC} output. By the use of VDL, TDC can have very fine and controllable resolution and, moreover, the load capacitance of Start and Stop are almost same. Therefore, Δ_{T2} is exactly equal to $|\Delta_T|$, and the offset due to the PFD reset delay can be eliminated. If Start and Stop pulses have enough width by the use of large D_{RST}, a dead-zone is not formed also. Note that it was not described in [15] that the P2D has the advantages of offset and dead-zone-free characteristic. A delay buffer is attached at the last of Start delay path in order to produce Trigger signal which will be used to latch the final code ($Q_0 \sim Q_{L-1}$).

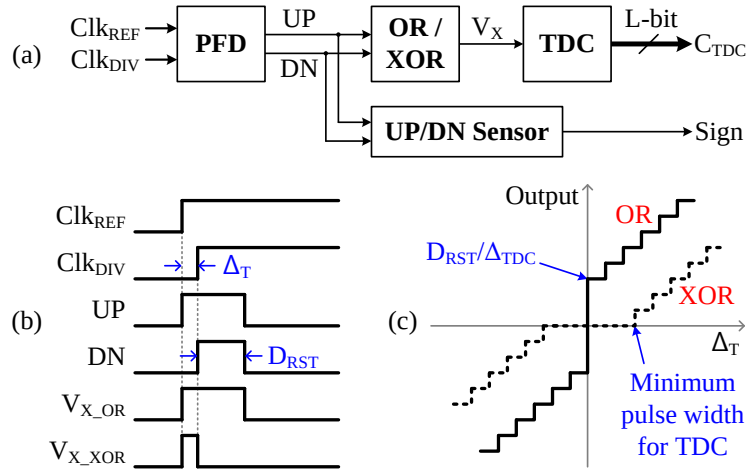


Figure 2.12: (a) Conventional combination of PFD and TDC, (b) timing diagram, (c) potential offset or dead-zone problem

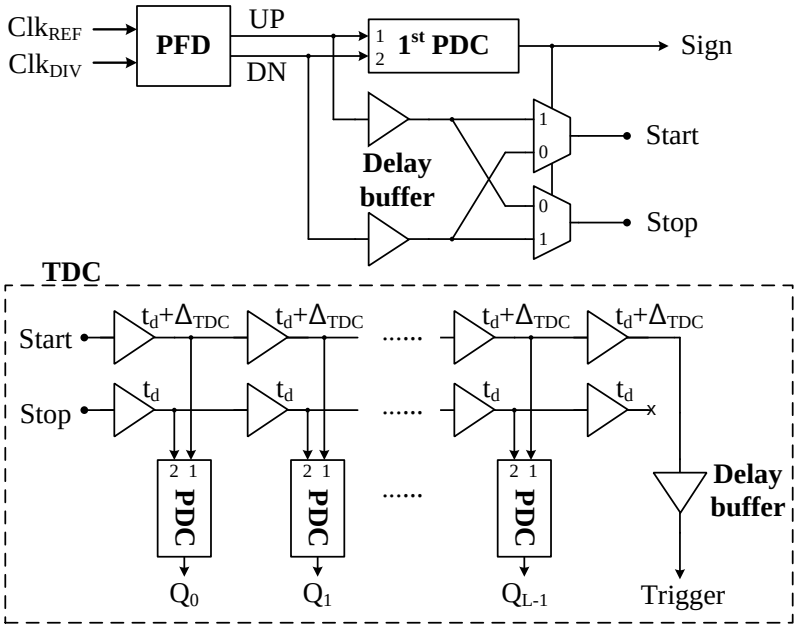


Figure 2.13: Designed combination of PFD and TDC which can avoid offset and dead-zone problems

However, this P2D requires precise PDCs which can accurately determine the order of two pulses. If each PDC is made up of a conventional D-flip-flop (DFF), the finite setup time of a DFF produces a phase offset of 30∼50 ps resulting in a dead-zone and limited TDC resolution. In order to avoid this problem, [15] adopts two high-gain time-amplifiers (TAs) at the front of a conventional DFF. However, this TA-based PDC (TA-PDC) is complex and consumes large power. Moreover, due to finite gain and non-linearity of TAs, the phase offset cannot be completely eliminated.

In order to solve these problems, a novel arbiter-based PDC circuit is proposed. An arbiter circuit can be used to determine the order of two pulses [16]. Because it has a symmetric architecture for both input pulses, very small time difference between two input pulses can be detected. However, because arbiter output responds to the falling edges of input pulses, stand-alone arbiter cannot be used for PDC. By adding a saving circuit optimized for the P2D, a new PDC having very small phase offset can be realized.

Figure. 2.14 (a) shows the schematics of the proposed arbiter-based PDC. While both IN_1 and IN_2 are low, both of arbiter outputs (X, Y) are reset to high. With the arrival of IN_1 rising edge, X goes low and Y remains high regardless of IN_2 rising edge as shown in Figure. 2.14 (b). In order to save this Y value, a gated D latch is attached. Two buffers having time delay of T_{BD} are inserted between the arbiter and the latch so that the arbiter is not influenced by the latch switching. Dummy buffers are attached in order to make the arbiter symmetric. The latch tracks the buffered Y pulse (Y') while the buffered IN_2 pulse (E) is high.

Figure. 2.14 (c) shows the case when IN_2 rises before IN_1. With the arrival of IN_2 rising edge, X remains high and Y goes low and the latch starts to track Y until IN_2 falls.

After IN_2 falls, X goes low and Y goes high. However, the latch output does not tracks this Y transition and remains low because E goes low at the same time as Y' rising edge.

Figure. 2.14 (d) shows the case when IN_1 rises and falls earlier than IN_2. In this case, Y' goes low before E goes low and the latch saves the low value even though IN_1 rises before IN_2. However, this case cannot occur in the P2D made up of PFD and TDC because PFD outputs are simultaneously reset and IN_1 and IN_2 of the 1^{st} PDC have falling edge at the same time. In TDC, since Start and Stop have falling edges at the same time and Start is more delayed than Stop through VDL, IN_1 falling edge of each PDC is always later than IN_2 falling edge. If IN_1 falling edge is slightly earlier than IN_2 falling edge due to noises or device mismatches, this does not become a problem because the latch has 30$\sim$50-ps setup time before it can track IN_1 falling edge.

Another type of arbiter-based PDC circuit was introduced in [17]. It can decide the pulse order exactly with low power consumption and short input-to-Q delay. However, it requires a reset signal before a new measurement. Since our PDC does not require reset signals, it should be more appropriate for high-speed P2D operation.

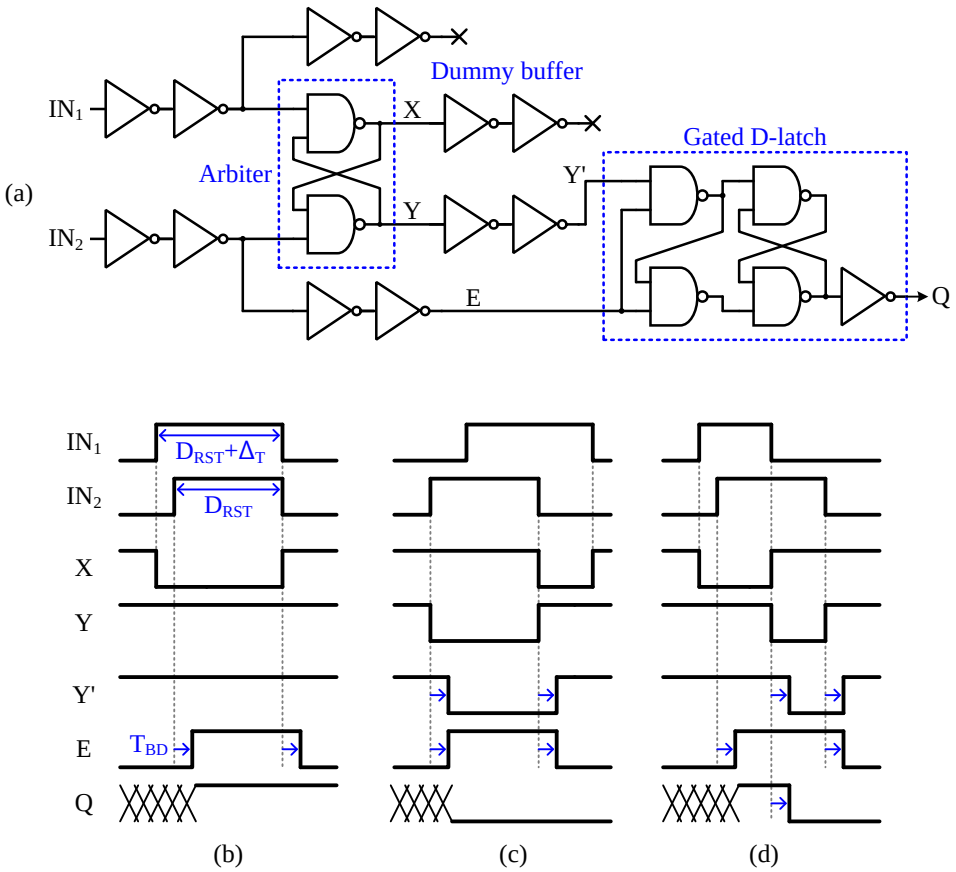


Figure 2.14: (a) Schematics of proposed arbiter-based PDC circuit, timing diagram with the case of (b) IN_1 first, (c) IN_2 first, (c) error

For the performance comparison between the TA-based PDC (TA-PDC) having TA gain of about 216 [15] and our PDC, each PDC is simulated with Monte-Carlo analysis. Two pulses having time difference of Δ_T are introduced to PDC, and PDC output (Q) is measured with Δ_T sweep. Then, Δ_T where Q changes is marked, which indicates PDC phase offset. To account for device mismatches, a 100-iteration Monte-Carlo analysis is carried out. The results of two PDCs are summarized in Figure. 2.15 (a) and (b). From these, we can see that the proposed arbiter-based PDC has much smaller phase offset than TA-PDC. Furthermore, the proposed PDC is much more insensitive to device mismatches than TA-PDC. It is because the proposed PDC is structurally symmetric.

The energy consumption (femto-Joule) per one operation and input-to-Q delay are also simulated. The proposed PDC and TA-PDC consume 308.43fJ and 1282.7fJ per one operation, respectively. As a result, energy consumption is reduced more than 75%. Figure. 2.16 shows the input-to-Q delay simulation results of two PDCs. When the PDC output rises, the input-to-Q delays of the proposed PDC and TA-PDC are 296.75ps and 709.57ps, respectively. When the PDC output falls, the input-to-Q delays are 227.85ps and 567.64ps. Therefore, the input-to-Q delay is also reduced more than 58%.

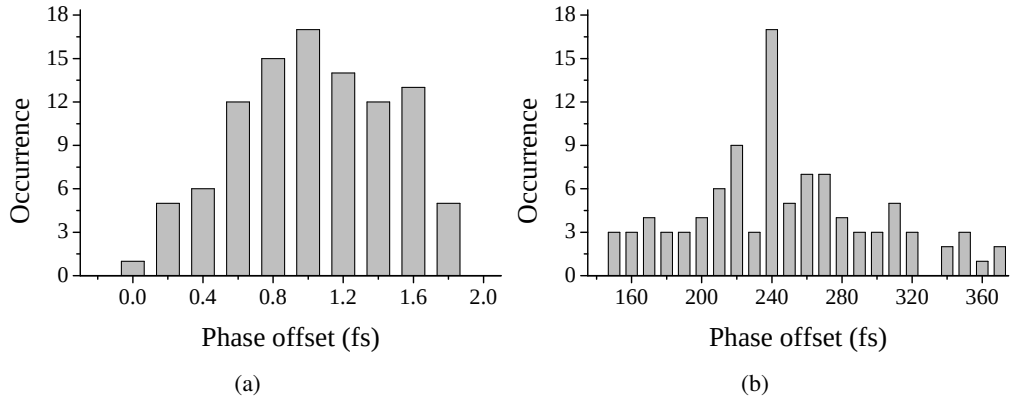


Figure 2.15: Monte-Carlo phase offset simulation results of (a) proposed arbiter-based PDC, (b) time-amp-based PDC

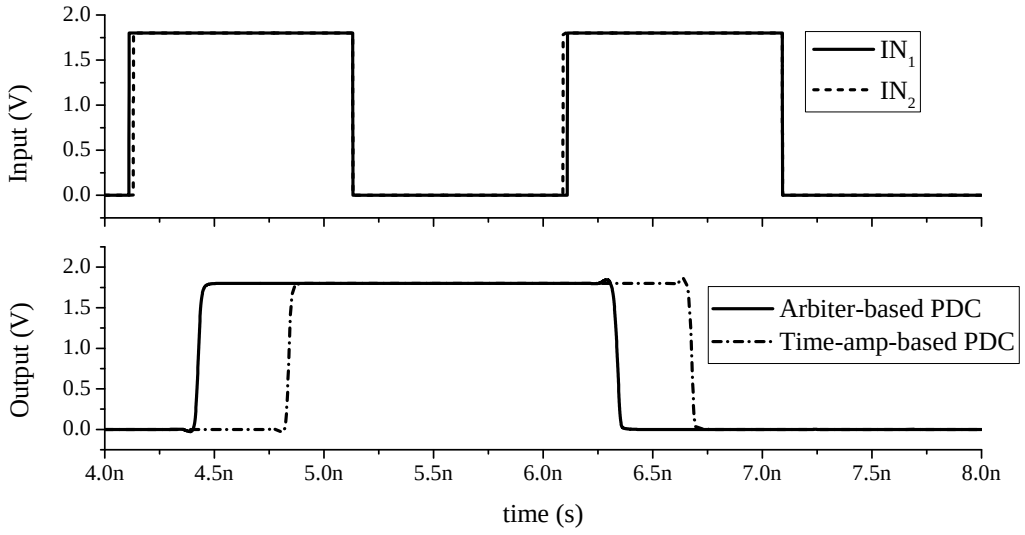


Figure 2.16: Input-to-Q delay simulation results

PFD circuit is implemented using a conventional NAND-latch type PFD as shown in Figure. 2.17 (a) [18]. MUX circuit is implemented using transmission gates as shown in Figure. 2.17 (b). Delay cells for the fast path and the slow path in VDL TDC are shown in Figure. 2.17 (c) and (d), respectively. By different sizing the first inverter, Figure. 2.17 (c) and (d) has different delay times which decides Δ_{TDC}. The TDC consists of 31-stage vernier delay line. Therefore, the TDC has 5-bit output code, and C_{TDC_max} is 31.

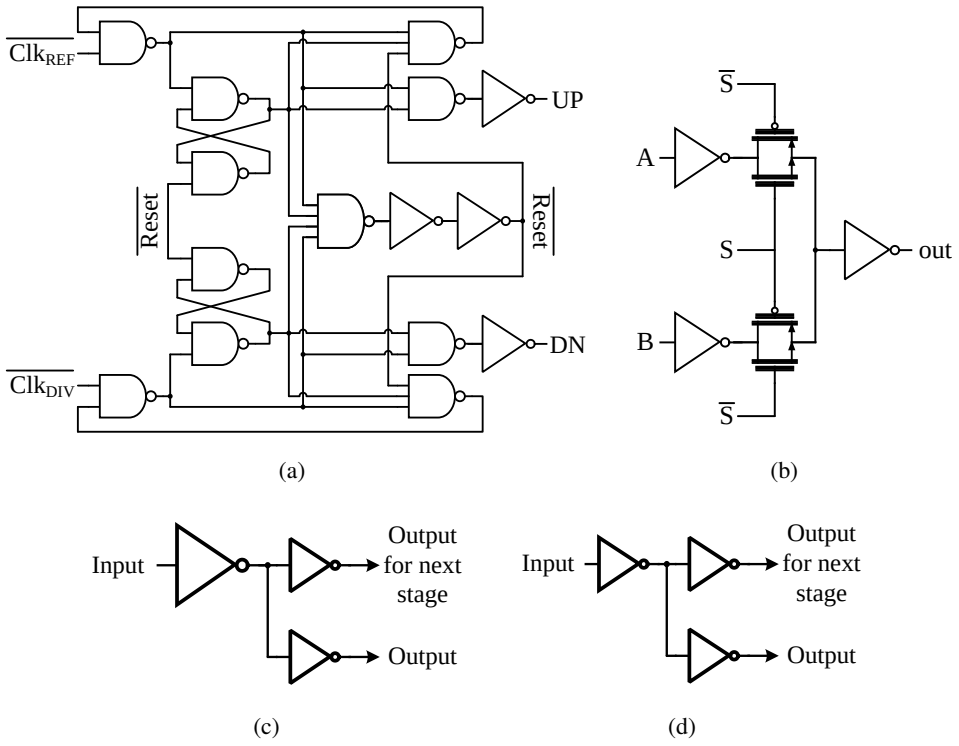


Figure 2.17: Schematics of (a) PFD, (b) MUX, (c) delay cell for fast path, (d) delay cell for slow path in VDL TDC

A P2D shown in Figure. 2.13 based on our PDC is simulated with the same test-bench as the PDC simulation, and the energy consumption per one operation and P2D transfer function are measured. The P2D consumes 36.71pJ per one operation for NN process corner. The P2D power consumption will be the product of energy consumption per one operation and the PLL reference frequency. Figure. 2.18 shows simulated P2D transfer functions with process corner variations. Δ_{TDC} results are 6.45ps, 7.78ps, 9.88ps for FF, TT, SS corners, respectively. Although Δ_{TDC} is affected by process corner variations, no offset nor dead-zone is observed for all process corners. The Δ_{TDC} variation will be calibrated in chapter 4.

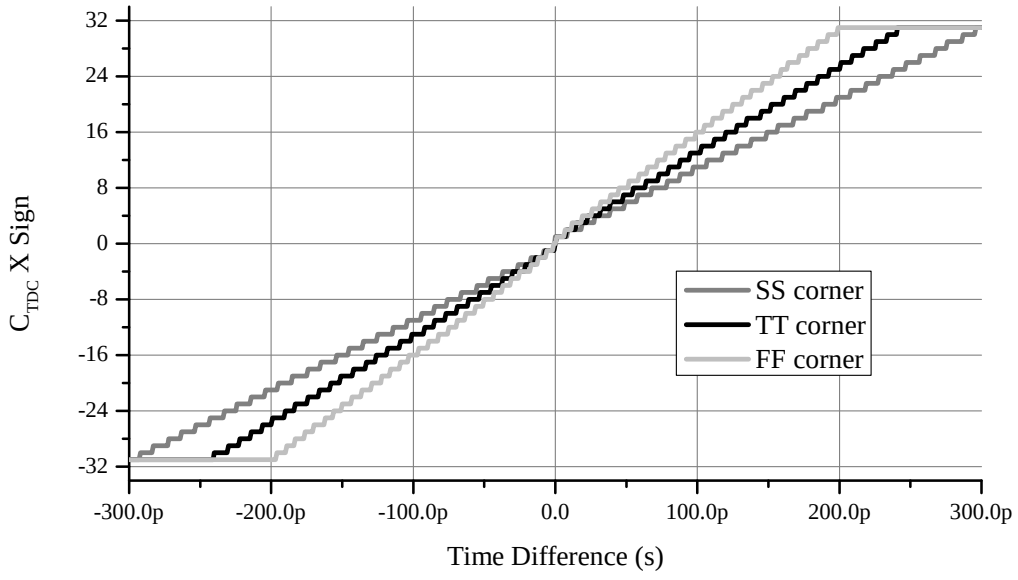


Figure 2.18: Simulated transfer function of PFD-TDC using our PDC

2.5 Implementation - Etc.

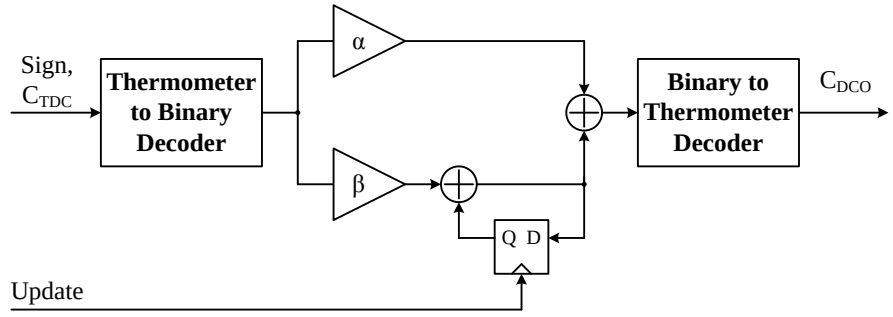
2.5.1 DLF

Figure. 2.19 (a) shows the DLF block-diagram. For the digital arithmetic operations, TDC outputs (Sign, C_{TDC}) should be decoded from thermometer type to binary type. And, in order to guarantee the DCO monotonicity, DLF output should be decoded from binary type to thermometer type. For these, a thermometer-to-binary decoder (T2B) and a binary-to-thermometer decoder (B2T) are attached. Overall DLF is synthesized automatically using standard digital logic cells as shown in Figure. 2.19 (b). It occupies a chip area of 314.5×75.1μm^2.

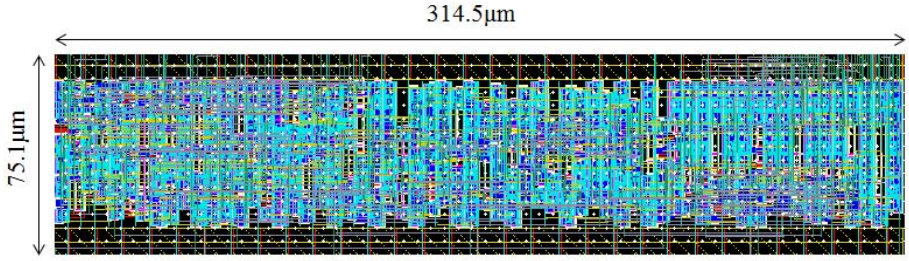
In the proposed PLL, DLF can be designed simply due to following reasons.

1. Because the multiplicands (α, β) are certain fixed constants, digital multiplier can be simple, occupying small chip area.

2. In conventional ADPLLs, C_{DCO} should have many control bits to provide a frequency range, and the design of B2T for these ADPLLs is a burden because it should have an enough speed margin and small timing misalignments. Therefore, it should be custom-designed as [13]. However, in the proposed PLL, because C_{DCO} has only 31 levels, B2T can be synthesized automatically. C_{TDC} has also only 31 levels, and T2B is also synthesized. As a result, the DLF design time can be effectively reduced.



(a)



(b)

Figure 2.19: (a) DLF block-diagram, (b) synthesized layout

2.5.2 MLCP

31 $\overline{up}$ signals and 31 dn signals are generated in accordance with the TDC outputs ($Sign$ and $C_{TDC[0:30]}$) by the MLCP controller shown in Figure. 2.20 (a). The controller consists of 31 controller logic cells shown in Figure. 2.20 (b). These $\overline{up_{[0:30]}}$ and $dn_{[0:30]}$ signals drive the MLCP core circuit which is made up of several current sources and switches as shown in Figure. 2.20 (c). When $Sign$ is high, only charging switches are activated. When $Sign$ is low, only discharging switches are activated. The number of activated switches is equal to C_{TDC}.

In order to minimize current mismatches between charging currents and discharging currents, the bias voltage for charging current sources (pbias) is automatically generated by a replica-pbias generator [19].

The amplitude of charging/discharging currents per LSB (I_{CPunit}) is about 3μA.

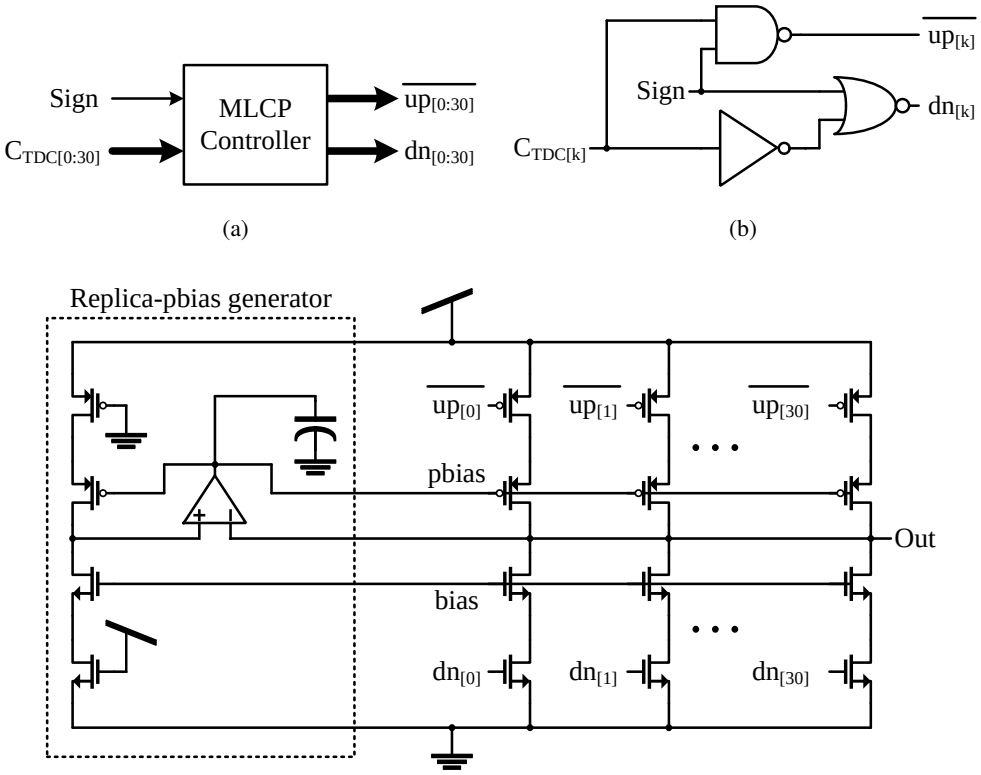


Figure 2.20: (a) MLCP controller, schematics of (b) MLCP controller cell, (c) MLCP core

2.5.3 LDO

LDO is made up of an OP-amp, a power PMOS, and a compensation capacitor as shown in Figure. 2.21 (a). The power PMOS is used for low drop-out voltage. The compensation capacitor made up of a MOSCAP helps LDO to be stable. The OP-amp is designed using a self-biased folded-cascode OTA [20] as shown in Figure. 2.21 (b), whose DC voltage gain is about 40dB.

2.5.4 FD

In the prototype chip of the proposed PLL, a simple programmable FD is used which is made up of 8 $\frac{1}{2}$ frequency dividers and 7 MUXs as shown in Figure. 2.21. The dividing ratio can be chosen from 8 cases (2, 4, 8, 16, 32, 64, 128, 256) by controlling MUX switching signals (sw0$\sim$sw2) which are provided by 3 external toggle switches. In order to guarantee the FD operating speed margin, true single-phase clock (TSPC) DFF-based $\frac{1}{2}$ frequency dividers are used for the first 4 $\frac{1}{2}$ divider stages [21]. For a low power consumption and a stability, NAND DFF-based $\frac{1}{2}$ frequency dividers are used for the last 4 $\frac{1}{2}$ divider stages.

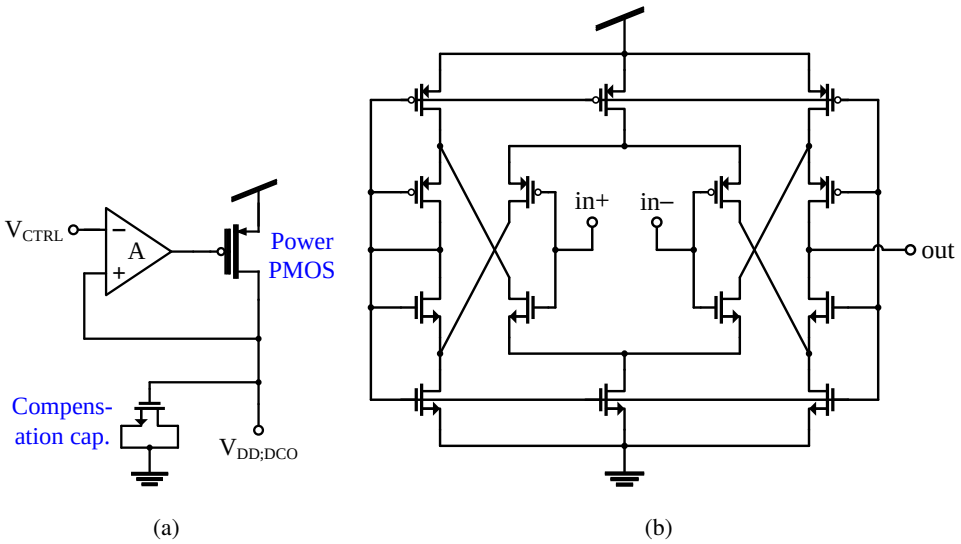


Figure 2.21: Schematics of (a) LDO, (b) OP-Amp

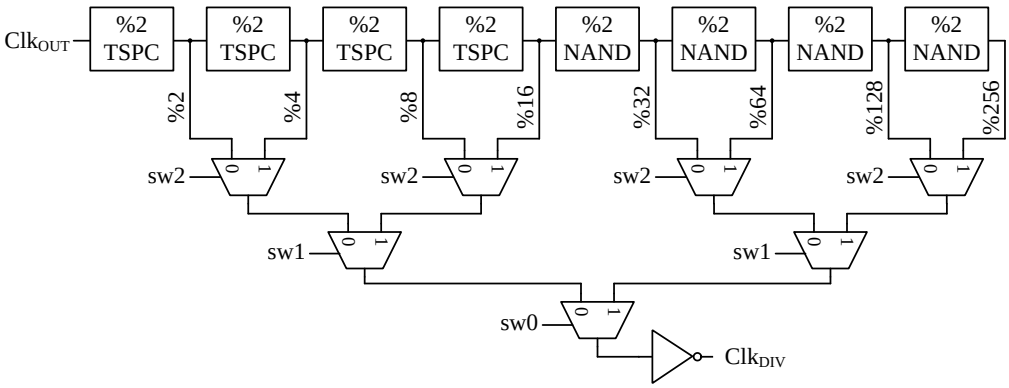
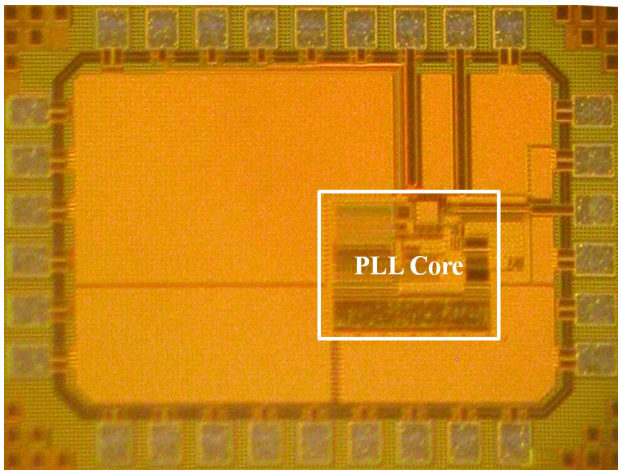


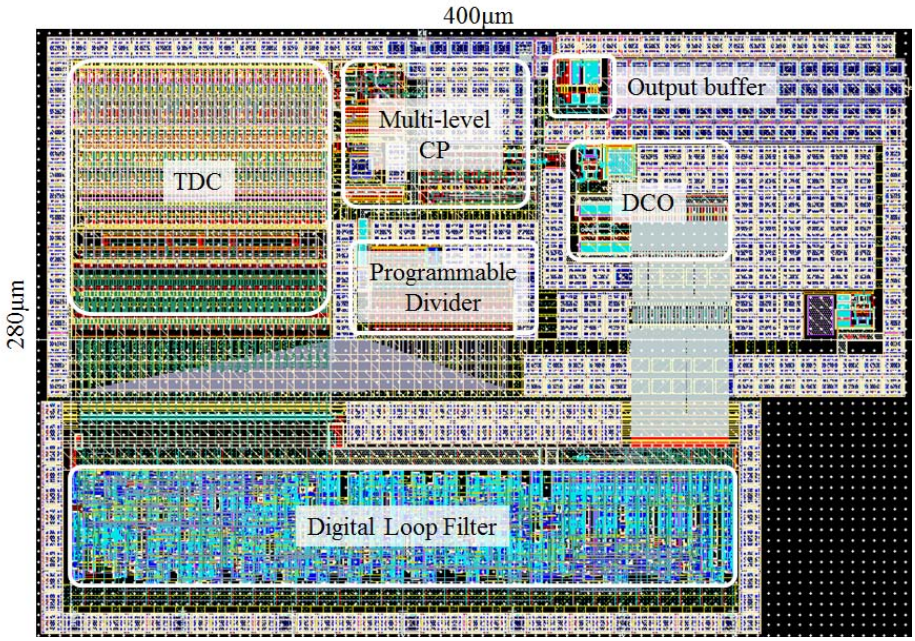
Figure 2.22: Schematics of programmable frequency divider

2.6 Implementation - Prototype Chip

Figure. 2.23 (a) shows the die photograph of the prototype chip which is implemented in 0.18μm CMOS process. The PLL core layout is shown in Figure. 2.23 (b). The core occupies a chip area of about $400\times280\mu m^2$. LF is not included because it will be realized using an off-chip ceramic capacitor.



(a)



(b)

Figure 2.23: (a) Fabricated chip photograph, (b) PLL core layout

Chapter 3

Measurement Results

In this chapter, experimental results of fabricated chip are given. The chips are mounted on printed circuit board (PCB) with bonding-wires (device under test or DUT) as shown in Figure. 3.1. At first, the DCO oscillation frequency characteristics are measured in section 1. And the PLL operations with various N_{DIV} are tested in section 2. Unfortunately, fabricated prototype PLL chips show an abnormal behavior. The reason of the defect is analyzed in section 3.

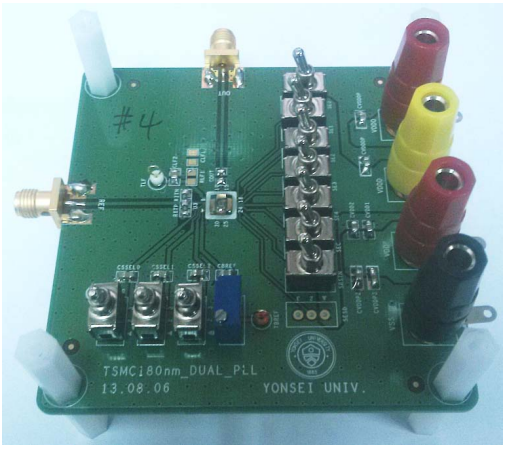


Figure 3.1: Photograph of test board (DUT)

3.1 DCO Measurement Results

In order to measure the DCO coarse-tuning range, the control voltage (V_{CTRL}) is forcibly controlled by connecting V_{CTRL} to a power supply directly, and the fine-tuning control code (C_{DCO}) is fixed to zero. The main supply voltage (V_{DD}) is connected to an 1.8-V power supply. DCO oscillation frequencies (f_{DCO}s) are measured using a spectrum analyzer with V_{CTRL} variation from 0.5V to 1.2V. The same measurement is repeated in several changes of DUTs (Chip1$\sim$Chip4) and main supply voltages (1.6V$\sim$2.0V), and results are summarized in Figure. 3.2 (a). From these, it is verified that the fabricated DCO can provide a very wide frequency range from 15MHz to 1.88GHz for all cases of DUTs and V_{DD}s. The measured DCO coarse-tuning gain for V_{CTRL} (K_{VCO}) is about 3.27GHz/V when f_{DCO} is 1.6GHz.

In order to the DCO fine-tuning gain for C_{DCO} (K_{DCO}), V_{CTRL} is fixed to a specific value within a range of 0.5$\sim$1.2V, and f_{DCO}s are measured with C_{DCO} variations. After then, the averaged K_{DCO} is calculated. Like the preceding, the same measurement is repeated in changes of DUTs and V_{DD}s, and results are summarized in Figure. 3.2 (b). The ratios between K_{DCO} and f_{DCO} (=K_{dg}), which are very important characteristics for the proposed PLL, are calculated as shown in Figure. 3.2 (c). K_{dg} is about 1.194mHz over whole frequency range, even though DUT or V_{DD} is varied. The K_{dg} errors defined as Error$(\%) = (1.194\text{mHz} - K_{dg})/1.194\text{mHz} \times 100$ are calculated as shown in Figure. 3.2 (d), verifying that K_{dg} has the error margin of only $\pm$10%. Therefore, the fabricated DCO can satisfy the condition which make the proposed PLL insensitive to N_{DIV} variations with an error of under 10% regardless of process and voltage variations.

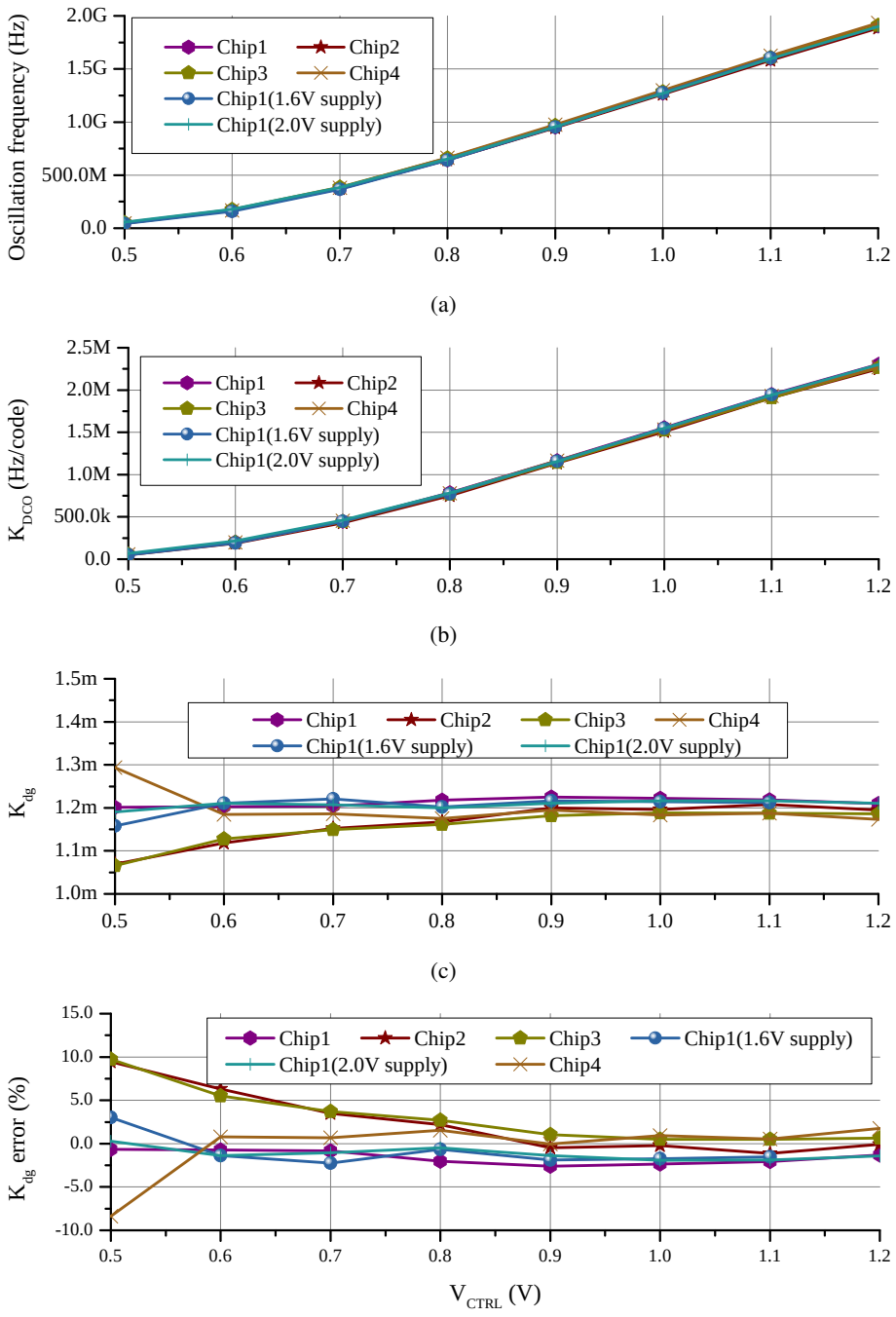


Figure 3.2: (a) Measured DCO frequency with C_{DCO}=0, (b) K_{DCO}, (c) K_{dg}, (d) K_{dg} error versus V_{CTRL}

3.2 PLL Measurement Results

Figure. 3.3 shows the measurement setup to verify the PLL operation. A reference clock having 25-MHz frequency is provided from a signal source. An 1.8-V supply voltage (V_{DD}) is supplied from a power supply. The PLL output signal which is synthesized clock in accordance with the reference clock and N_{DIV} is connected to a spectrum analyzer and an oscilloscope. Power spectrum densities (PSDs) and phase noises are measured by the spectrum analyzer. An eye-diagram and timing jitters are measured by the oscilloscope. N_{DIV} is decided by 3 toggle switches on the PCB.

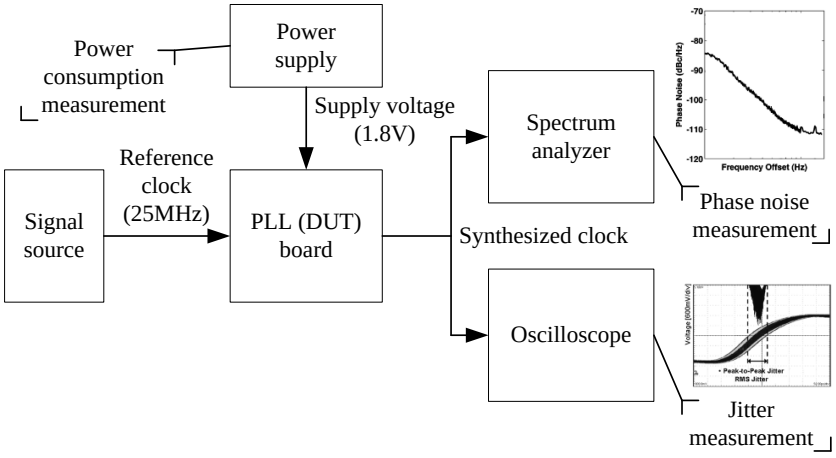
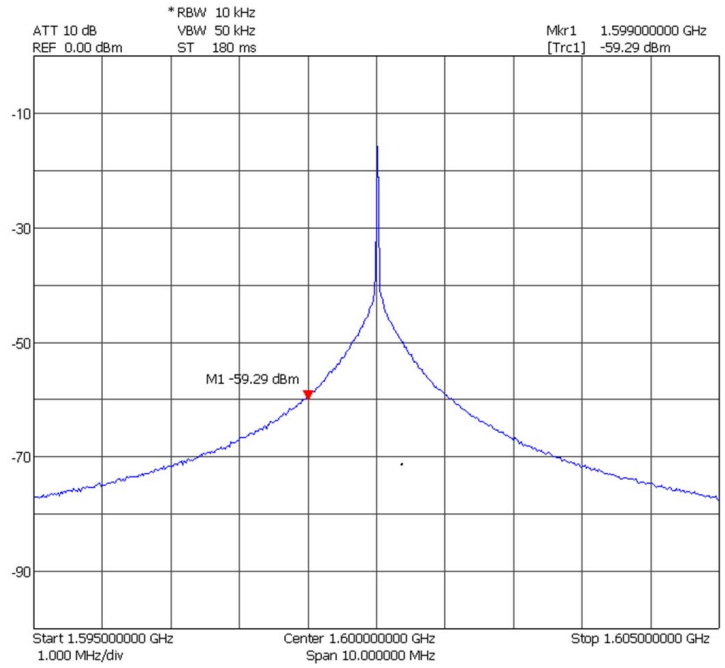
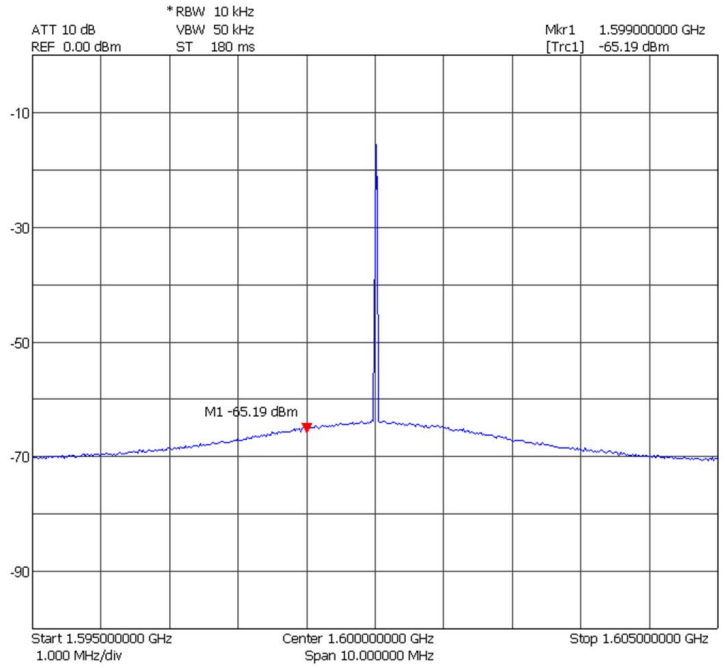


Figure 3.3: PLL Measurement setup

At first, the PLL is tested with N_{DIV} of 64 and no N_{DIV} variations. In order to verify that proposed PLL dynamics comply the digital loop having a wide loop bandwidth regardless of the AFC loop having a very narrow loop bandwidth, PLL performances are compared when the digital loop is turned on and off. If C_{DCO} is forcibly fixed an arbitrary value, the digital loop has no loop gain, and the PLL is identical with conventional CPPLLs. This condition means that the digital loop is turned off. Figure. 3.4 (a) and (b) show PSD results for two cases. When the digital loop is turned off, the PLL output spectrum has large low-frequency phase noises as shown in Figure. 3.4 (a), because almost all phase noises generated from DCO are transfered to the PLL output due to the very narrow AFC loop bandwidth. When the digital loop is turned on, the overall PLL loop bandwidth is dramatically extended, and low-frequency phase noises from DCO can be effectively reduced. As a result, the PLL output spectrum becomes much purer than the previous one as shown in Figure. 3.4 (b). This performance difference also can be observed in time domain by eye-diagram measurement. Figure. 3.5 (a) shows the result when the digital loop is turned off, where the PLL output quality is very poor. After the digital loop is turned on, the PLL jitter is dramatically reduced as shown in Figure. 3.5 (b) because low-frequency phase noises are suppressed which are critical in the jitter performance. The measured RMS jitter and peak-to-peak jitter in this case are about 9.96ps and 65.28ps, respectively. They are equal to 0.016UI (unit interval) and 0.1UI, respectively.

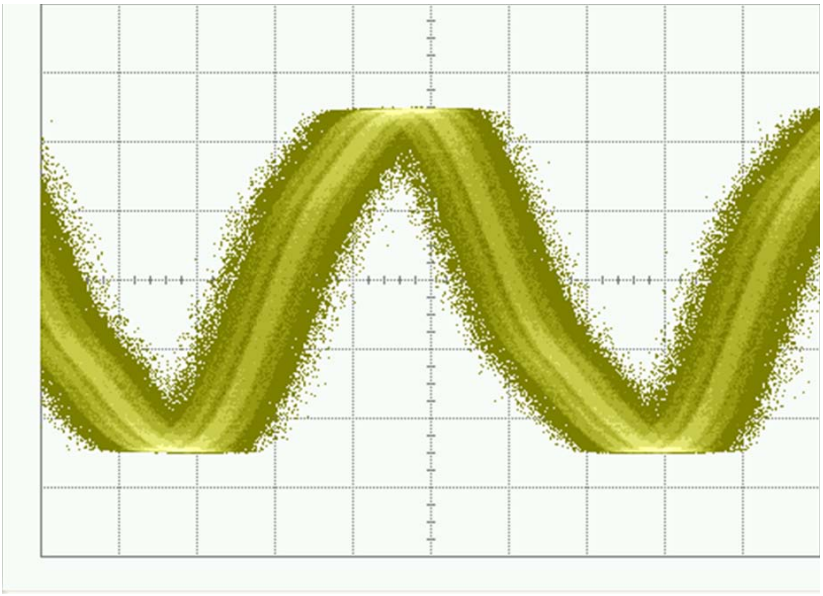


(a)

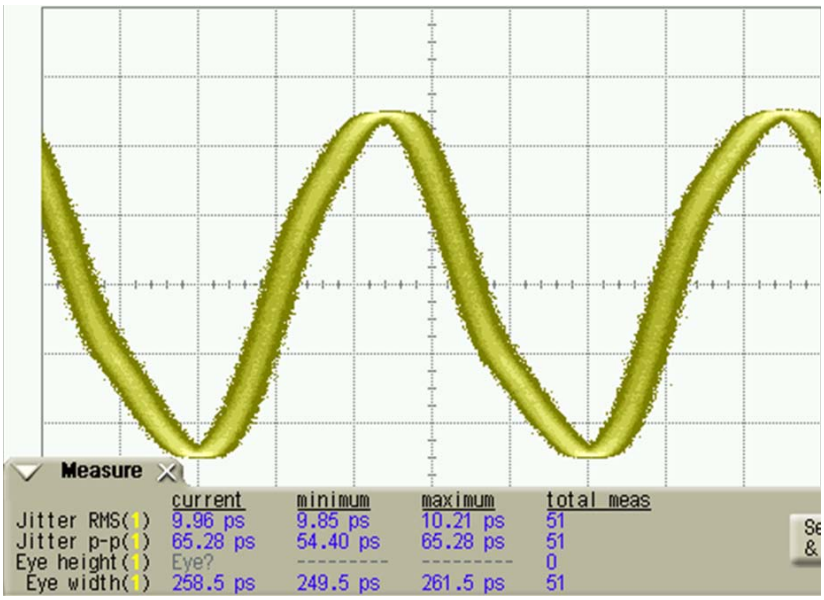


(b)

Figure 3.4: PSD results of 1.6-GHz output clock, when (a) digital loop is turned off, (b) digital loop is turned on



(a)



(b)

Figure 3.5: Eye-diagram results of 1.6-GHz output clock, when (a) digital loop is turned off, (b) digital loop is turned on

The PLL is also tested in several changes of N_{DIV} from 2 to 64. Figure. 3.6 shows PLL output spectrum results and power consumptions in accordance with N_{DIV} variations. From these results, it is verified that the implemented AFC works well, and the PLL can operate within a very wide output frequency range from 50MHz to 1600MHz, even though C_{DCO} and C_{TDC} have only 5-bit code. Power consumptions of the PLL core is varied within a range of 15mA$\sim$18mA according to the PLL output frequency.

However, unfortunately, jitter and phase noise performances are dissatisfied in most cases. At the beginning of the PLL operation, pure clock is generated for a little while. After some time, digital loop is turned off unintentionally, and the PLL starts to show poor performances like as Figure. 3.4 (a) and Figure. 3.5 (a). Although we tried quite a lot of the experiment, only one satisfactory result could be obtained, which are described in Figure. 3.4 (b) and Figure. 3.5 (b). Therefore, accurate phase noises, jitter transfer functions, and supply noise sensitivities could not be measured.

The reasons why the digital loop is turned off automatically are analyzed in the next section. And, the method how to avoid this problem is proposed in the next chapter.

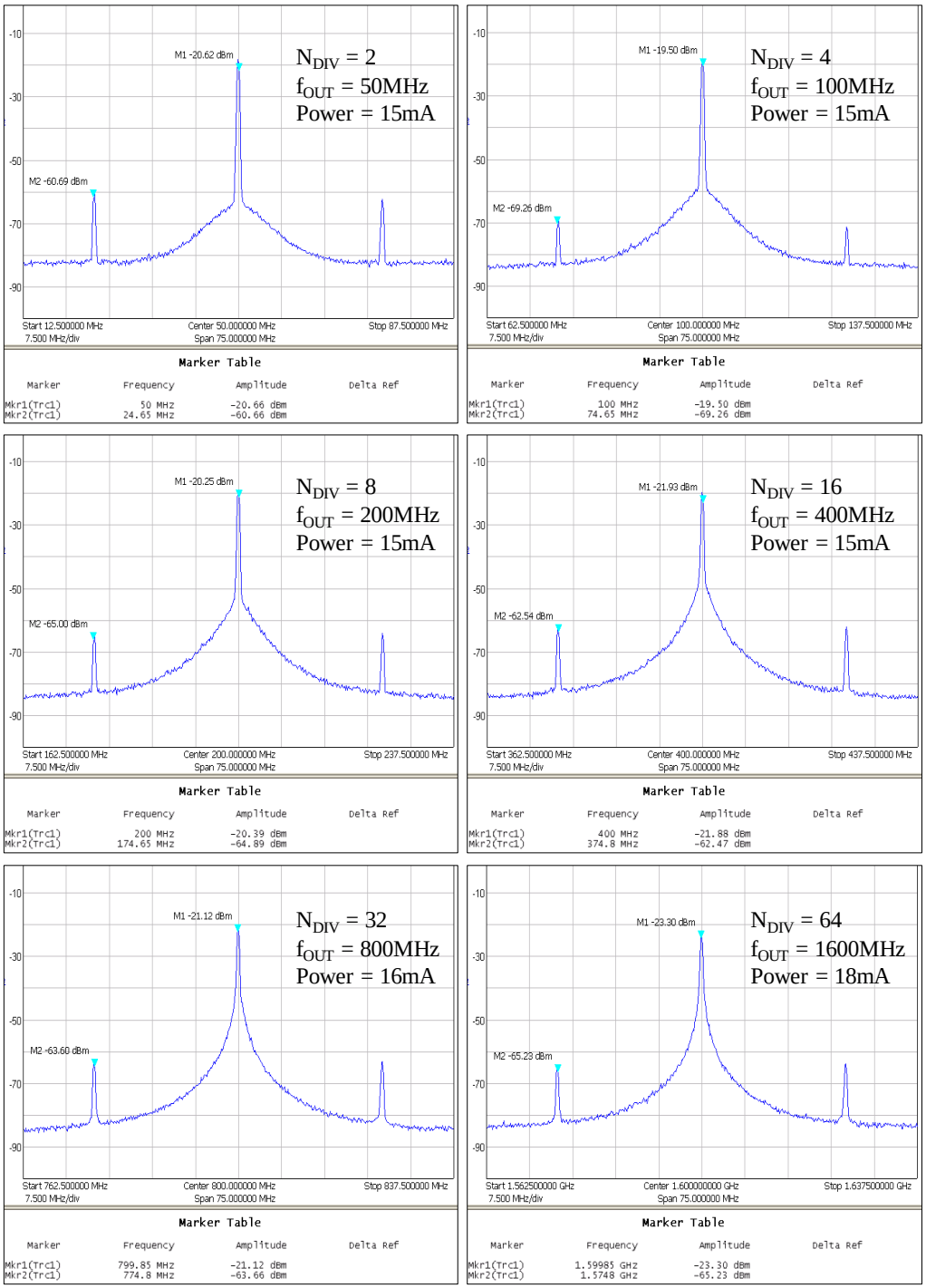


Figure 3.6: PSD results of output clock with N_{DIV} variations from 2 to 64

3.3 Problem Analysis

In this section, the reason of observed problem on the fabricated PLL chip is analyzed using behavioral SPICE simulation. Behavioral circuit models are implemented in Verilog-AMS [22]. The Verilog-AMS codes are given in the appendix.

Figure. 3.7 shows the simulation test-bench. Simulation parameters such as the TDC resolution (Δ_{TDC}) are marked under each building block. The LDO in Figure. 2.2 is skipped in the test-bench because $V_{DD;DCO}$ is equal to V_{CTRL} in the ideal situation.

Simulation parameters for the first trial are summarized in Table. 3.1. In the fabricated chip, f_{REF} and C_{TDC_max} are 25MHz and 31, respectively. However, in order to reduce the simulation time, large C_{TDC_max} and high f_{REF} are used. N_{DIV} is fixed to 8. K_{DCO} and K_{VDO} are decided according to measurement results. Δ_{TDC} and I_{CPunit} are decided according to the building block simulation results. The phase margin for the digital loop (θ_{mD}), the unit-gain bandwidth for the AFC loop (ω_n), and the unit-gain bandwidth for the digital loop (ω_{ugbw}) are set at the values mentioned in the previous chapter. Filter coefficients for LF and DLF are calculated using Eq. 2.4 and Eq. 2.7, respectively. Because D_{RST}, D_{Update} for PFD and TDC has a negligible effect on the PLL operation, they are arbitrarily set at reasonable values. f_0 means the DCO center frequency whose value is f_{DCO} with C_{DCO} of 0 and V_{CTRL} of 0.5V. I_{leak} means the charge pump leakage current. In this step, I_{leak} is fixed to 0.

Figure. 3.8 shows simulation results. After the phase is locked, C_{TDC} has a zero value on average, and the MLCP output current becomes also zero on average. Therefore, V_{CTRL} is perfectly fixed to the value for f_{DCO} of 1.6GHz, and C_{DCO} is toggled between

two adjacent values as we intended.

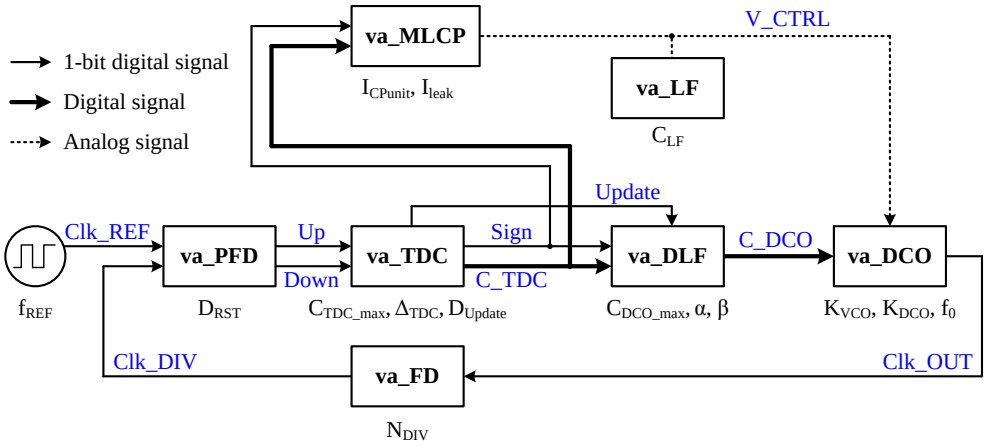
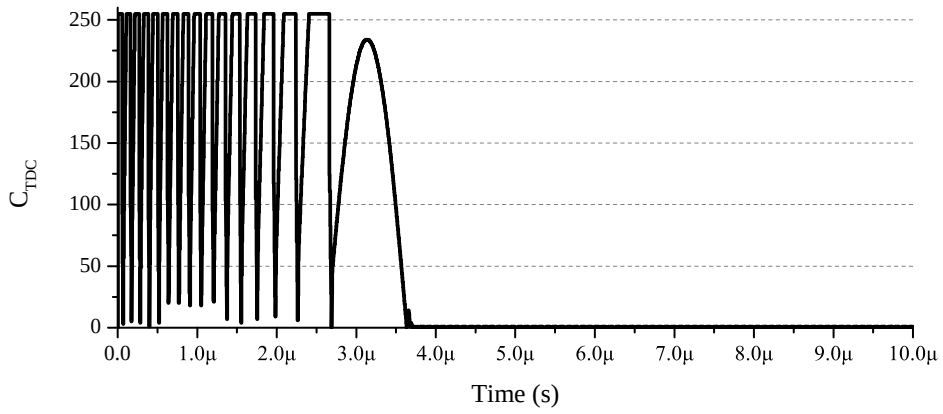


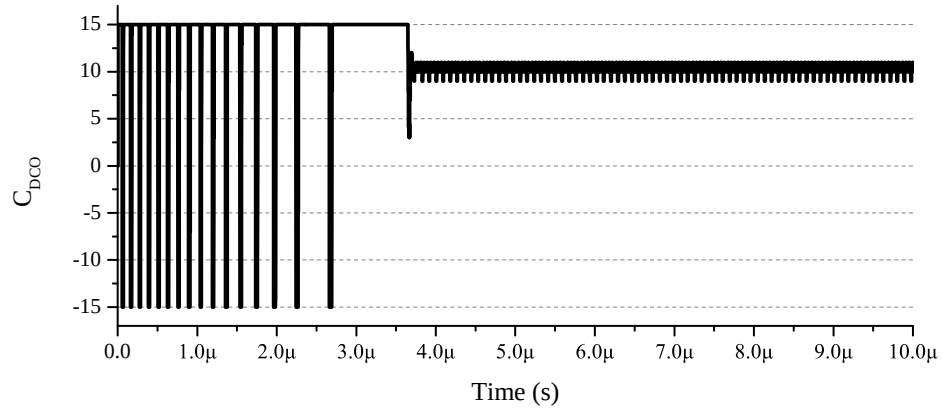
Figure 3.7: Behavioral simulation test-bench for problem analysis

Table 3.1: Simulation parameters

f_{REF}	200MHz	D_{RST}	1ns
N_{DIV}	8	D_{Update}	2ns
K_{DCO}	1.91MHz/LSB	C_{TDC_max}	255
K_{VCO}	3.27GHz/V	C_{DCO_max}	15
f_0	1.6GHz	ϕ_{mD}	$\frac{2\pi}{6}$
Δ_{TDC}	7.78ps	ω_n, ω_{ugbw}	$\frac{2\pi f_{REF}}{400}$, $\frac{2\pi f_{REF}}{10}$
I_{CPunit}	3μA	α, β	0.1367, 0.01029
I_{leak}	0	C_{LF}	79.85nF



(a)



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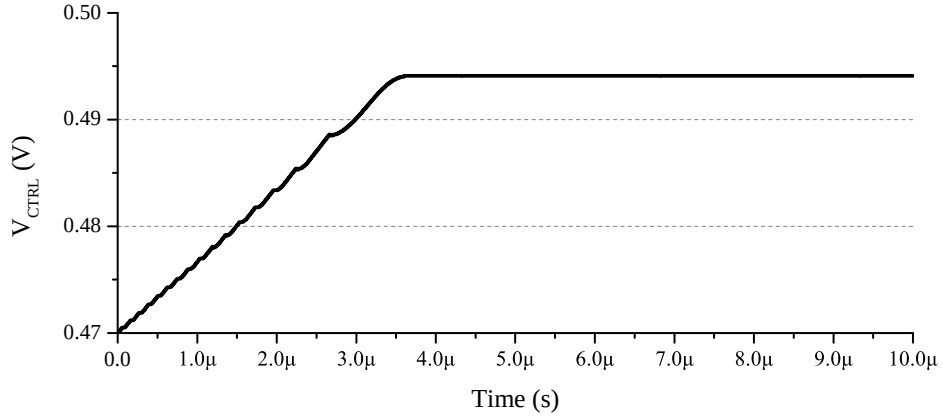


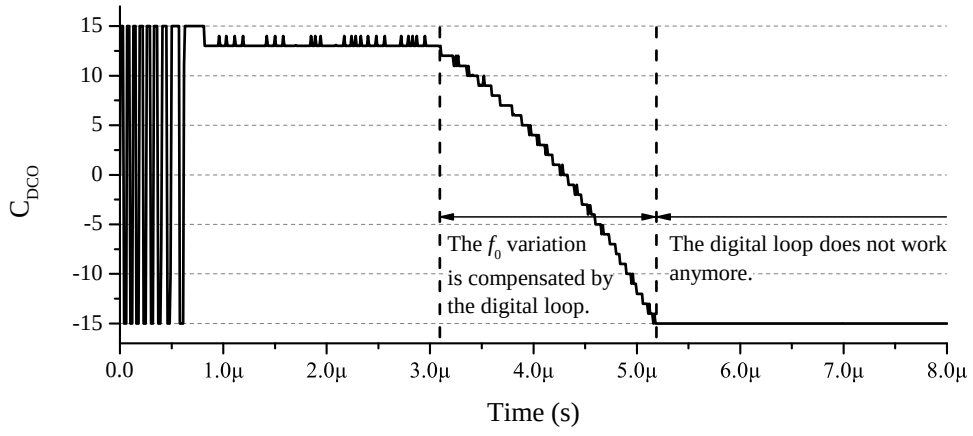
(c)

Figure 3.8: Behavioral simulation results without leakage currents and f_0 variations, (a) C_{TDC}, (b) C_{DCO}, (c) V_{CTRL}

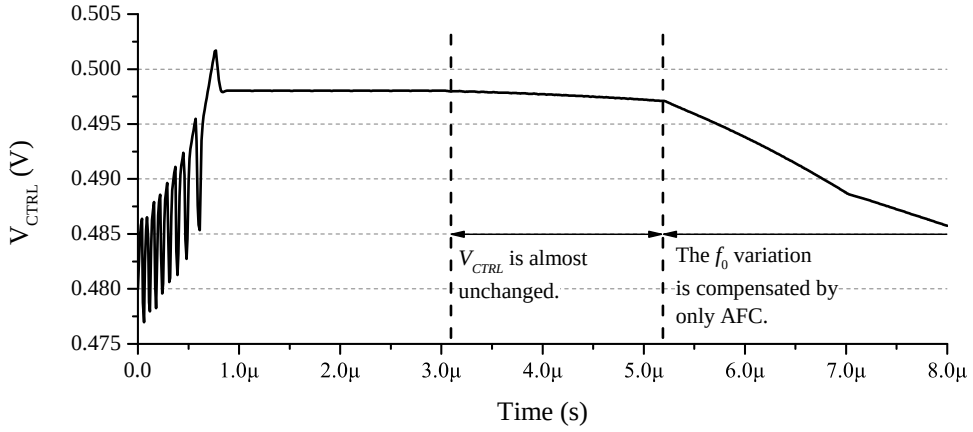
With ideal conditions (I_{leak} of zero and fixed f_0), the observed problem of the fabricated PLL chip mentioned in the previous section does not exist in the simulation. However, in reality, it is impossible to make I_{leak} zero completely. f_0 is also hard to be fixed completely due to voltage and temperature variations and circuit noises. If f_{DCO} excessively drifts as time goes on after the phase is locked by leakage currents or DCO frequency characteristic variations (f_0 variations), and C_{DCO} is saturated to its maximum or minimum value, the problem can be found in the simulation.

Figure. 3.9 shows simulation results with f_0 variations on the time. Before C_{DCO} is saturated to the minimum value (-15), f_0 variations are compensated mainly by the digital loop, while V_{CTRL} is almost unchanged. After C_{DCO} is saturated, the digital loop does not work anymore and the phase-locking condition is maintained by only AFC. A leakage current also induces similar phenomenon. Figure. 3.10 shows the simulation results with I_{leak} of 10μA. During a specific time interval, the digital loop can compensate V_{CTRL} drop. However, after C_{DCO} is saturated, the digital loop does not work anymore like the preceding. In this simulation, a very large I_{leak} is used for the simulation time. In reality, the charge pump leakage current is very small under 100nA. However, if I_{leak} is not completely zero, it is not able to avoid the phenomenon regardless of the I_{leak} magnitude.

Based on these simulation results, we guess that the abnormal behavior of the fabricated PLL chip is caused by the frequency drift due to charge pump leakage currents and DCO frequency characteristic variations as mentioned above. How to solve this problem is discussed in the next chapter.



(a)



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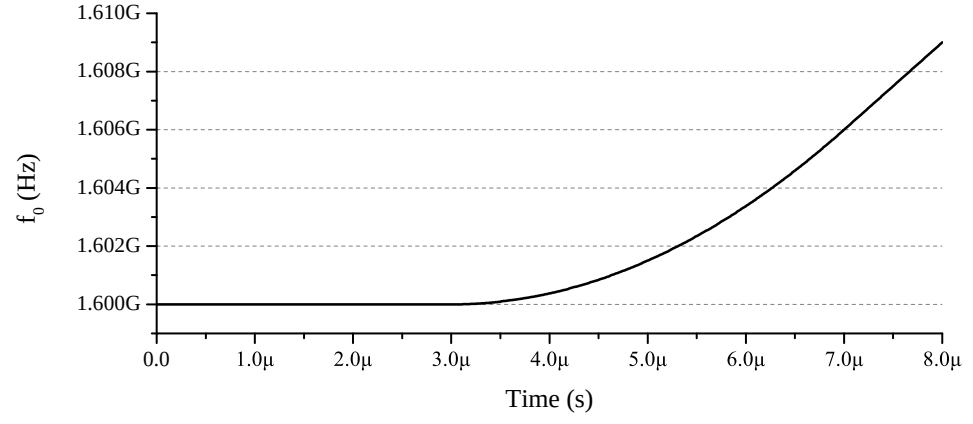
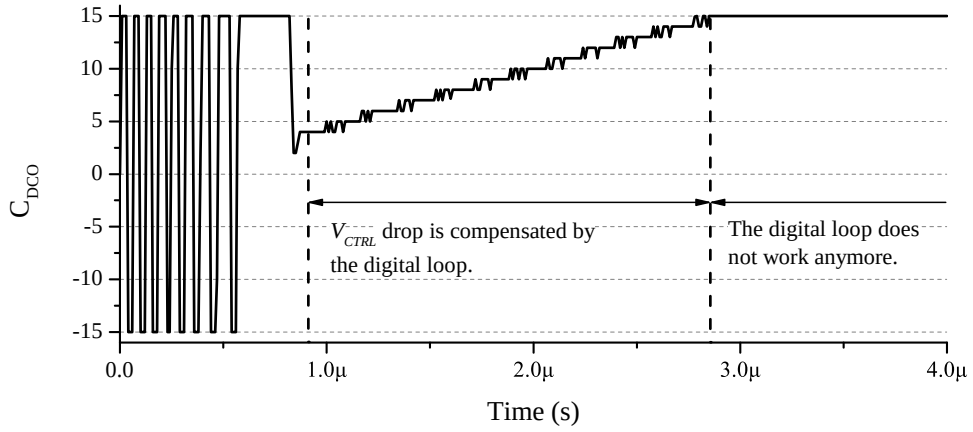
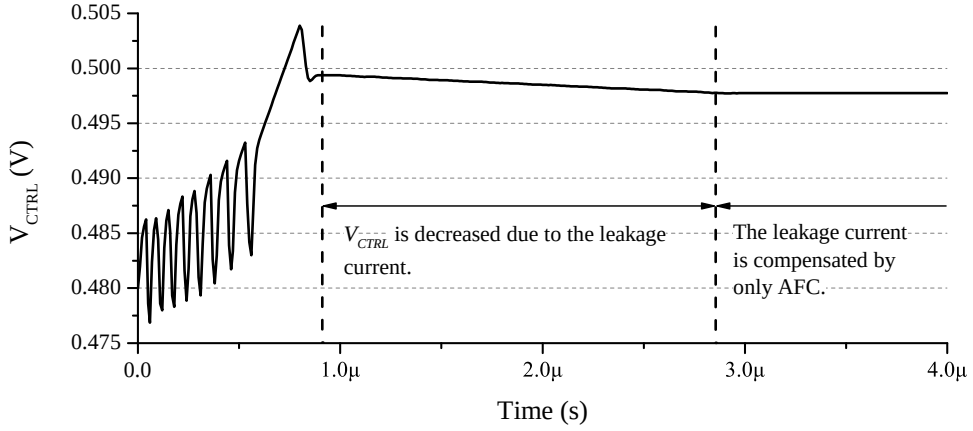


(c)

Figure 3.9: Behavioral simulation results with f_0 variations, (a) C_{DCO}, (b) V_{CTRL}, (c) f_0



(a)



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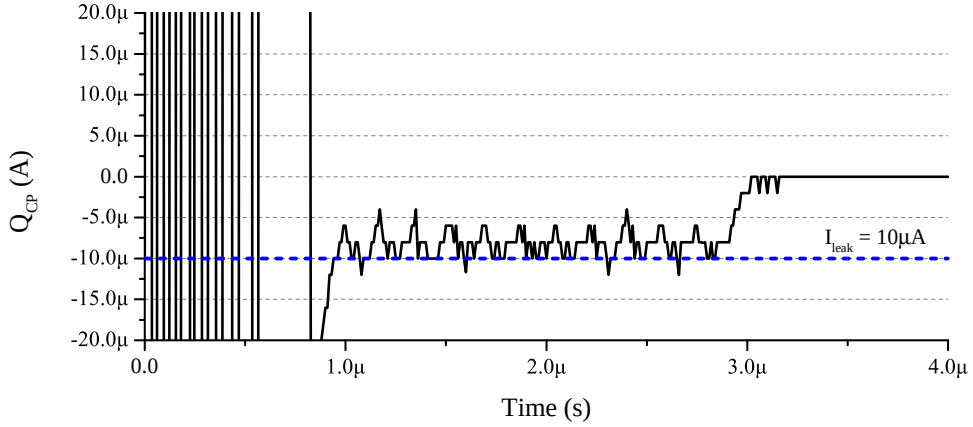


(c)

Figure 3.10: Behavioral simulation results with a leakage current of 10μA, (a) C_{DCO}, (b) V_{CTRL}, (c) MLCP output current

Chapter 4

Modified PLL Architecture

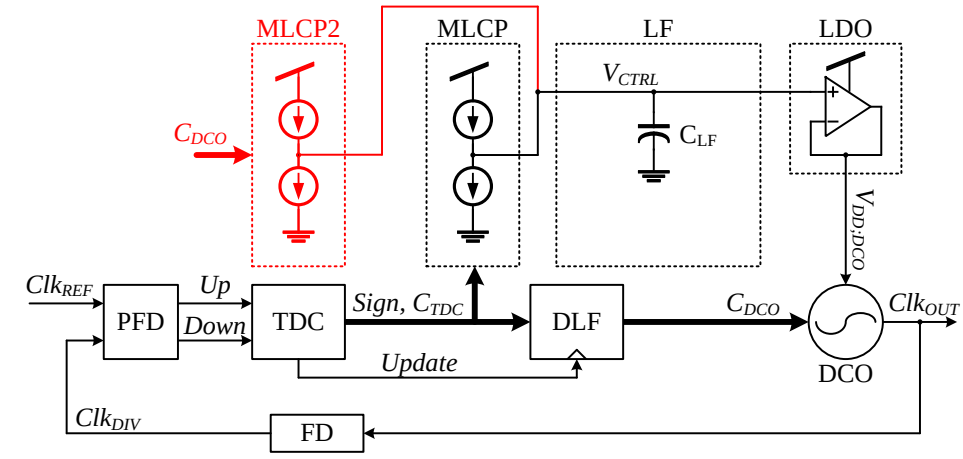
In this chapter, how to solve the observed problem of the fabricated PLL chip mentioned in the previous chapter is discussed in section 1. Furthermore, how to make the PLL always have optimum loop dynamics is discussed in section 2, even though PVT conditions, N_{DIV}, and f_{REF} are varied unintentionally. In section 3, noise simulation results of the modified PLL are given.

4.1 AFC Compensator for Frequency Drift

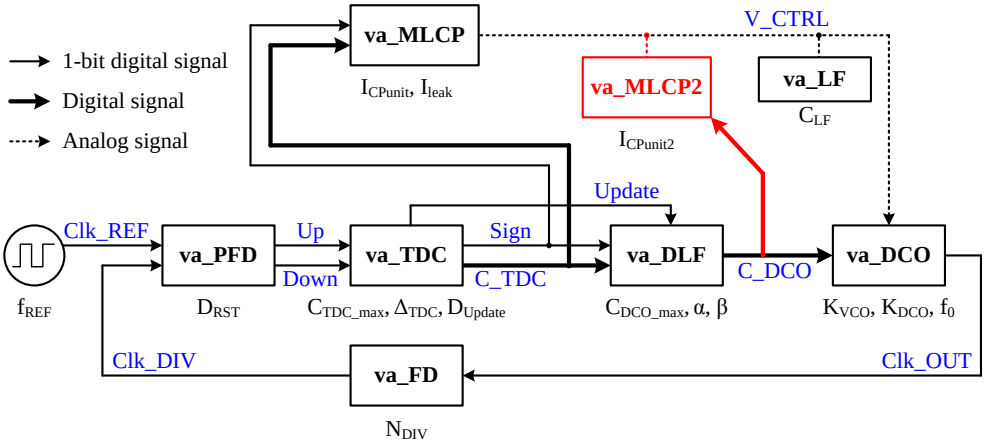
4.1.1 Modified Architecture

As mentioned in section 3.3, the problem that the digital loop is turned off is happened when C_{DCO} is saturated by the DCO frequency drift. In order for C_{DCO} not to reach the boundary (C_{DCO_max} or $-C_{DCO\_max}$), another MLCP (MLCP2) which generates a current signal in accordance with the DCO control signal (C_{DCO}) is added as shown in Figure. 4.1 (a). If C_{DCO} is larger than zero, a positive current is charged to the loop filter, V_{CTRL} is increased, and C_{DCO} is decreased until C_{DCO} reach the zero value, and vice versa. As a result, after the phase is locked, C_{DCO} value is converged to zero.

To verify this phenomenon, behavioral simulations with f_0 variations or a leakage current are performed using the simulation test-bench shown in Figure. 4.1 (b), where $I_{CPunit2}$ is the current magnitude per LSB of MLCP2. To reduce the simulation time, large loop bandwidth is used for this step. Figure. 4.2 and 4.3 show the simulation results. Without MLCP2, C_{DCO} reaches its minimum or maximum value due to f_0 variations or the leakage current, like as the results of Figure. 3.9 and 3.10. However, if MLCP2 is included, V_{CTRL} is compensated for C_{DCO} to be converged to zero as time goes on. Therefore, the digital loop can always work even though the DCO frequency characteristic is varied by voltage or temperature variation on time, or a static leakage current affects V_{CTRL}.

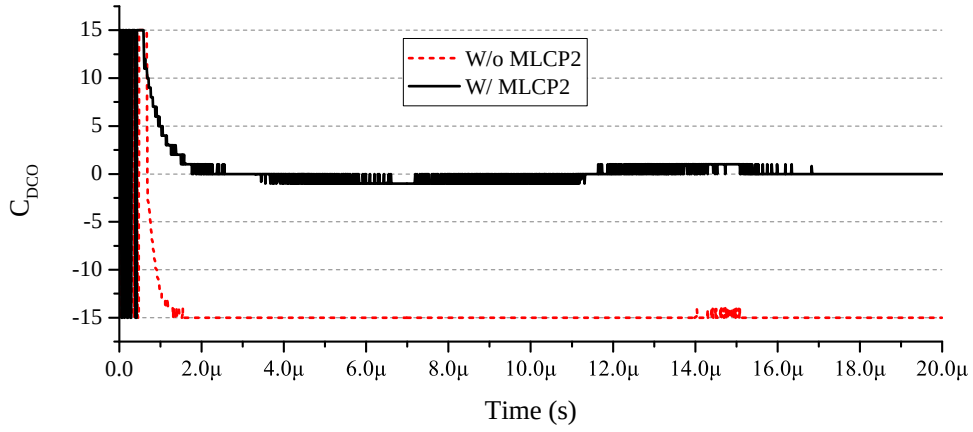


(a)

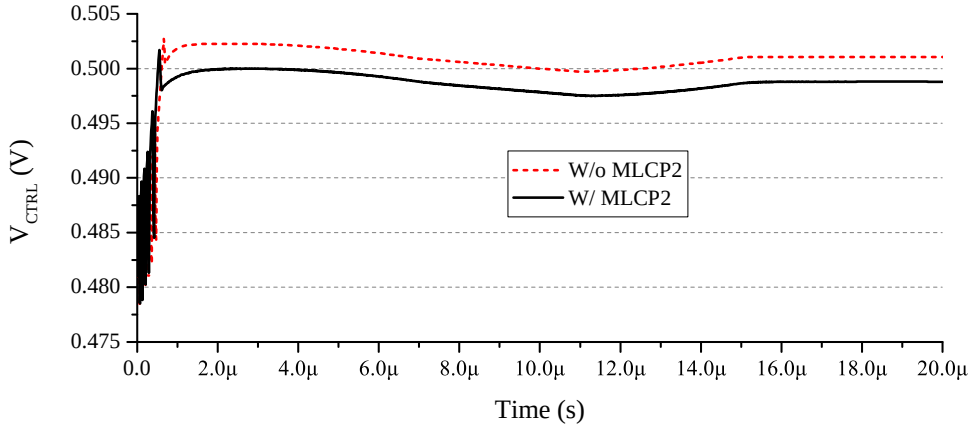


(b)

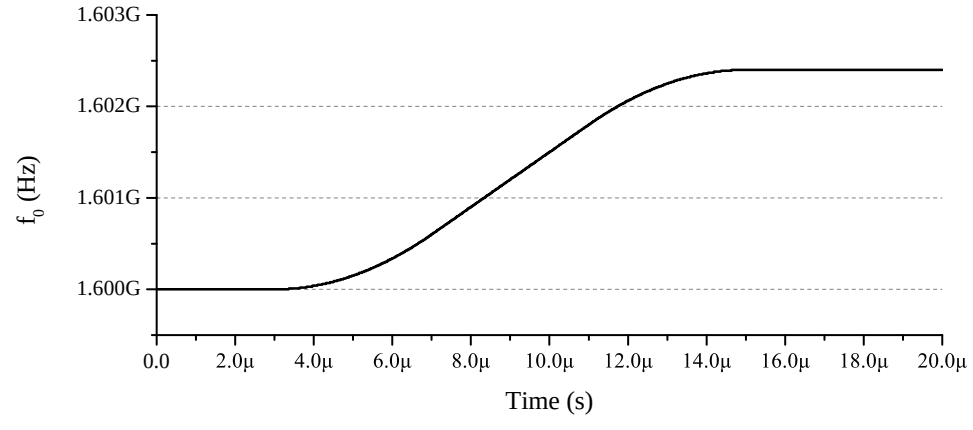
Figure 4.1: (a) Block-diagram of modified PLL including an AFC compensator, (b) simulation test-bench



(a)

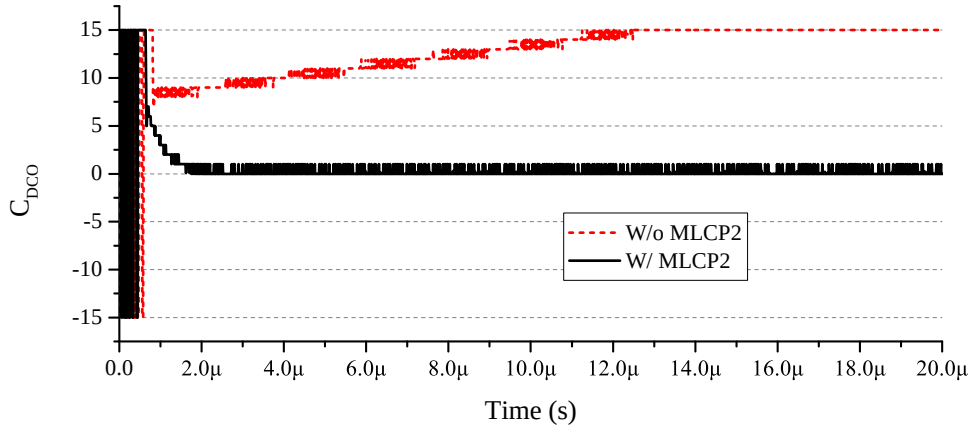


(b)

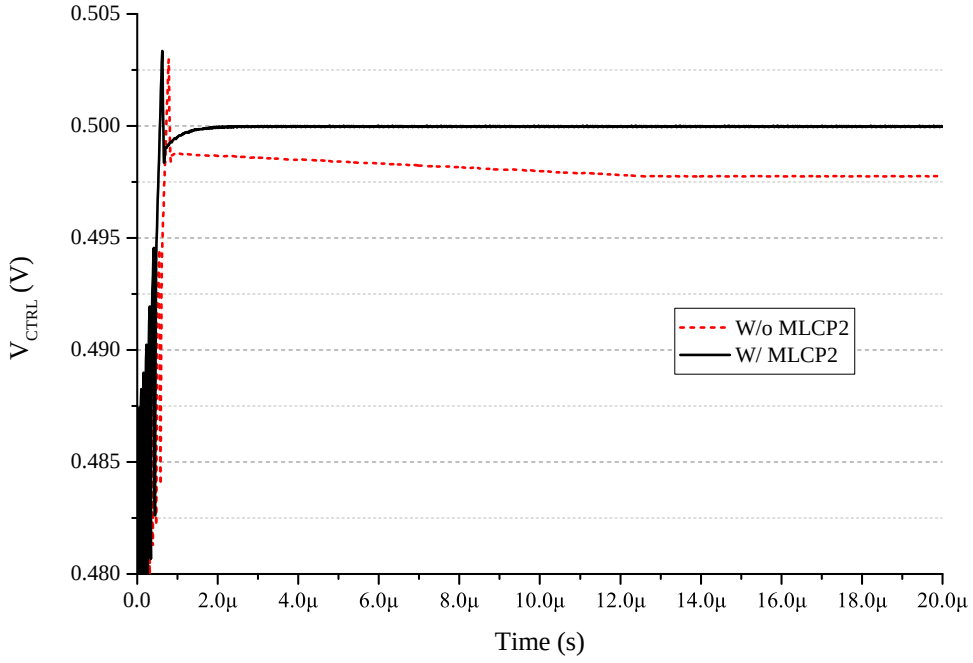


(c)

Figure 4.2: Behavioral simulation results of modified PLL with f_0 variations, (a) C_{DCO}, (b) V_{CTRL}, (c) f_0



(a)

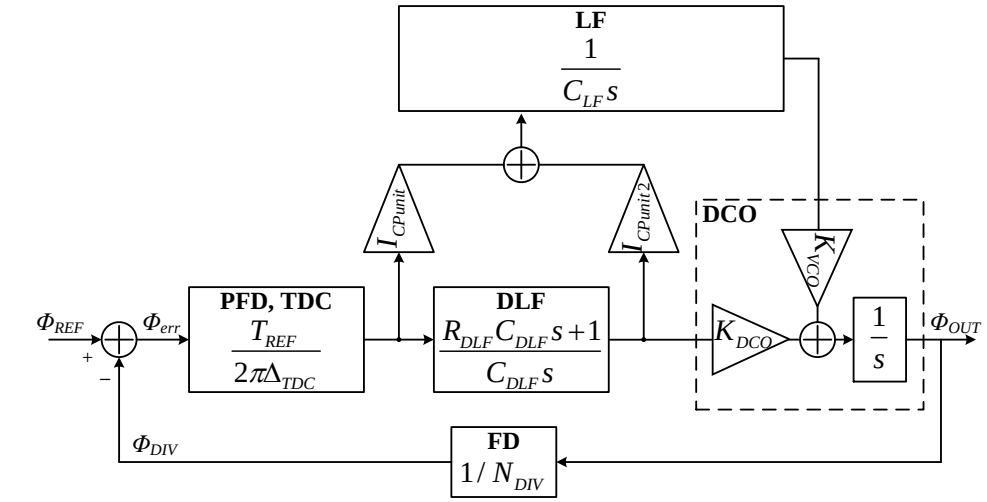


(b)

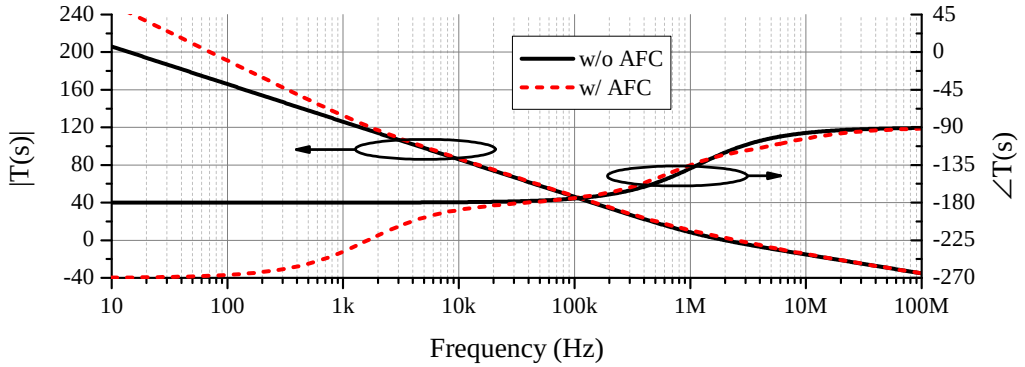
Figure 4.3: Behavioral simulation results of modified PLL with a leakage current, (a) C_{DCO}, (b) V_{CTRL}

4.1.2 Loop Dynamics Analysis

Figure. 4.4 (a) shows the small-signal model of the modified PLL. By the addition of MLCP2, a zero and a pole are added in the overall PLL dynamics, where the pole is at the origin. However, the PLL stability, the loop bandwidth, the phase margin, and the jitter peaking are not changed significantly by MLCP2 because the additional zero frequency is very low. Figure. 4.4 (b) and (c) show the PLL open-loop gain and the closed-loop gain, respectively, where f_{REF} is 100MHz, N_{DIV} is 10, K_{DCO} is 300kHz, K_{VCO} is 2GHz, I_{CPunit} is 2μA, and $I_{CPunit2}$ is 1μA. In comparison with the intrinsic digital loop dynamics, overall dynamics of the modified PLL is not different significantly.



(a)



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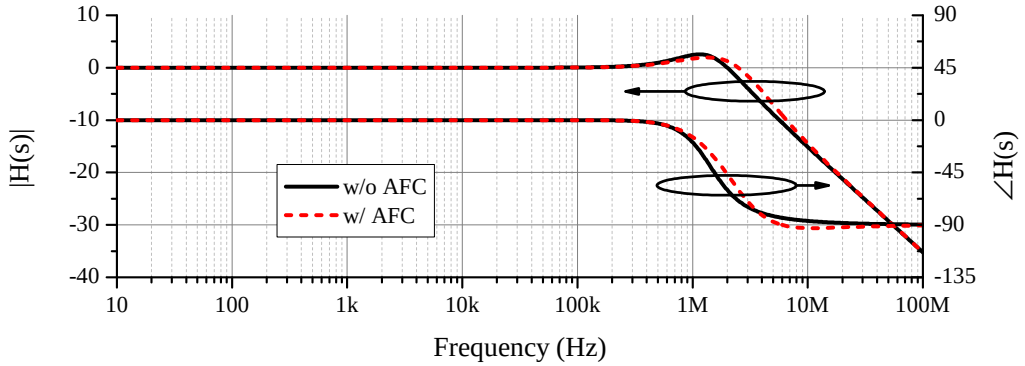


(c)

Figure 4.4: (a) Small-signal model of modified PLL, (b) open-loop gain plot, (c) closed-loop gain plot

4.1.3 Circuit Implementation

The MLCP2 circuit is identical with the MLCP circuit shown in Figure. 2.20, except the controller circuit. Because C_{DCO} inherently has the direction information, it can be easily converted to 16 $\overline{up}$ signals and 16 dn signals by simple inverter array as shown in Figure. 4.5, where the figure is the example of the case that C_{DCO} has 4 bits.

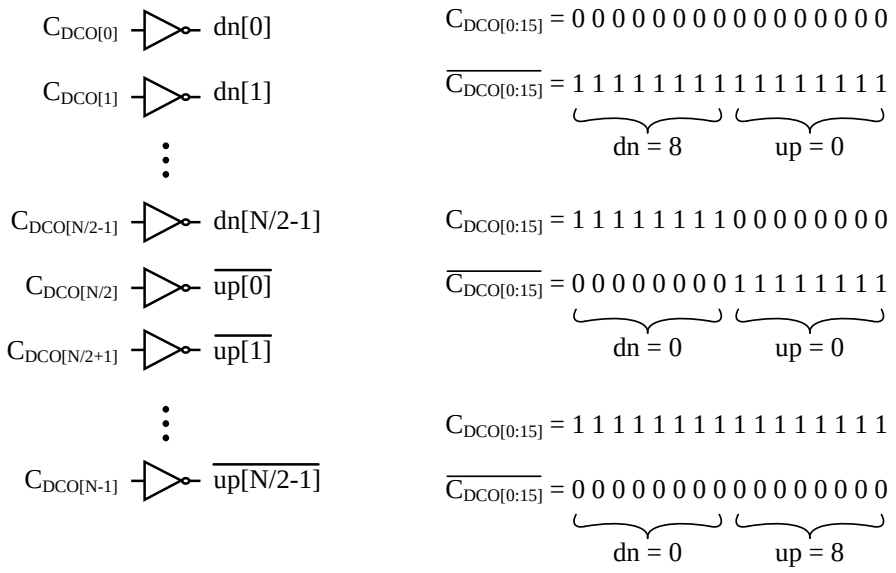


Figure 4.5: MLCP2 controller example

4.2 TDC Resolution Calibrator for Dynamics Optimization

4.2.1 Purpose

The PLL loop bandwidth is constrained by the reference frequency in order to avoid instability due to the sampling delay. However, for the optimum PLL jitter performance, the self-induced noise, e.g., DCO noise, should be rejected as much as possible, thus the loop bandwidth should be maximized in so far as the stability is guaranteed. Usually, the loop bandwidth is about ten times small than the reference frequency.

If the PLL loop bandwidth is fixed, and the reference frequency can be varied within a certain range, the loop bandwidth must be decided for the minimum reference frequency. However, in this case, the PLL will have suboptimal performance when the reference frequency is larger than the minimum. On the contrary to this, if the loop bandwidth is adaptive to the reference frequency as shown in Figure. 4.6, the PLL can have best performance regardless of the reference frequency variation [23]. Furthermore, PVT variations can lead to uncertainties in loop dynamics parameters such as K_{DCO} and Δ_{TDC}. These uncertainties force a designer to choose a conservative operating point that guarantees stable operation for all conditions, which is unfortunately not the best performance point in most cases. For example, Figure. 4.7 (a) shows the case with a typical CMOS DCO. The PVT variations cause the DCO frequency to vary by a factor of 2$\sim$3 between its slowest and fastest conditions. Therefore, the oscillator must have a wide enough tuning range to ensure operation at the target frequency, even if the target frequency is just a single point. Figure. 4.7 (b) shows the variation in loop bandwidth due to variation in the DCO gain. To guarantee stability, the designer must select the band-

width based on the worst case condition, resulting in suboptimal performance for all other cases.

To solve this problem, several PVT-tolerant ADPLL were reported [13][24][25][26]. In [13], K_{DCO} and Δ_{TDC} are measured and memorized before the PLL operation, and loop dynamics are calibrated based on that. However, if the parameters are varied as time goes on, they cannot be calibrated continuously. In [24], K_{DCO} and Δ_{TDC} are determined by the constant proportional relation based on a free-running ring oscillator. However, the PLL maximum frequency is very low, and the DCO resolution is hard to be fine, resulting in a poor jitter performance. In [25], a fractional-N frequency synthesizer based on a conventional CPPLL is used for a DCO. Therefore, K_{DCO} is strongly determined by the CPPLL reference frequency regardless of the PVT variations. Δ_{TDC} is also determined by the same reference frequency. However, [25] requires an additional reference frequency for CPPLL. The chip area burden of the CPPLL loop filter also can be a problem. In [26], K_{DCO} is measured during the PLL locking process, and the filter coefficient is calibrated. However, it also cannot calibrate the time-variant K_{DCO} variation like as [13].

In the next section, how the proposed PLL can be insensitive to PVT, f_{REF}, and N_{DIV} variations will be described. Note that the AFC loop bandwidth variation due to the variations in K_{VCO}, C_{LF}, I_{CPunit}, and $I_{CPunit2}$ is not significant because AFC has a very low loop bandwidth and negligible effects on the PLL. Therefore, the AFC loop dynamics are not treated in this section.

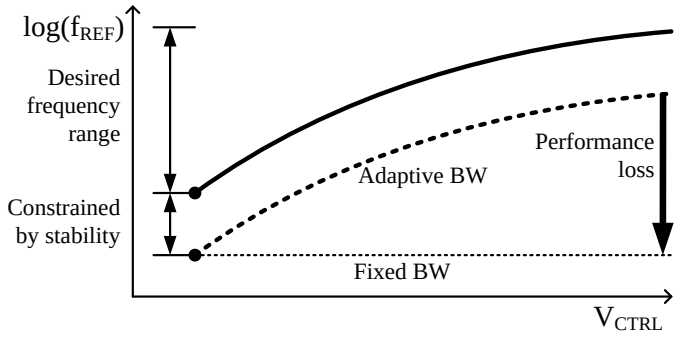


Figure 4.6: Adaptive bandwidth versus fixed bandwidth in case of a wide frequency range

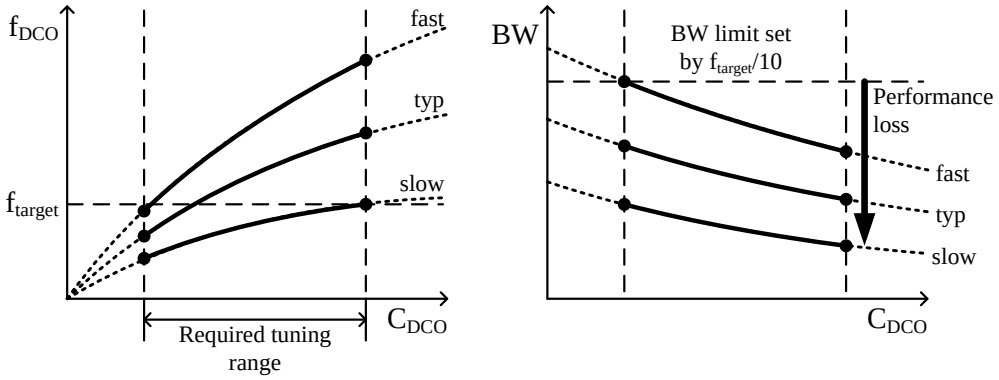


Figure 4.7: (a) Example of variation in DCO frequency, (b) variation in DCO gain due to PVT variations

4.2.2 PVT, N_{DIV} and f_{REF}-Tolerant PLL

In order for the PLL to always have the best jitter performance without any possibility for instability, the ADPLL loop dynamics optimization in regard to the PVT, f_{REF}, and N_{DIV} variations is important.

K_{DCO} in the fabricated PLL is proportional to the PLL output frequency with a PVT-insensitive proportional constant as verified by measurements. However, because Δ_{TDC} is influenced by PVT variations as shown in Figure. 2.18, PLL dynamics are still sensitive to PVT variations. Furthermore, if the PLL reference frequency is varied, DLF coefficients is adjusted for a optimum loop bandwidth as shown in Eq. 2.6.

If Δ_{TDC} can be inversely proportional to the reference frequency ($\Delta_{TDC} \propto 1/f_{REF}$), calculations for DLF coefficients can be simplified from Eq. 2.6 as the following equation.

$$
\begin{aligned}
&K_{DCO} = K_{dg} f_{REF} N_{DIV}, \qquad \Delta_{TDC} = \frac{K_{tr}}{f_{REF}}, \\
&\alpha = \frac{N_{DIV}\Delta_{TDC} f_{REF}^2}{K_{DCO}} \frac{2\pi \cdot 0.1}{\sqrt{\frac{1}{T^2}+1}} \left(1\text{-}\frac{2\pi \cdot 0.1}{2T}\right) = \frac{K_{tr}}{K_{dg}} \frac{2\pi \cdot 0.1}{\sqrt{\frac{1}{T^2}+1}} \left(1\text{-}\frac{2\pi \cdot 0.1}{2T}\right), \\
&\beta = \frac{N_{DIV}\Delta_{TDC} f_{REF}^2}{K_{DCO}} \frac{(2\pi \cdot 0.1)^2}{\sqrt{T^2+1}} = \frac{K_{tr}}{K_{dg}} \frac{(2\pi \cdot 0.1)^2}{\sqrt{T^2+1}}
\end{aligned}
\tag{4.1}
$$

, where $T = \tan\theta_{mD}$, K_{dg} and K_{tr} are the proportional constants for the DCO gain and the TDC resolution, respectively. From this equation, we can see that DLF coefficients for the loop unit-gain bandwidth (ω_{ugbw}) of $0.1 f_{REF}$ are unrelated to f_{REF} and N_{DIV}. And, if K_{tr} can be insensitive to PVT variations like as K_{dg}, the ratio between ω_{ugbw} and f_{REF} is not varied by f_{REF}, N_{DIV} or PVT variations even with the coefficients fixed at certain constants. In other words, if the assumptions (K_{DCO}=$K_{dg} f_{REF} N_{DIV}$, Δ_{TDC}=$\frac{K_{tr}}{f_{REF}}$,

K_{dg} and K_{tr} are PVT-insensitive constants) are satisfied, the PLL can always avoid instability and has the best jitter performance regardless of f_{REF}, N_{DIV} or PVT variations.

In order for satisfying the assumptions mentioned above, a Δ_{TDC} calibrator circuit is added as shown in Figure. 4.8. It can be implemented using several delay-locked loops (DLLs) [27]. With this scheme, Δ_{TDC} can be determined by the reference frequency only, regardless of PVT variations. The detailed circuit structure will be described in the next section.

The PLL including Δ_{TDC} calibrator is behaviorally simulated. The test-bench shown in Figure. 4.1 (b) is used again. However, simulation parameters are changed from the previous, which are summarized in Table. 4.1. The filter coefficients (α, β, C_{LF}) are fixed certain constants. K_{dg} and K_{tr} are determined as 0.0003 and 0.0001, respectively. K_{DCO} and Δ_{TDC} are calculated based on K_{dg} and K_{tr}, respectively.

Figure. 4.9 shows simulated open-loop gain and closed-loop gain with N_{DIV} and f_{REF} variations. From Figure. 4.9 (a) and (b), we can see that loop dynamics are almost unchanged by N_{DIV} variations. From Figure. 4.9 (c) and (d), we can see that the loop bandwidth is changed in accordance with f_{REF}. Figure. 4.10 summarizes the loop dynamics parameters (f_{ugbw}, jitter peaking, phase margin). They are negligibly affected by N_{DIV} and f_{REF} variations, except f_{ugbw} which is proportional to f_{REF}.

Figure. 4.11 and 4.12 show the transient simulation results. Even with the fixed filter coefficients, the PLL operates well without any worry for instability regardless of N_{DIV} and f_{REF}.

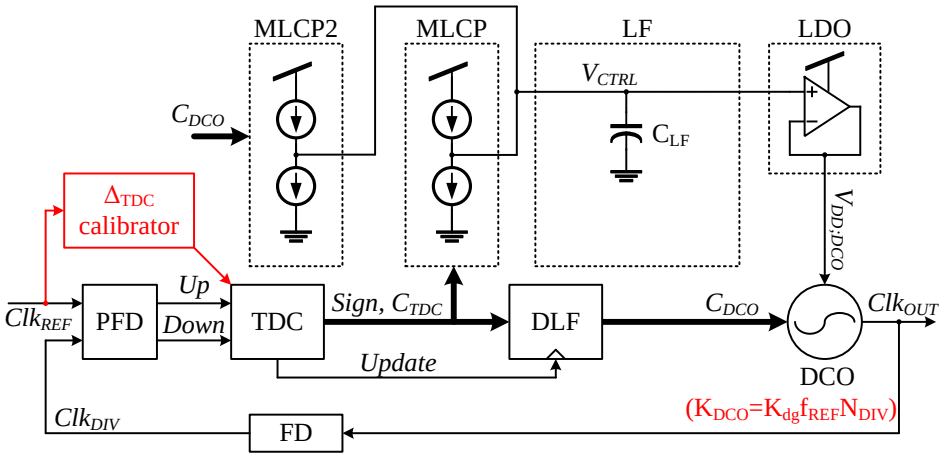


Figure 4.8: Block-diagram of secondly modified PLL

Table 4.1: Simulation parameters

f_{REF}	20∼200 MHz	D_{RST}	1ns
N_{DIV}	2∼20	D_{Update}	2ns
K_{DCO}	0.0003Hz/LSB$\times f_{REF}N_{DIV}$	C_{TDC_max}	255
K_{VCO}	2GHz/V	C_{DCO_max}	15
f_0	1GHz	α	3.496×10^{-2}
Δ_{TDC}	$0.0001\text{s}/f_{REF}$	β	2.632×10^{-3}
I_{CPunit}	2μA	C_{LF}	8.775μF
$I_{CPunit2}$	1μA	I_{leak}	0

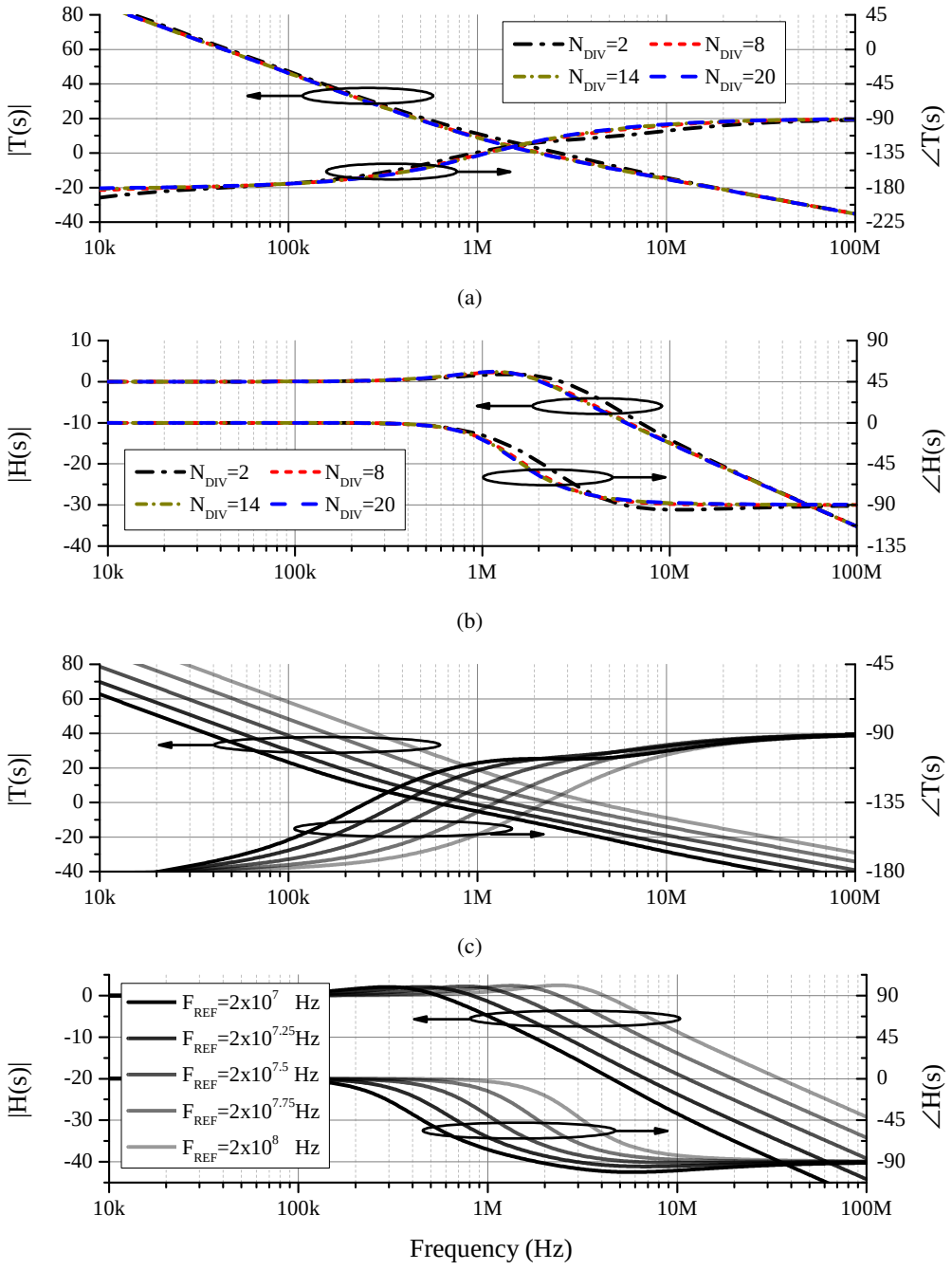
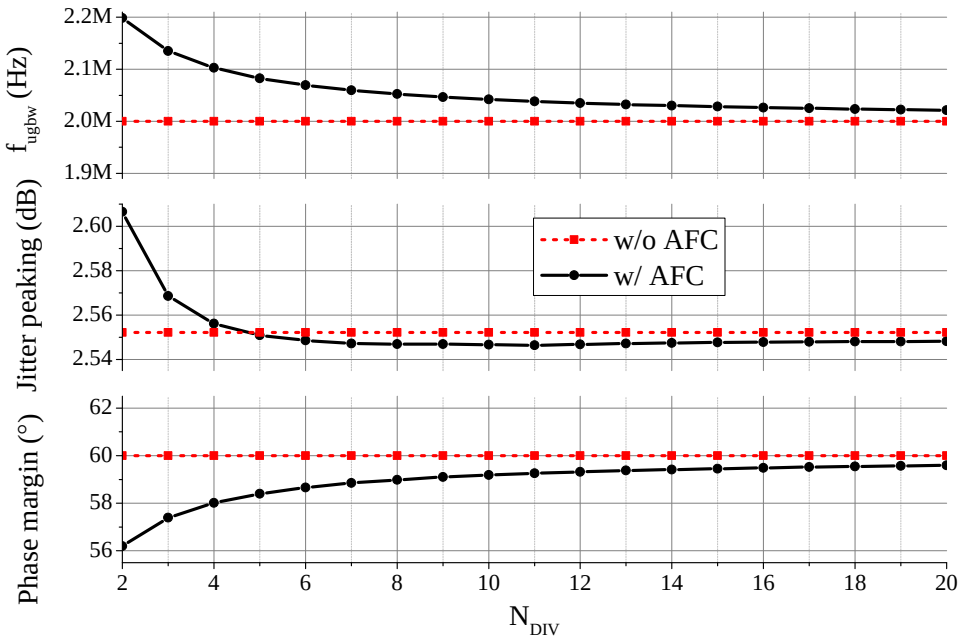
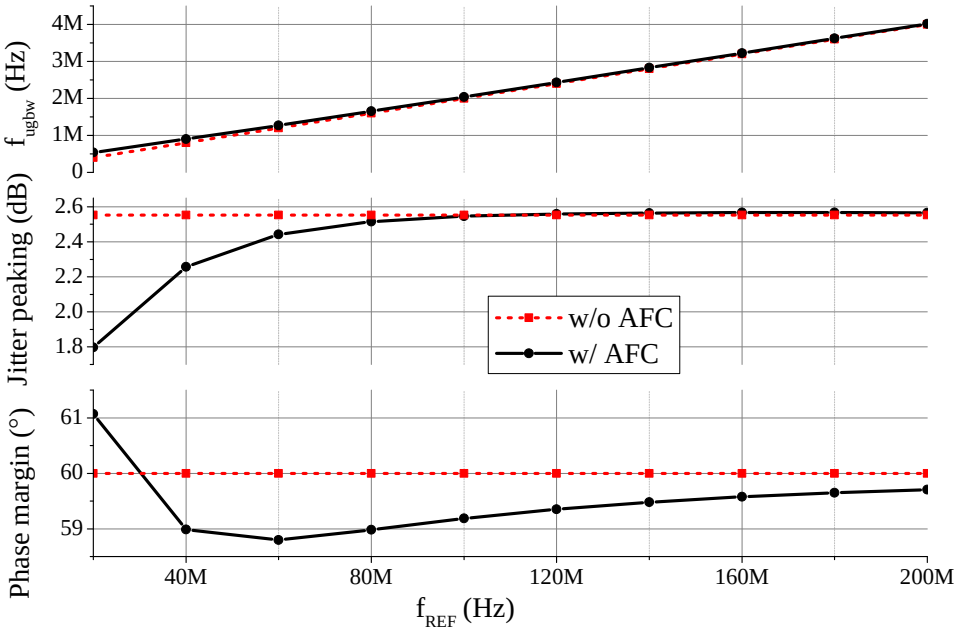


Figure 4.9: Small-signal transfer function of secondly modified PLL, (a) open-loop gain, (b) closed-loop gain with N_{DIV} variation, (c) open-loop gain, (d) closed-loop gain with f_{REF} variation



(a)



(b)

Figure 4.10: Unit-gain bandwidth, jitter peaking, phase margin of secondly modified PLL with (a) N_{DIV} variations, (b) with f_{REF} variations

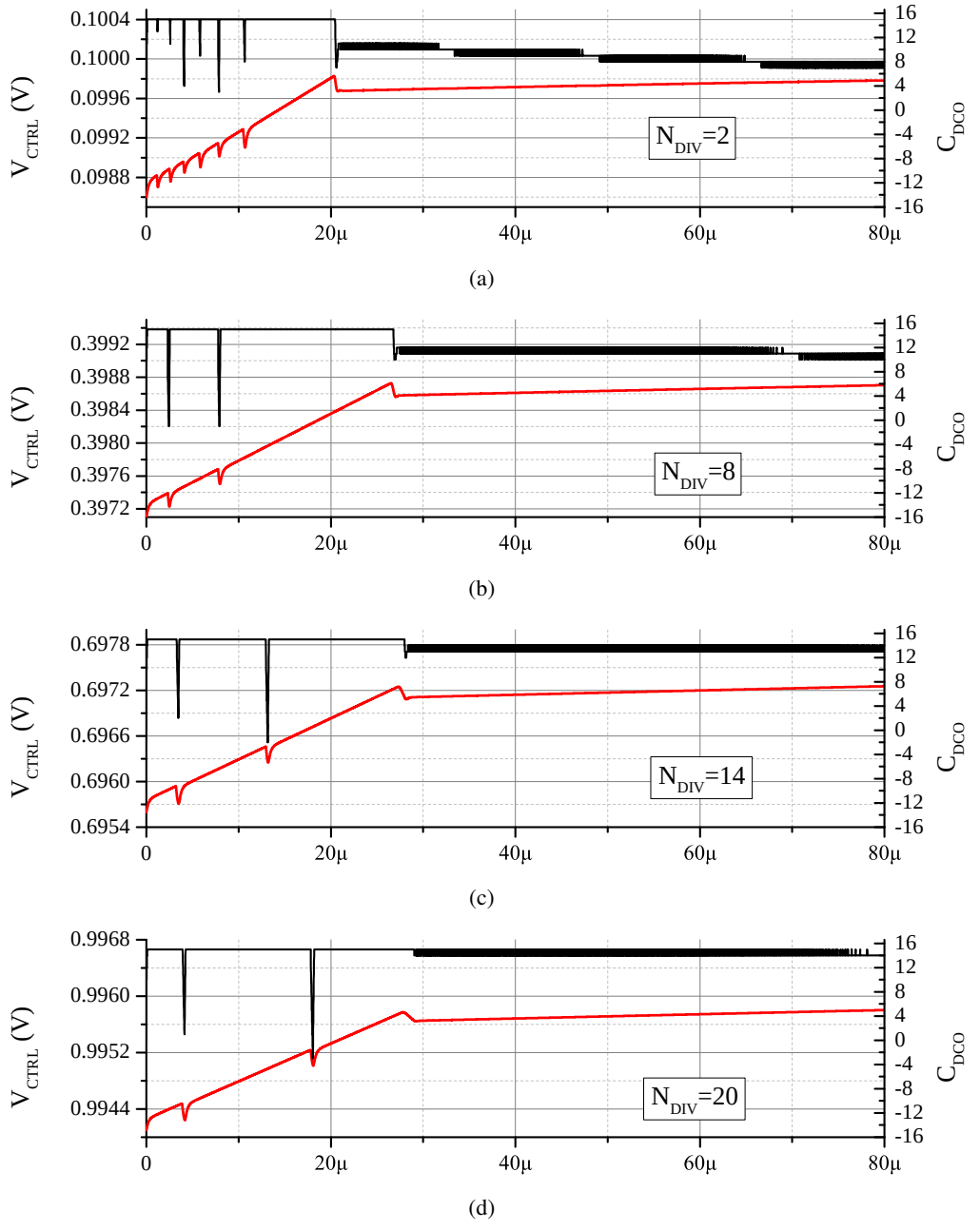


Figure 4.11: Behavioral simulation results of secondly modified PLL with N_{DIV} variations

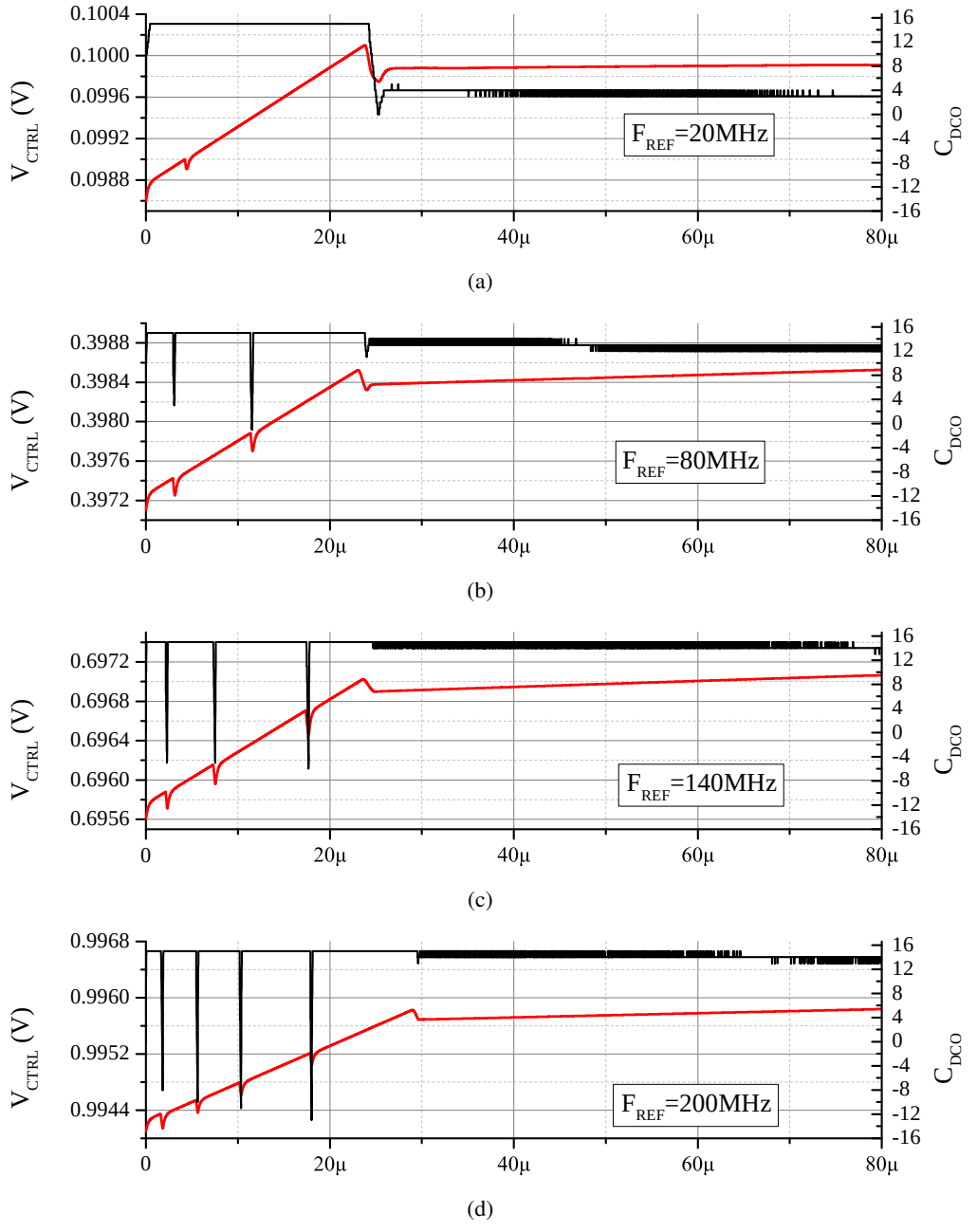


Figure 4.12: Behavioral simulation results of secondly modified PLL with f_{REF} variations

4.2.3 Circuit Implementation

Figure. 4.13 (a) shows schematics of conventional Δ_{TDC} calibrator which is made up of two DLLs [27]. The first DLL has N+1 delay stages, and the second DLL has N delay stages. After two DLLs are locked with the DLL reference clock (REF_{DLL}), and VDL TDC delay cells are adjusted in accordance with control voltages of two DLLs (b_{slow}, b_{fast}), Δ_{TDC} can be calculated as the following equation.

$$t_f = T_R/(N+1), \qquad t_s = T_R/N,$$
$$\Delta_{TDC} = t_s - t_f = \frac{T_R}{N(N+1)} \tag{4.2}$$

, where T_R is the period of REF_{DLL}, and t_f and t_s are delay times of delay cells in the first DLL and the second DLL, respectively. By the use of this calibrator, Δ_{TDC} can be determined by T_R and N only, regardless of PVT variations.

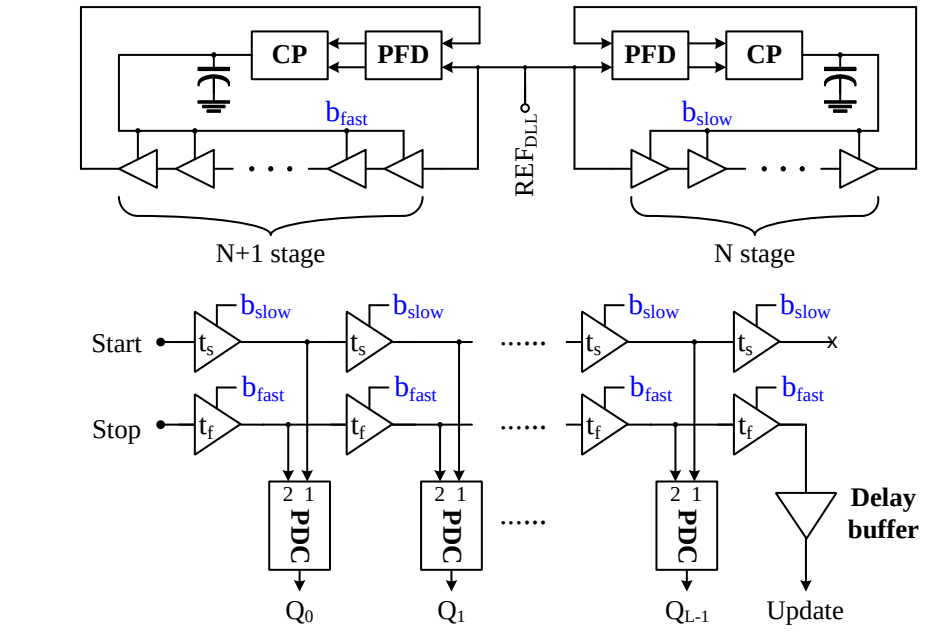
However, the PLL reference clock (Clk_{REF}) is hard to be used for REF_{DLL} because it has a very low frequency in general, and a very large N is required for a fine Δ_{TDC}. For example, if f_{REF} is 25MHz, required N is 72 for about 7.6-ps resolution. Totally 144 delay cells are required for two DLLs, resulting a large power consumption and a large chip area. The DCO output clock (Clk_{OUT}) can have much higher frequency than Clk_{REF}, but it is also hard to be used for REF_{DLL} because its frequency is varied by N_{DIV}, making Δ_{TDC} dependent to N_{DIV}.

In order to solve this problem, a novel Δ_{TDC} calibrator based on a quadruple-DLL is proposed as shown in Figure. 4.13 (b). It is made up of four DLLs (DLL1$\sim$DLL4). Both of the DLL1 and the DLL2 have N stage. The DLL3 and the DLL4 have N+1 stage and N-1 stage, respectively. Output phases of the DLL1 and the DLL3 are locked to the

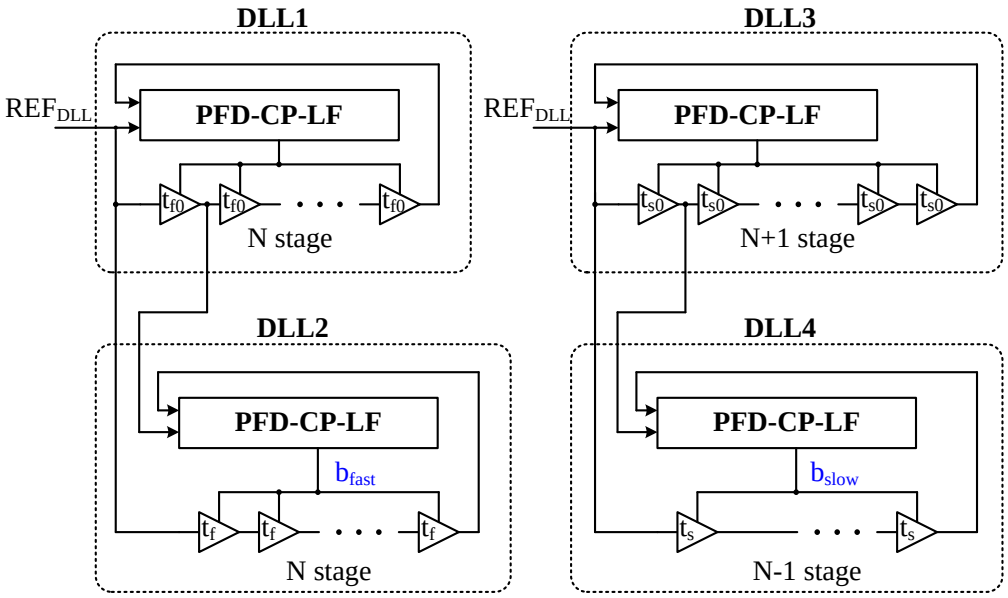
REF_{DLL}. And output phases of the DLL2 and the DLL4 are locked to the first delay cell outputs of the DLL1 and the DLL3, respectively. By this configuration, Δ_{TDC} is calculated as

$$
\begin{aligned}
&t_{f0} = T_R/N, && t_f = t_{f0}/N = T_R/N^2, \\
&t_{s0} = T_R/(N+1), && t_s = t_{s0}/(N-1) = T_R/(N^2-1), \\
&\Delta_{TDC} = t_s - t_f = \frac{T_R}{N^2(N^2-1)}
\end{aligned} \tag{4.3}
$$

, where t_{f0}, t_{s0}, t_f, t_s are delay times of delay cells in DLL1$\sim$4, respectively. If f_{REF} is 25MHz, N of 9 makes Δ_{TDC} of 6.2ps, where the total number of delay cells is 36. Therefore, the required number of delay cells for a high TDC resolution can be dramatically reduced compared with the conventional Δ_{TDC} calibrator. Power consumed by DLLs can be reduced also.



(a)



(b)

Figure 4.13: Schematics of (a) conventional dual-DLL, (b) proposed quadruple-DLL for Δ_{TDC} calibration

Figure. 4.14 (a) shows PFD and CP circuits for avoiding the DLL harmonic lock [28]. First, the delay between the voltage-controlled delay cell (VCDC) input and output is initially set to the minimum value, activating the PFD output down signal. This approach assumes that the VCDC's delay increases as the control voltage decreases. Therefore, the delay between VCDC input and output increases until it reaches one clock cycle of the input signal. Thus, the DLL will not fall into false locking and the latency is fixed to one clock cycle regardless of how long a delay the VCDC provides.

Figure. 4.14 (b) shows the timing diagram of the PFD. Initially, $\overline{RESET}$ is set at low to clear the DFF output. Therefore, $ENABLE$ is low and fulls the control voltage to VDD, setting the VCDC delay to its minimum value. In this condition, the two PFD inputs are at a low level. When $\overline{RESET}$ switches to high, $ENABLE$ also switches to high after the rising edge of IN_1. Thus, the first rising edge of IN_1 can be virtually hidden and neglected during phase comparison. Due to the nature of the negative feedback architecture, the VCDC delay increases until it is equal to one clock cycle of input signal. Since the circuit forces the VCDC delay to its minimum value and causes the VCDC delay to increase until its delay equals one clock cycle, the DLL will not fall into harmonic locking.

Figure. 4.14 (c) shows the charge pump circuit. Because the charge pump current mismatch is critical to the DLL phase offset, a replica-biasing circuit is attached to minimize it. The loop filter for DLLs is realized using a NMOS-FET capacitor to minimize the chip area occupation.

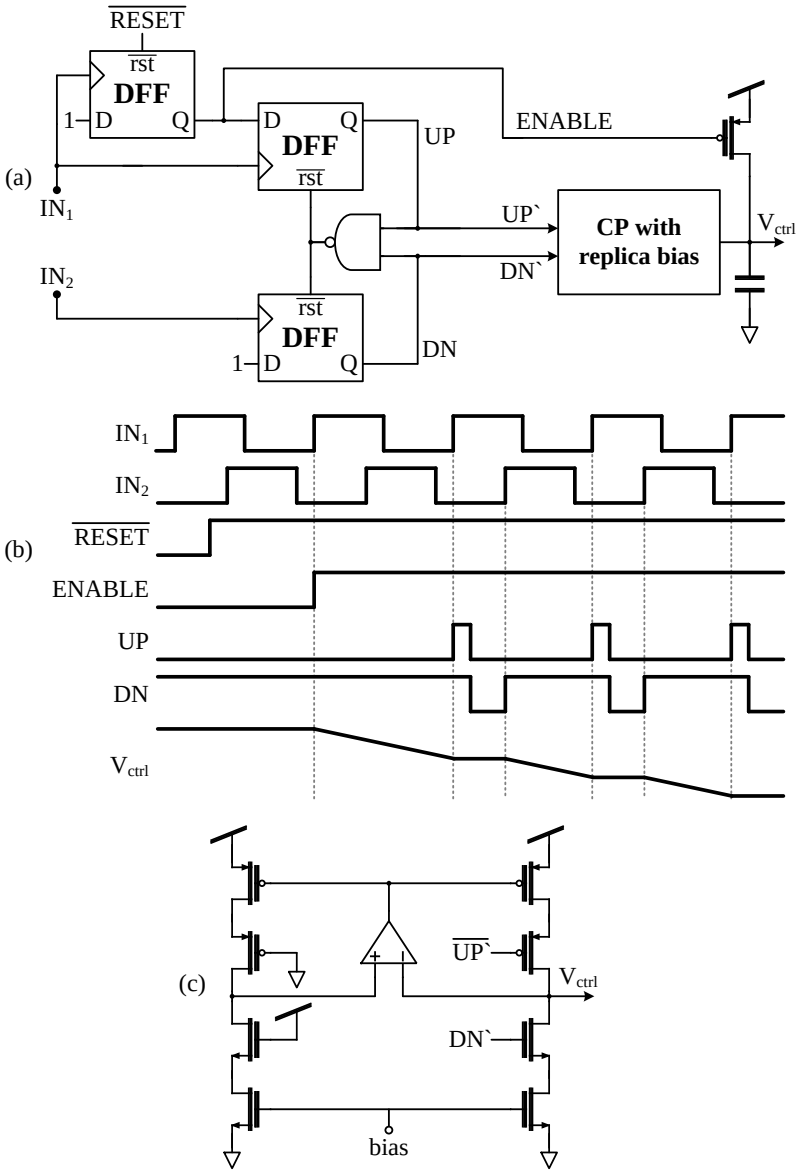


Figure 4.14: (a) Schematics of PFD and CP for DLL to avoid harmonic-lock problem, (b) timing diagram, (c) pulse reshape circuit, (d) CP circuit

Figure. 4.15 shows schematics of VCDC. Two bias voltages (b_P, b_N) are generated from the DLL control voltage (V_{ctrl}) as shown in Figure. 4.15 (a). VCDC is made up of a current-starved inverter which is controlled by b_P and b_N, and two inverters for buffering as shown in Figure. 4.15 (b). In VCDC for DLL1 and DLL3, the current-starved inverter has small size to provide a long delay time (t_{f0} or t_{s0} in Eq. 4.3). In VCDC for DLL2 and DLL4, the current-starved inverter has large size to provide a short delay time (t_f or t_s in Eq. 4.3). Inverters for buffering have the same size for all VCDCs. VCDC for DLL1 and DLL3 is designed to have a delay time range of 500ps∼15.4ns. VCDC for DLL2 and DLL4 is designed to have a delay time range of 95ps∼1.67ns. N in Eq. 4.3 is set to 9.

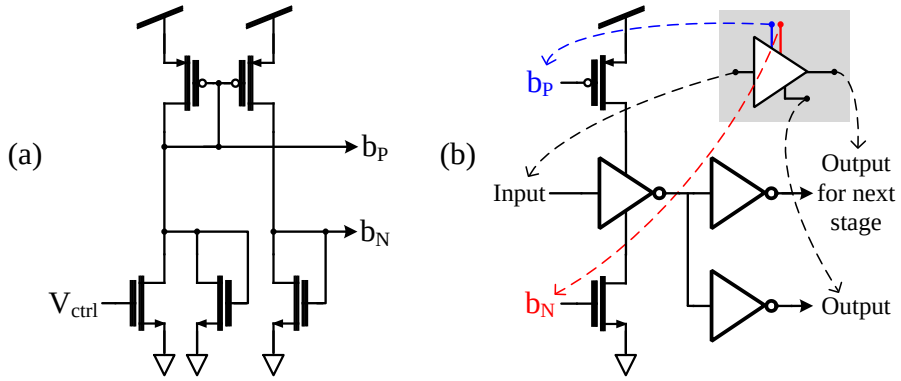


Figure 4.15: Schematics of (a) bias generator, (b) voltage-controlled delay cell

4.2.4 SPICE Simulation Results

Figure. 4.16 shows simulation results of the proposed quadruple-DLL with f_{REF} variations and process corner variations, where the black lines and the gray lines are control voltages of DLL2 and DLL4, respectively. V_{ctrl} of DLL2 is slightly higher than V_{ctrl} of DLL4 for all cases.

VDL-TDC shown in Figure. 4.14 (a) consists of the same delay cell used in DLL2 and DLL4. In the fast path (Start path), b_P and b_N from DLL2 are used. In the slow path (Stop path), b_P and b_N from DLL4 are used. Figure. 4.17 shows simulation results of VDL-TDC with f_{REF} and process corner variations. Simulated Δ_{TDC} are summarized in Table. 4.2, where the desired Δ_{TDC}s are calculated by $\frac{1/f_{REF}}{9^2(9^2-1)}$. From these, it is verified that Δ_{TDC} of VDL-TDC is always inversely proportional to f_{REF} with the error margin of only $\pm 6\%$ over a very wide f_{REF} range from 10MHz to 100MHz, regardless of process corner variations. Due to a very long simulation time, influences of temperature and supply voltage variations are not verified. However, we guess that as long as the proposed quadruple-DLL is operating normally, temperature and supply voltage variations are not critical in Δ_{TDC}, like as process corner variations.

Table 4.2: Comparison between simulated Δ_{TDC} and desired value

Process corner	f_{REF}	Simulated Δ_{TDC}	Desired Δ_{TDC}	Error
NN	10MHz	15.34ps	15.43ps	0.58%
NN	100MHz	1.453ps	1.543ps	5.83%
FF	25MHz	6.387ps	6.173ps	3.47%
NN	25MHz	6.125ps	6.173ps	0.78%
SS	25MHz	5.959ps	6.173ps	3.47%

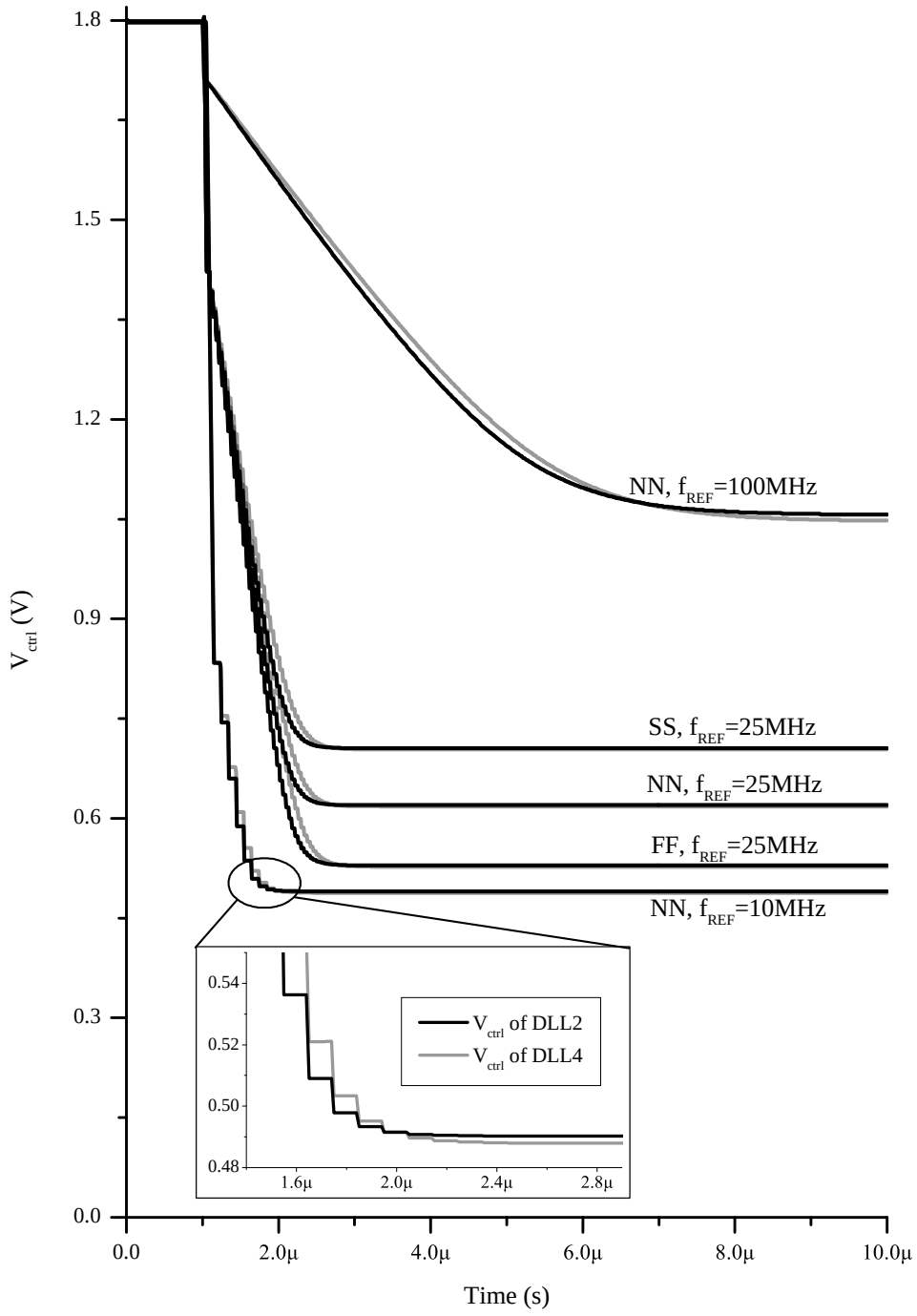


Figure 4.16: DLL simulation results with f_{REF} variations and process corner variations

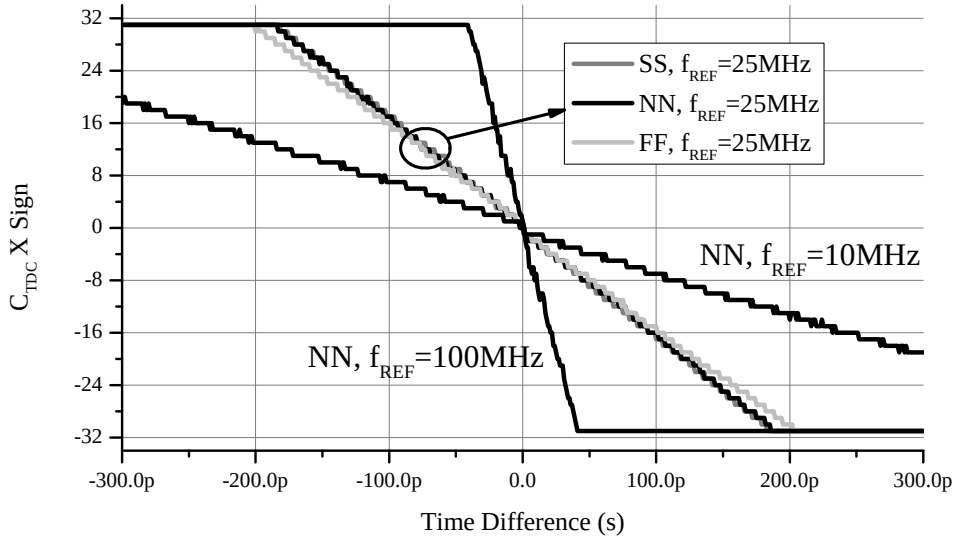


Figure 4.17: TDC curve simulation results with f_{REF} variations and process corner variations

4.3 DCO Phase Noise and Relation between K_{DCO} and C_{DCO_max}

By the proposed analog AFC, a very wide output frequency range can be easily achieved even though DCO has a few control bits and a high resolution (small C_{DCO_max} and small K_{DCO}), resulting a narrow digitally-controllable frequency range (Δ_{f_dig}). However, it is not possible to reduce Δ_{f_dig} recklessly in reality due to the intrinsic DCO phase noise. If C_{DCO} fluctuates with the DCO phase noise and reaches the DCO control code boundary (C_{DCO_max}), the digital loop is turned off temporarily. Therefore, required minimum Δ_{f_dig} is restricted by the DCO phase noise, resulting a trade-off between K_{DCO} and C_{DCO_max} because Δ_{f_dig} is equal to the product of K_{DCO} and C_{DCO_max}.

The required minimum Δ_{f_dig} is confirmed by the following procedure.

1. DCO phase noises for several DCO oscillation frequencies are simulated by a periodic steady state (PSS) analysis and a phase noise (pnoise) analysis in Spectre simulator. The results are shown in Figure. 4.18. The phase noises at 1-MHz offset are -85.34dBc/Hz and -80.01dBc/Hz when f_{DCO}s are 200MHz and 2GHz, respectively.

2. Time-domain additive white Gaussian noise (AWGN) signals corresponding to the simulated phase noises are generated.

3. Behavioral simulations are achieved including the time-domain AWGN signals, which are added to the DCO control voltage. Simulation parameters are summarized in Table. 4.3.

Figure. 4.19 shows simulation results of the DCO control code (C_{DCO}) fluctuation. When K_{dg} and K_{tr} are 0.002, C_{DCO} is almost fixed at zero as shown in Figure. 4.19 (a) due to large K_{DCO} and Δ_{TDC} (K_{DCO} and Δ_{TDC} are 400kHz/LSB and 100ps in this case, respectively). However, when K_{dg} and K_{tr} are 0.0002, C_{DCO} fluctuates in a certain range as shown in Figure. 4.19 (b) due to small K_{DCO} of 40kHz/LSB and small Δ_{TDC} of 10ps. f_{REF} variation is not critical for the maximum C_{DCO} fluctuation as shown in Figure. 4.19 (c) because the product of K_{DCO} and Δ_{TDC} is not varied (K_{DCO} and Δ_{TDC} are 400kHz/LSB and 1ps in this case, respectively), and the loop gain is not varied. However, if the dividing ratio (N_{DIV}) is decreased from 10 to 1, K_{DCO} is decreased to 40kHz/LSB, where Δ_{TDC} is not varied. As a result, the product of K_{DCO} and Δ_{TDC} is decreased, and C_{DCO} fluctuates intensely as shown in Figure. 4.19 (d) in order for maintaining the loop dynamics with the decreased loop gain. In this case, C_{DCO} fluctuates in a range from -62 to 61. Therefore, required minimum C_{DCO_max} is 62 in this case in order to prevent the digital loop from becoming off.

In these simulations, only DCO phase noises are considered. When reference spurs, charge pump noises, and TDC noises are added, C_{DCO} fluctuation will be enlarged. Therefore, enough C_{DCO_max} margin is needed when a very fine DCO resolution is required and available N_{DIV} range should be wide.

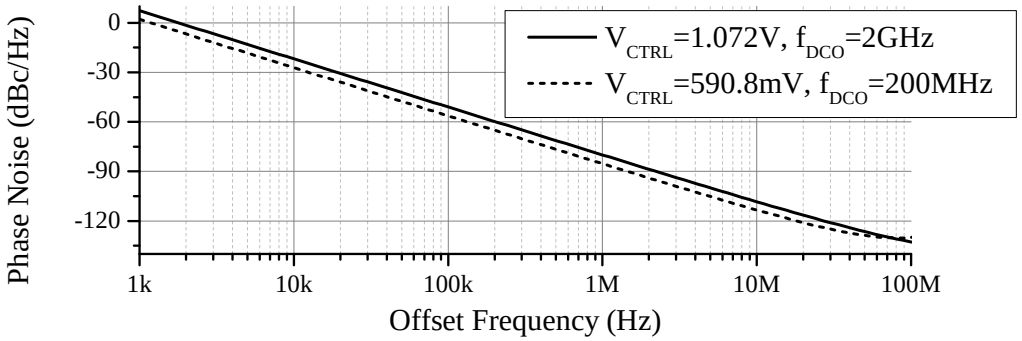


Figure 4.18: Simulated DCO phase noises

Table 4.3: Simulation parameters

f_{REF}	20,200MHz	D_{RST}	1ns
N_{DIV}	1,10	D_{Update}	2ns
K_{DCO}	0.002,0.0002Hz/LSB $\times f_{REF} N_{DIV}$	C_{TDC_max}	255
K_{VCO}	3GHz/V	C_{DCO_max}	63
f_0	0.2,2GHz	I_{leak}	0
Δ_{TDC}	0.002,0.0002s/f_{REF}	α	0.4454
I_{CPunit}	3μA	β	0.1974
$I_{CPunit2}$	10μA	C_{LF}	5μF

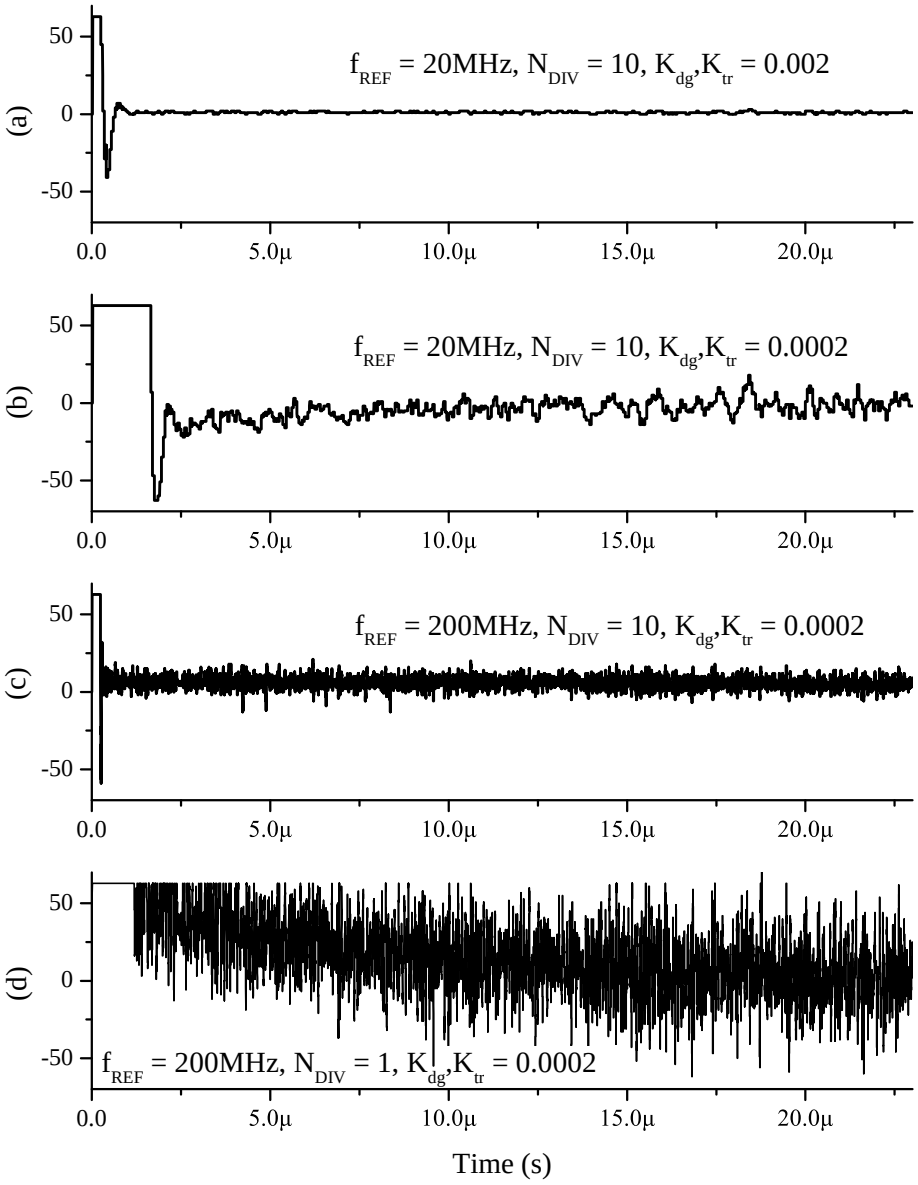


Figure 4.19: Simulated C_{DCO} fluctuations

As mentioned in chapter 3, designed DCO can provide a frequency range from 15MHz to 1.88GHz, where the DCO gain is proportional to the DCO frequency with a proportional constant K_{dg} of 0.001194. If the same performance is realized using a conventional DCO, required C_{DCO_max} can be calculated by the following equation.

$$
\begin{aligned}
&f_{DCO}(C_{DCO}) = f_{min}\mathrm{e}^{\frac{\ln(f_{max}/f_{min})}{C_{DCO\_max}} \times C_{DCO}}, \\
&K_{DCO}(C_{DCO}) = \frac{\Delta f_{DCO}}{\Delta C_{DCO}} = \frac{f_{min}\ln(f_{max}/f_{min})}{C_{DCO\_max}} \times \mathrm{e}^{\frac{\ln(f_{max}/f_{min})}{C_{DCO\_max}} \times C_{DCO}}, \\
&K_{dg} = \frac{K_{DCO}(C_{DCO})}{f_{DCO}(C_{DCO})} = \frac{\ln(f_{max}/f_{min})}{C_{DCO\_max}}, \\
&C_{DCO\_max} = \frac{\ln(f_{max}/f_{min})}{K_{dg}}
\end{aligned}
\tag{4.4}
$$

, where f_{min} and f_{max} are the minimum and maximum DCO frequencies, respectively, and C_{DCO_max} is the maximum C_{DCO}. When f_{min}, f_{max}, and K_{dg} are 15MHz, 1.88GHz, and 0.001194, respectively, calculated C_{DCO_max} is 4046.04 $\approx 2^{12}$. Therefore, the proposed DCO having 5 control bits is equivalent to the conventional DCO having 12 control bits. Moreover, if the conventional DCO is implemented using a multi-band tuning with a digital AFC, it should be considered that the monotonicity may be broken at band boundaries. Therefore, more bits are required to cover the frequency range without frequency gaps in the conventional DCO.

In the prototype chip, DCO is designed conservatively to have an excessively large K_{DCO}, where K_{dg} is 0.001194. However, in accordance with the DCO phase noise simulation mentioned in the previous section, low K_{dg} of about 0.0002 is acceptable if the minimum N_{DIV} is not too much low. With the K_{dg} of 0.0002, required C_{DCO_max} for a conventional DCO is 24155, which means that the number of control bits should be larger than 15. Therefore, with some modifications of K_{dg}, the proposed DCO can be

equivalent to the conventional DCO having 16 control bits.

Chapter 5

Conclusion

In this dissertation, a wide-range ADPLL with a novel analog/digital dual-loop architecture for SoC applications is proposed. In the main digital loop, DCO has a high resolution for the PLL jitter performance, but has a very narrow range for simple implementation. Insufficient DCO frequency range is greatly improved with assistance from an analog AFC having very low loop bandwidth. In addition, the method for making the PLL always have optimum loop dynamics is proposed.

Compared with conventional CPPLLs, the proposed PLL has the following advantages:

1. The PLL can have the best jitter performance regardless of PVT variations, the dividing ratio variation, and the reference frequency variation.

2. Several analogue problems such as a leakage current, CP current mismatches, and CP timing mismatches are intrinsically prevented.

Compared with conventional wide-range ADPLLs, the proposed PLL has the following advantages:

1. DCO and TDC can be implemented very simply, and occupies small chip area even though the PLL can provide a very wide output frequency range.

2. Phase-locking is never broken even though temperature and voltage conditions are changed as time goes on.

3. The PLL can be tolerant to the time-variant PVT conditions, dividing ratio and the reference frequency. Even though the reference frequency and the dividing ratio are unknown, the PLL can be always stable and always have optimum loop dynamics.

4. The PLL jitter performance degradation due to external supply noises can be suppressed.

The proposed PLL has a disadvantage in that its frequency acquisition time is long because the analog AFC has a very low loop bandwidth. However, if the application does not require a tight locking-time specification, the proposed architecture can be useful as a PLL IP core due to the advantages summarized above.

Appendix

A. Verilog-AMS codes for behavioral simulation

```
/* Reference clock */
module      va_REF(Clk_REF);
electrical  Clk_REF;
parameter   real Fref=1e9; // Fref: reference frequency
analog begin
        V(Clk_REF) <+ 0.5 + 0.5*sin(2*‘M_PI*Fref*$realtime);
end
endmodule


/* Frequency Divider */
module      va_FD(Clk_OUT, Clk_DIV);
electrical  Clk_OUT, Clk_DIV;
parameter   integer Ndiv=2; // Ndiv: frequency dividing ratio
integer     rCounter;
real        rClk_OUT;
analog begin
        @(initial_step) begin
                rCounter = 0; rClk_OUT = 0;
        end
        @(cross(V(Clk_OUT)-0.5, +1)) begin
                rCounter = rCounter + 1;
                if (rCounter == Ndiv/2) rClk_OUT = 1;
                if (rCounter == Ndiv) begin
                        rCounter = 0; rClk_OUT = 0;
                end
        end
        if (Ndiv > 1) V(Clk_DIV) <+ rClk_OUT; else V(Clk_DIV) <+ V(Clk_OUT);
end
endmodule
```

```
/* Phase-Frequency Detector */
module      va_PFD(Clk_REF, Clk_DIV, Up, Down);
electrical  Clk_REF, Clk_DIV, Up, Down;
parameter   real Drst = 1e-9; // Drst: PFD reset delay
real        rUp, rDown;
analog begin
        @(initial_step) begin
                rUp = 0; rDown = 0;
        end
        @(cross(V(Clk_REF)-0.5, +1)) begin
                rUp = 1;
        end
        @(cross(V(Clk_DIV)-0.5, +1)) begin
                rDown = 1;
        end
        @(cross( (delay(rUp, Drst, 1) & delay(rDown, Drst, 1))-0.5, +1)) begin
                rUp = 0; rDown = 0;
        end
        V(Up) <+ rUp; V(Down) <+ rDown;
end
endmodule


/* Loop Filter */
module      va_LF(V_CTRL);
electrical  V_CTRL;
parameter   real Clf=1; // Clf: LF coefficient
analog begin
        V(V_CTRL) <+ laplace_nd(I(V_CTRL), {1}, {0, Clf});
end
endmodule


/* Multi-Level Charge Pump */
module      va_MLCP(Sign, C_TDC, V_CTRL);
electrical  Sign, C_TDC, V_CTRL;
parameter   real Icpunit=10e-6, Ileak=0.1e-6; // Icpunit: current per LSB, Ileak: leakage
real        rQ_up, rQ_down;
analog begin
        if (V(Sign)>0.5) begin
                rQ_up = Icpunit*V(C_TDC); rQ_down = 0;
        end
        else begin
                rQ_up = 0; rQ_down = Icpunit*V(C_TDC);
        end
```

```
        I(V_CTRL) <+ -(rQ_up - rQ_down) + Ileak;
end
endmodule


/* Digitally-Controlled Oscillator */
module          va_DCO(V_CTRL, C_DCO, Clk_OUT);
electrical      V_CTRL, C_DCO, Clk_OUT;
parameter       real Kvco = 1e9, Kdco = 1e3, F0 = 0.5e9;
                // Kvco, Kdco: DCO gain for V_CTRL, C_DCO, F0: center frequency
real            rFreqIdt = 0.5e9;
analog begin
        rFreqIdt = Kdco*V(C_DCO) + Kvco*(V(V_CTRL)-0.5);
        V(Clk_OUT) <+ 0.5+0.5*sin(2*`M_PI*(F0*$realtime + idt(rFreqIdt,0)));
        $bound_step(0.01/F0);
end
endmodule


/* Time-to-Digital Converter */
module          va_TDC(Up, Down, Sign, C_TDC, Update);
electrical      Up, Down, Sign, C_TDC, Update;
parameter       integer Ctdc_max = 31; // Ctdc_max: maximum output value
parameter       real Dtdc=10e-12, Dupdate=1e-9; // Dtdc: TDC resolution, Dupdate: update delay
integer         rOut_int, rSign, rC_TDC;
real            rTime_up, rTime_down, rUpdate;
analog begin
        @(initial_step) begin
                rOut_int = 0; rTime_up = 0; rTime_down = 0; rSign = 0; rC_TDC = 0; rUpdate = 0;
        end
        @(cross(V(Up)-0.5, +1)) begin
                rTime_up = $realtime;
        end
        @(cross(V(Down)-0.5, +1)) begin
                rTime_down = $realtime;
        end
        @(cross(V(Down)-0.5, -1)) begin
                rOut_int = (rTime_down - rTime_up) / Dtdc;
        end
        rUpdate = delay(V(Up),Dupdate,1) & delay(V(Down),Dupdate,1);
        @(cross(rUpdate-0.5, +1)) begin
                if (rOut_int < 0) rSign = 0; else rSign = 1;
                if (abs(rOut_int) > Ctdc_max) rC_TDC = Ctdc_max; else rC_TDC = abs(rOut_int);
        end
        V(Update) <+ (1-rUpdate); V(Sign) <+ rSign; V(C_TDC) <+ rC_TDC;
```

```
end
endmodule


/* Digital Loop filter */
module          va_DLF(Clk, Sign, C_TDC, C_DCO);
electrical      Clk, Sign, C_TDC, C_DCO;
parameter       integer Cdco_max = 31; // Cdco_max: maximum output value
parameter       real Alpha=1, Beta=1; // Alpha, Beta: DLF filter coefficients
real            rInput, rIntg;
integer         rOutput;
analog begin
        if (V(Sign) > 0.5) rInput = V(C_TDC); else rInput = -V(C_TDC);
        @(initial_step) begin
                rInput = 0; rIntg = 0;
        end
        @(cross(V(Clk)-0.5,+1)) begin
                rIntg = Beta*rInput + rIntg;
                if (rIntg > Cdco_max*2) rIntg = Cdco_max;
                if (rIntg < -Cdco_max*2) rIntg = -Cdco_max;
        end
        rOutput = rIntg + Alpha*rInput;
        if (rOutput > Cdco_max) rOutput = Cdco_max;
        if (rOutput < -Cdco_max) rOutput = -Cdco_max;
        V(C_DCO) <+ rOutput;
end
endmodule


/* Multi-Level Charge Pump 2 */
module          va_MLCP2(C_DCO, V_CTRL);
electrical      C_DCO, V_CTRL;
parameter       real Icpunit2 = 10e-6; // Icpunit2: current per LSB
analog begin
        I(V_CTRL) <+ -Icpunit2*V(C_DCO);
end
endmodule
```

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국 문 요 약

넓은 주파수 범위에서 최적의 루프 다이나믹스 특성을 가지는 아날로그/디지털 혼합 위상 고정 루프 회로

위상 고정 루프(PLL) 회로는 통신, 제어, 계측, 센서, 시스템-온-칩 등 여러 분야에 폭넓게 사용되는 회로로, 기존에는 주로 차지-펌프 기반의 아날로그 회로를 이용해서 설계해 왔다. 최근에는 반도체 공정이 발달하고 디지털 회로 설계에 특화되면서, 여러 응용 분야에서 올-디지털 위상 고정 루프(ADPLL) 회로가 기존 아날로그 PLL 회로를 대체하고 있다. 하지만, 기존 ADPLL 회로들은 몇 가지 한계점을 가지고 있다. 첫 번째로, 복잡한 디지털-아날로그 변환기(DAC)를 사용하지 않는 디지털-제어 발진기(DCO)로는 넓은 주파수 범위를 구현하기 어렵다. 두 번째로, 일반적으로 넓은 주파수 범위를 가지는 DCO를 구현할 때에, 좁은 주파수 미세조정 구간에서만 단조 증가성을 보장하고, 대략적인 주파수는 자동 주파수 교정기(AFC)를 이용하여 주파수 대역을 목표치에 맞추는 다대역 조정 방법을 사용하는데, 이 방법은 미세조정 루프가 해당 대역의 범위를 벗어날 때에 위상 고정이 유지되지 않을 수 있는 위험성을 가지고 있다. 세 번째로, DCO의 특성이 공정, 전원전압, 온도(PVT)에 민감하게 바뀌기 때문에, PLL의 다이나믹스가 PVT로부터 자유롭기가 어렵다.

본 논문에서는 새로운 구조의 아날로그/디지털 이중 루프 방식의 PLL 회로를 제안하였다. 주가 되는 디지털 루프에서는 DCO가 PLL의 지터 성능을 위해 높은 해상도를 가지면서, 간단한 구현을 위해 매우 좁은 주파수 범위를 가진다. 모자란

DCO 주파수 범위는 간단한 아날로그 AFC 회로를 이용해서 크게 넓힌다. 결과적으로, 복잡한 DAC 회로의 사용 없이 매우 넓은 주파수 범위를 구현할 수 있다. 또한, 제안한 DCO는 그 주파수 이득이 DCO의 출력 주파수에 비례한 특성을 가지는데, 이로 인해 PLL의 다이나믹스가 PLL의 주파수 분주 계수에 적응성을 가질 수 있다. 제안한 구조는 180nm CMOS 공정을 이용해서 시제품 칩을 제작하였다. 제작된 DCO는 5비트의 제어 신호를 가지지만, 15MHz부터 1.88GHz까지 매우 넓은 주파수 범위에서 동작함을 검증하였다. 이는 기존의 12비트 DCO와 동등한 성능을 갖는다. 제작된 PLL 또한 루프 안정성을 위한 보상 회로 없이도 50MHz부터 1.6GHz까지의 넓은 범위에서 동작함을 검증하였다.

하지만 유감스럽게도 제작된 PLL 칩은 DCO의 주파수 표류로 인해 주가 되는 디지털 루프가 의도치 않게 꺼져 버리는 비정상적인 현상을 보였다. 이 문제를 해결하는 방법을 본 논문의 후반부에서 제안하였고, 이를 시뮬레이션을 통해 검증하였다. 더 나아가서, PLL이 PVT 변화와 기준 주파수 변화에도 적응성을 가질 수 있도록 개선하는 방법을 제시하였다. 이를 위해서 시간-디지털 변환기(TDC)의 해상도를 보상하는 간단한 보상기 회로를 제안하였다. 결과적으로, 개선된 PLL은 PVT, 주파수 분주 계수, 기준 주파수에 둔감하면서, 불안정성의 위험 없이 항상 최적의 루프 다이나믹스를 가질 수 있다.

핵심되는 말: 위상 고정 루프, 올-디지털 위상 고정 루프, 자동 주파수 교정기, 넓은 출력 주파수 범위, 루프 다이나믹스 최적화