Adaptive Equalization Based on Asynchronously Under-Sampled Histograms

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Adaptive Equalization Based on Asynchronously Under-Sampled Histograms

by

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Abstract

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Compensating the inter-symbol interference (ISI) caused by frequency dependent loss of the band-limited channel is a major challenge for realizing high-speed wire-line link. Various equalization techniques are used in order to remove ISI. Successful equalization requires precisely described channel characteristics, which is usually unavailable in many high-speed serial interface applications due to process, voltage and temperature (PVT) variations. Consequently,

adaptive equalization that compensates various channel environments is highly desirable in various high-speed interface systems.

A new type of adaptive continuous-time linear equalizer (CTLE) based on asynchronously under-sampled histograms is investigated and fabricated with standard complementary metal-oxide-semiconductor (CMOS) technology. Our CTLE automatically selects the optimal equalization coefficient among several predetermined values by searching for the coefficient that produces the largest peak value in histograms obtained with asynchronous under-sampling. This scheme is simple and robust monitoring without any clock recovery or synchronization architectures.

A prototype chip realized in 0.13-μm CMOS technology successfully achieves equalization for 5.4-Gbit/s $2^{31} - 1$ pseudorandom bit sequence (PRBS) data through 40-, 80-, and 120-cm PCB traces and 3-m DisplayPort cable. The peak-to-peak jitters are 33.62, 34.81, 36.41, and 34.73 ps, respectively. The chip core occupies 0.18-mm^2 die area and consumes 35 mW from 1.2-V power supply. In addition, we present the results of statistical analysis with which we verify the reliability of our scheme for various sample sizes. The measurement results of this analysis are confirmed with experimental data.

We extended our asynchronously under-sampled histograms to

various applications due to its simplicity and data rate independent flexibility. Firstly, a low-power adaptive equalizer realized in 65-nm CMOS technology consumes 4.66 mW during adaptation and 2.49 mW after adaptation. For 10-Gbit/s $2^{31} - 1$ PRBS data transmitted over 40-cm FR4 PCB trace, our equalizer achieves error-free during 15 minutes and 26.6 ps peak-to-peak jitter. And then, a single-ended adaptive equalizer and duty-cycle corrector realized by 0.13-μm CMOS technology can compensate 10.9-dB channel loss at 2.5 GHz and 25~75 % duty-cycle distortion. For 5-Gbit/s data transmitted over 80-cm FR4 PCB trace, our circuit achieves error-free during 30 minutes and 53.2 ps peak-to-peak jitter. Finally, a PVT tolerant fast adaptive CTLE realized in 0.13-μm CMOS technology demonstrates 10-Gbit/s data transmission through 40-cm PCB trace. It shows stable operation for 1.0-V to 1.5-V supply voltage variations with error-free during 15 minutes and 18.9 ps peak-to-peak jitter.

Keywords: adaptive equalizer, asynchronously under-sampled histograms, bit-error rate (BER), continuous-time linear equalizer (CTLE), duty-cycle corrector, low-power, single-ended signaling

1. Introduction

1-1. Equalization Systems

As the information and communication technology rapidly developed, many wire-line applications require faster data rate. Fig. 1-1 shows the increasing speed requirement for I/O interconnect standards which reach the data rate over several Gbit/s. However, as the data rate requirements continuously increased, inter-symbol interference (ISI) becomes a serious problem in high-speed serial interfaces.

ISI caused by reflection of the connector, skin effect and dielectric loss of the channel degrades the timing jitter and the frequency bandwidth of received signal and worsen the bit-error rate (BER) [1]. In order to compensate the limited channel bandwidth, various types of equalizers are widely used. Fig. 1-2 shows various equalizations at high-speed serial interface in order to flatten the frequency response out to the Nyquist frequency and remove time-domain ISI.

Pre-emphasis in the transmitter achieves equalization by boosting up high-frequency components or reducing low-frequency of transmitted data [2]–[4]. Pre-emphasis is relatively easy to implement and it cancels ISI in pre-cursor and post-cursor without noise amplification.

However, Pre-emphasis limits voltage swing due to peak power constraint. Moreover, Pre-emphasis requires additional feedback channel from the receiver to the transmitter for pre-emphasis control.

Decision feedback equalizer (DFE) in the receiver operates with the incoming signal directly subtracting ISI based on the decided data [5]-[7]. Since the decision data is stuck on one of two voltage levels (high or low level), incident noise is removed, DFE can boost high frequency content without noise amplification. However, DFE cannot cancel the pre-cursor ISI and it has chance for error propagation. In addition, DFE requires the stringent timing constraint due to feedback path delay as well as clock recovery and distribution circuits in terms of implementation scheme.

Continuous-time leaner equalizer (CTLE) which is amplifier with source degeneration, inductive peaking or negative capacitance technique can provide frequency peaking with gain at Nyquist frequency [8]-[11]. CTLE has simple structure and good linearity. Moreover, CTLE does not require synchronous clock signals for equalizing operation. However, CTLE is sensitive to process-voltage-temperature (PVT) variation.

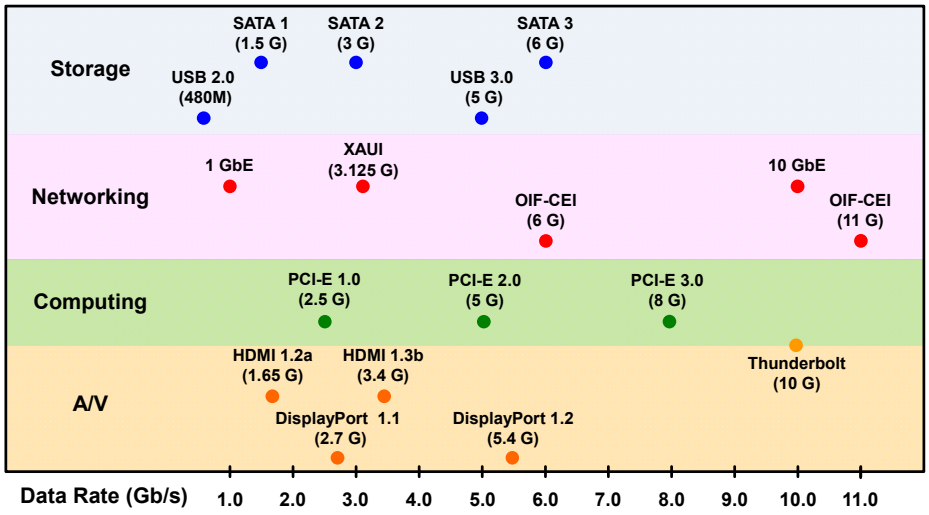

Fig. 1-1. Increasing speed requirement for I/O interconnect standards.

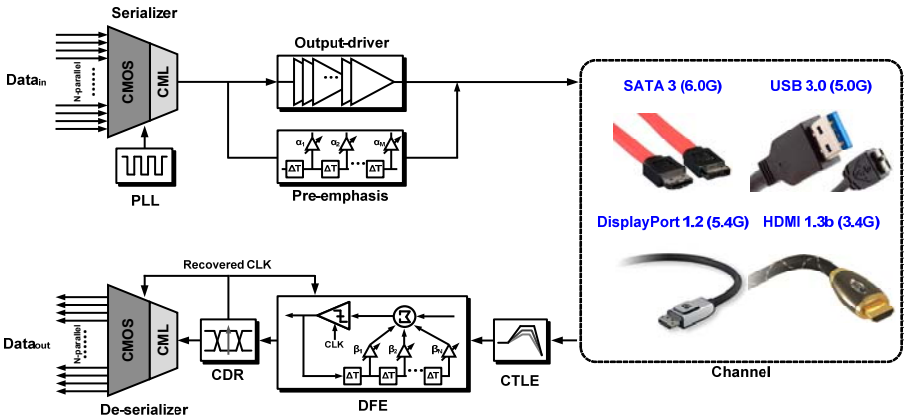

Fig. 1-2. Various equalizations for high-speed serial interface.

1-2. Adaptive Equalization

Many applications require equalizers having adaptation ability that can provide optimal equalization for different channel conditions. Various adaptive equalizers have been reported. In the spectrum balancing method as show in Fig. 1-3, adaptive equalization is achieved by comparing high- and low-frequency components of data power and generating feedback signals until the power spectrum is balanced [12], [13]. Although equalizer adaptation in this method can be realized independent of timing recovery, its implementation requires complicated analog circuits whose performance can be affected by process variations. Digital signal processing (DSP) using the least mean square (LMS) or the zero forcing (ZF) algorithms can be also used for adaptive equalization as shown in Fig. 1-4 [14], [15]. This provides flexibility and easy programmability, but speed limitation and complexity of the required analog-to-digital converter (ADC) limit applicability of this scheme for high-speed applications.

One promising adaptive equalization technique is using an eye opening monitor (EOM) as show in Fig. 1-5 [16]–[18]. The EOM evaluates data quality with periodic observations of the filter output and provides information about the equalizing filter performance. Using

this information, the equalizer can determine the optimal filter conditions. In addition, EOM can give an intuition to debuggers on operating status of the chips. Therefore, EOM more reduce the testing time and cost than to measure bit-error rate (BER). For these methods, synchronous sampling clock circuits and high-speed comparators are essential. Moreover, it can be difficult to recover clock signals from the initially closed eye diagram, limiting its applicability.

We present novel adaptive equalization method using asynchronously under-sampled histogram in next chapter. This can avoid the need for clock recovery system, increasing the flexibility by allowing the potential application of the same monitor to signals with arbitrary data-rates. In addition, low-speed under-sampling clock can be used for reducing the cost of the monitoring system.

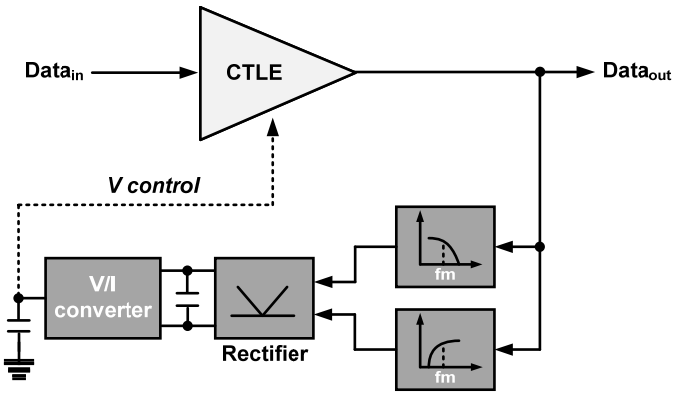

Fig. 1-3. Spectrum balancing adaptive equalization.

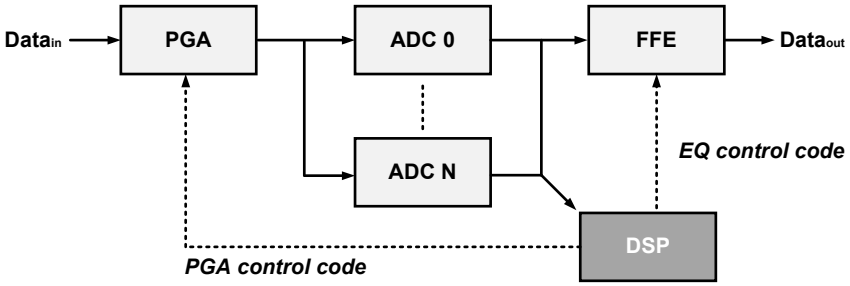

Fig. 1-4. DSP based adaptive equalization.

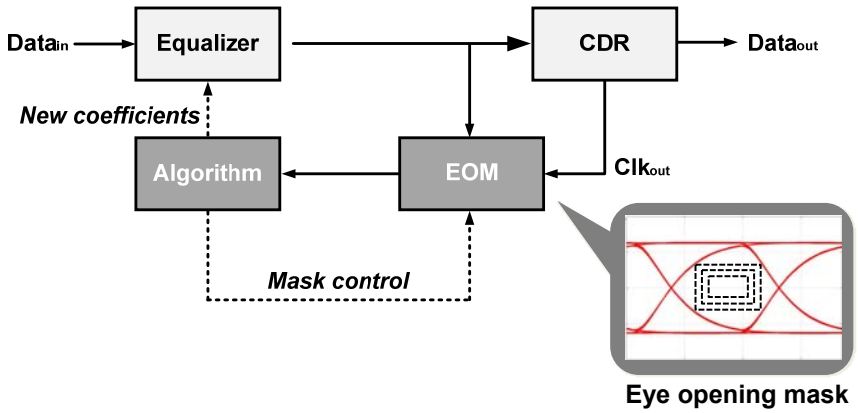

Fig. 1-5. On-chip EOM adaptive equalization.

1-3. Outline of Dissertation

The rest of this dissertation is organized as follows.

Chapter 2 presents adaptive algorithm based on asynchronously under-sampled histogram. This chapter explains the behavior simulation, impulse response analysis, asynchronous under-sampling clock, and histogram sample size for adaptive algorithm realization.

Chapter 3 describes a circuit implementation of proposed adaptive equalizer. This chapter explains channel modeling, equalizing filter design, histogram extraction circuit design, and digital controller operation.

Chapter 4 shows measurement results of a 5.4-Gbit/s adaptive equalizer fabricated with standard 0.13-μm CMOS technology. The measurement focuses on the proof of the concept design for asynchronously under-sampled histogram.

Chapter 5 proposes our adaptive algorithm to extend to various applications. A 10-Gbit/s low-power equalizer for 40-cm PCB trace is demonstrated. Next, a 5-Gbit/s single-ended adaptive equalizer and duty-cycle corrector for 80-cm PCB trace is demonstrated. Finally, a 10-Gbit/s PVT tolerant fast adaptive equalizer for 1.0-V to 1.5-V supply voltages is demonstrated.

Finally, this dissertation will be summarized in chapter 6.

2. Asynchronously Under-Sampled Histogram

2-1. Behavioral Simulation

We proposed a new type of adaptive CTLE based on asynchronous under-sampling histograms [20]. Our adaptation scheme is based on the simple observation that the clearest eye diagram produces the largest peak value in the histogram obtained with asynchronous under-sampling. Fig. 2-1 shows sequences of random binary data with different amounts of equalization. When these are sampled with a clock which is asynchronous and slower than the data clock, different types of histograms are produced.

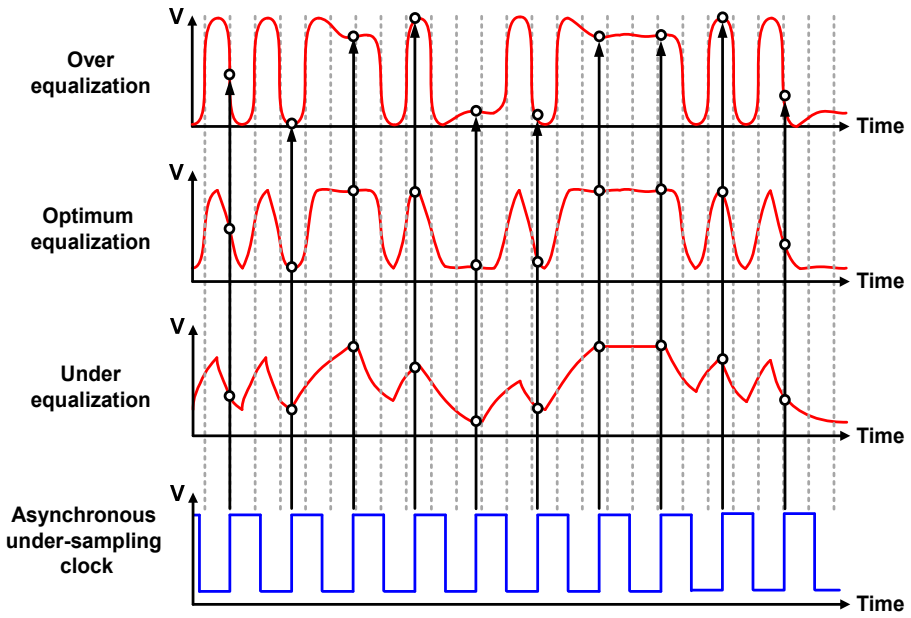

Fig. 2-1. Asynchronous under-sampling process.

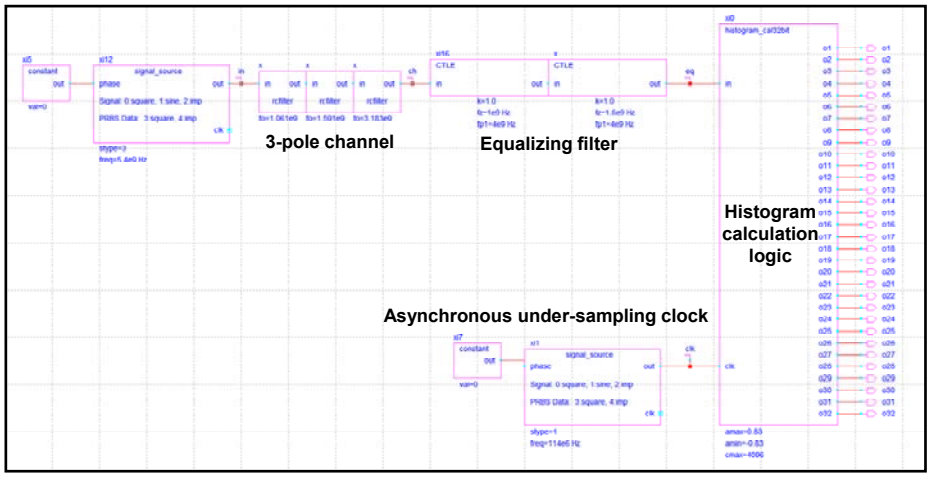

Fig. 2-2. Behavioral model of the asynchronously under-sampled histogram.

To verify the operation of the proposed adaptation scheme, the behavioral simulation is performed using the Cppsim system simulator. Fig. 2-2 shows the behavioral model of the asynchronously under-sampled histogram. The channel used for simulation is 3-m DisplayPort cable modeled with a three-pole low-pass filter whose characteristics are experimentally determined by S-parameter measurement of an actual cable. The poles are located at 1.061, 1.591, and 3.183 GHz. The equalizer used for simulation has a two-stage active filter in which high-frequency boosting is controlled by two zeros [19]. In the simulation, 5.4-Gbit/s $2^7 - 1$ pseudorandom bit sequence (PRBS) data are transmitted through the channel, and the eye diagrams resulting from three different filters having different amounts of high-frequency boosting are shown in Fig. 2-1. The resulting data are then asynchronously sampled with 114-MHz clock and compared with 32-amplitude levels for obtaining histograms. The sample size for each histogram is 4096.

The simulation results show the three cases of eye diagrams and histograms. For the case of over-equalization, the equalizer output has enhanced high-frequency components, which tend to broaden the data amplitude distribution around peak values as shown in Fig. 2-3(a). For the case of under-equalization, the distribution in the histogram is

spread out as shown in Fig. 2-3(c). With optimal equalization, the distribution is concentrated at peak values as shown in Fig. 2-3(b). Based on these observations, we can easily determine the equalizer condition that results in the best eye quality by simply searching for the histogram that has the largest peak value.

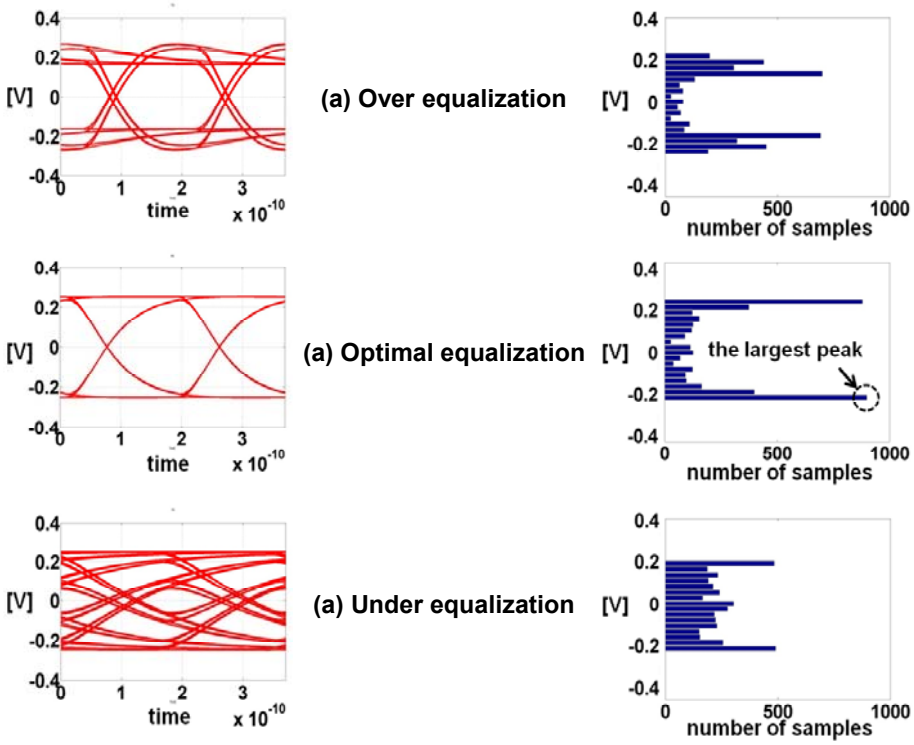

Fig. 2-3. Examples of eye diagrams and histograms: (a) Over equalization (b) Optimal equalization (c) Under equalization.

2-2. Impulse Response Analysis

A linear time-invariant (LTI) system can be completely characterized by its impulse response as shown in Fig. 2-4. Thus, for any input, the output function can be calculated in terms of the input and the impulse response.

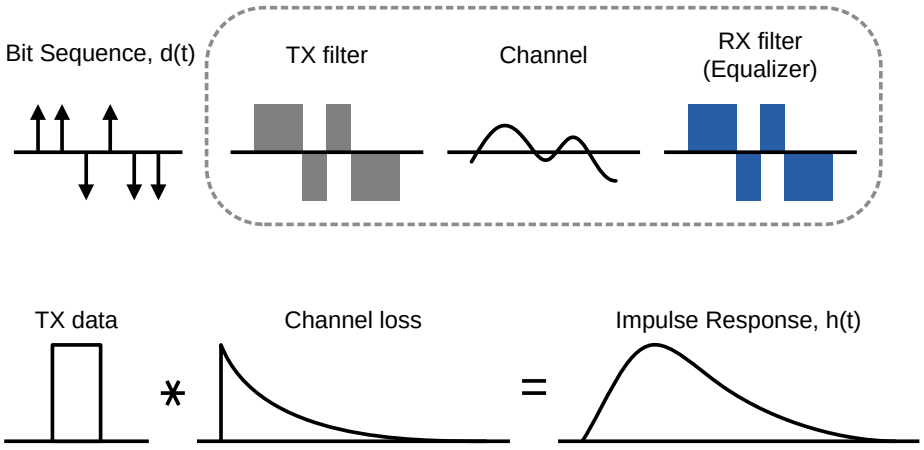

Fig. 2-4. Unit impulse response from channel characteristics.

In order to quantify the ISI of the channel, we investigate the characteristic of channel output signal. It is a function of periodic sampling convolution and represented as follow.

$$y(t) = h(t) * d(t) = h(t) * \delta(t - iT)d_i = \sum_{i=-\infty}^{\infty} h(t - iT)d_i \qquad (2.1)$$

where the $h(t)$ is channel impulse response, the $d(t)$ is data stream with delta function and T is the minimum data period. If the channel impulse response is limited to a pre-cursors and b post-cursors, channel output is as follow.

$$y(t) = \sum_{i=-a}^{b} h(t - iT)d_i = \sum_{i=-a}^{b} h_{-i}(t)d_i \qquad (2.2)$$

where the $h_{-i}(t)$ is the weight of cursor which effects the data amplitude. For random data stream, number of cases of the amplitude of channel output response can be determined as $2^{(a+b+1)}$. Accordingly, the amplitude of probability is $0.5^{(a+b+1)}$ due to the probability of each data stream and the combinations of the $y(t)$ are 0.5 and $a+b+1$, respectively. If the channel impulse response has from 1 to 3 cursors, the number of output response can be calculated 2 to 8, and data probability in the signal distribution can be $1/2$ to $1/8$ as shown in Fig 2-5.

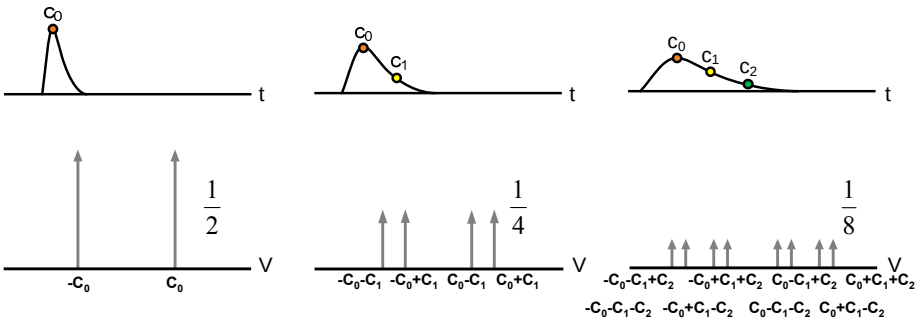

Fig. 2-5. Example of impulse responses and corresponding data probabilities in y(t) distribution.

As the length of channel impulse response decreases, the peak value of signal distribution increases. In other words, an equalizing filter is optimized when the signal distribution has the maximum peak value. Consequently, our adaptation algorithm based on the asynchronously under-sampled histograms is essentially searches for the filter coefficient producing the minimum ISI.

2-3. Sampling Clock

In proposed histogram scheme, the sampling clock is asynchronous to the transmitted data rate. With this sampling clock, all sampling points are plotted in time order, and superimposed for given sample size. To obtain the correct histogram, the following conditions should be satisfied. First, the sampling clock is non-integer ratio of data rate to sampling rate. When the sampling clock has integer ratio, the sampling positions are overlapping as shown in Fig. 2-6(a). Second, a sampling covered region should be uniformly spread across the entire bit period. When the sampling covered region is not enough, the incorrect histogram is extracted as shown in Fig. 2-6(b). With keeping these conditions, we can obtain the correct histogram representing signal amplitude distribution as shown in Fig. 2-6(c).

It can be analyzed as follow [21]:

$$T_{step} = \frac{1}{f_C} - \frac{1}{(\frac{n}{m}) f_S} = \frac{1}{k \cdot f_S} \tag{2.3}$$

where f_S is data rate, f_C is sampling clock rate, T_{step} is sampling time interval, n,m are natural numbers, and k is the sample size. From these

equations, f_C is given as

$$f_C = \left(\frac{1}{k} + \frac{m}{n}\right)^{-1} f_S \tag{2.4}$$

For example, k is 4096, f_S is 5.4 Gbit/s, and the n is 1024 and m is 48505, the required f_C is 114.000030 MHz. This sampling clock can be generated by external frequency synthesizer or internal free-running oscillator for random sampling process.

Consequently, the asynchronous under-sampling allows reliable data collection as long as a sufficient number of samples are taken and the sampling clock is not a sub-harmonic of the data clock.

Such an asynchronous under-sampling technique has been used for performance monitoring in optical communications. Asynchronous under-sampling histograms according to optical impairments was presented by Hanik et al. in [22]. And Shake et al. analyzed of asynchronous under-sampling histograms by developing methods to estimate the Q-factor and corresponding BER, based on processing the asynchronous under-sampling histograms in optical domain [23]–[26].

In this dissertation, we propose a simple adaptive equalization using asynchronously under-sampled histograms with statistical analysis based on fully integrated on-chip circuit design in electrical domain.

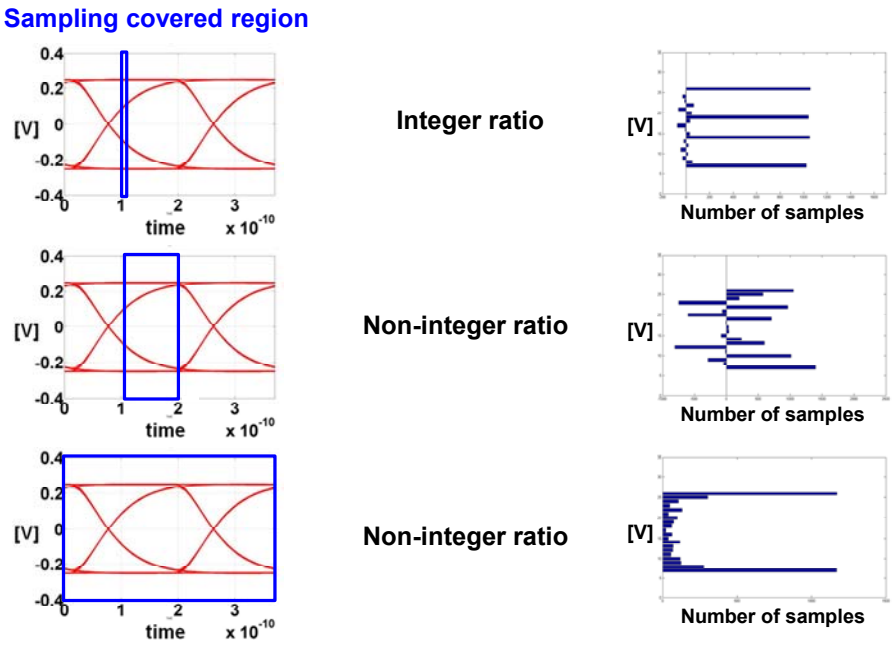

Fig. 2-6. Extracted histograms of integer ratio sampling clock, non-integer ratio sampling clock with narrow sampling covered region, and non-integer ratio sampling clock with enough sampling covered region.

2-4. Sample Size

A larger sample size guarantees better histogram reliability, but the sample size has limitation for practical implementation. In order to determine the proper sample size, we performed the following statistical analysis. For our analysis, we considered an eye diagram due to 3-bit random data sequence as shown in Fig. 2-7. Among all the possible data patterns, 111 data sequence always produces the high level when sampled, and both 011 and 110 sequences produce the high level half the time when sampled. The sampling process can be modeled with the binomial process in which the sampled data contributing to the high level are considered as success and all others are considered as failure. Consequently, when we sample a random 3-bit data sequence, the probability for sampling the high level p is $(1 + 2 \times 0.5)/8 = 1/4$. Here, 1/8 comes from 111 data sequence, and 0.5/8 comes from either 011 or 110.

The binomial process can be approximated by the normal distribution if $np > 10$ and $0.1 < p < 0.9$ [27], where n represents the sample number. With this approximation, we can use the well-known properties of the normal distribution. The required minimum sample number n with confidence interval of $(1 - \alpha)$ resulting in p bounded by

$p - e$ and $p + e$, where e represents the margin of error, is given as [28]

$$n = \frac{p(1-p)(z_{1-\alpha/2})^2}{e^2} \tag{2.5}$$

Here, $z_{1-\alpha/2}$ is the critical value in the normal distribution with probability of $\alpha/2$ in each tail as shown in Fig. 2-8. For example, for 99% confidence interval, α is 0.01, and $z_{1-\alpha/2}$ is 2.58. We found from our simulation that e = 0.0175, or 1.75% margin of error, guarantees a sufficient difference between the largest and the second largest peak values in our histograms. With 99% confidence interval and 1.75% margin of error, the minimum sample size determined by (2.5) is 4075. For real chip fabrication, 4096 samples with 12 bit register are used.

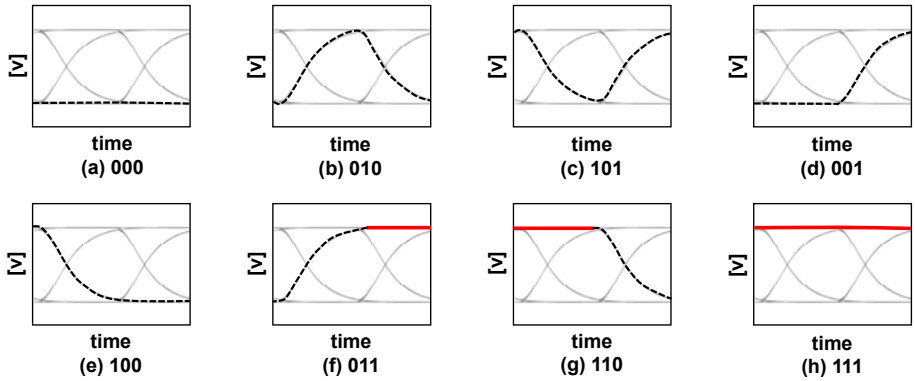

Fig. 2-7. (Straight line) Probability of success for 3-bit data pattern. (a) 000; (b) 010; (c) 101; (d) 001; (e) 100; (f) 011; (g) 110; (h) 111.

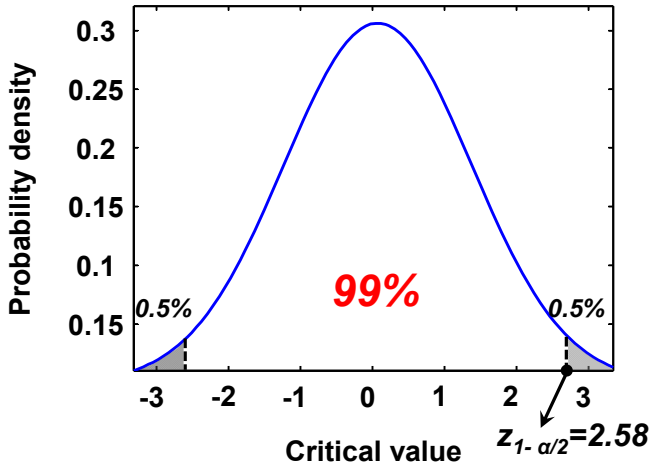

Fig. 2-8. Critical value of 99% confidence interval in the normal distribution.

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3. Adaptive Equalizer Realization

3-1. Channel Characteristics

Our design target is 5.4-Gbit/s data transmission over 40-, 80-, and 120-cm PCB traces and 3-m DisplayPort cable. As the first step, we measured the channel characteristics using a vector network analyzer for channel modeling. The accuracy of the model for the target channels is very important for system-level simulation and analysis. The most extensively used model is the S-parameter model which represents the characteristics of the insertion loss and the return loss. The channels have from about 5.9- to 15.7-dB loss at 2.7 GHz as shown in Fig. 3-1. With the S-parameter model file, the target channels can be simulated and analyzed with an n2port cell, which can load the model file, in Cadence environment. To verify the accuracy of the S-parameter model, we compare 5.4-Gbit/s measured eye diagrams and simulated eye diagrams for 4-type different channels. Fig. 3-2 shows the channel model having well-fitted tendency with measurement results.

From this, we designed our adaptive CTLE to have from −4- to 18-dB equalizing gain which compensates channel loss as well as loss due to circuit implementation.

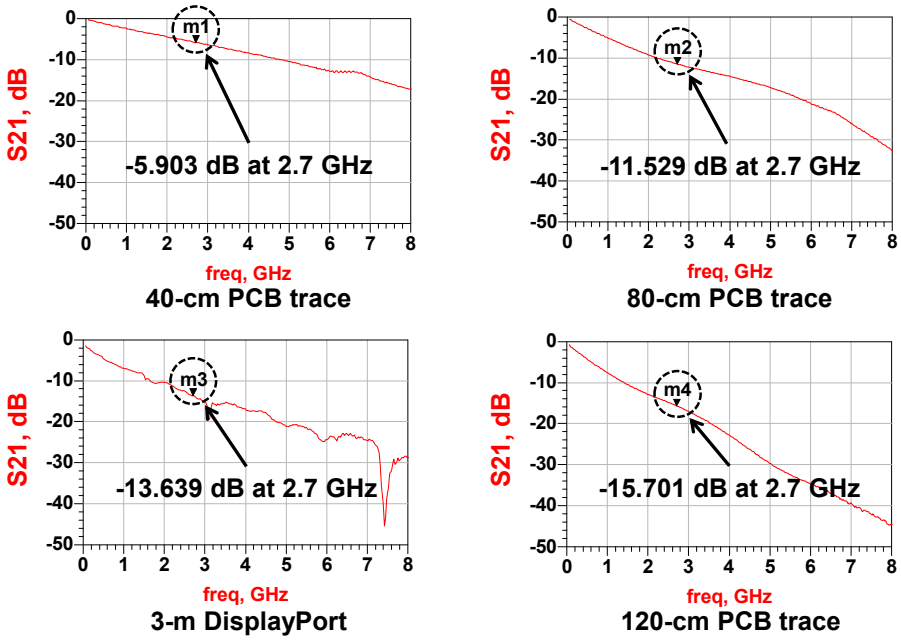
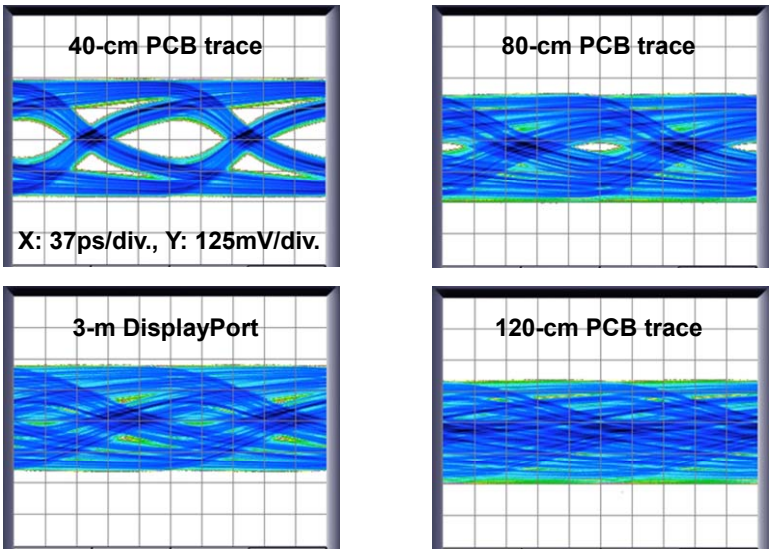
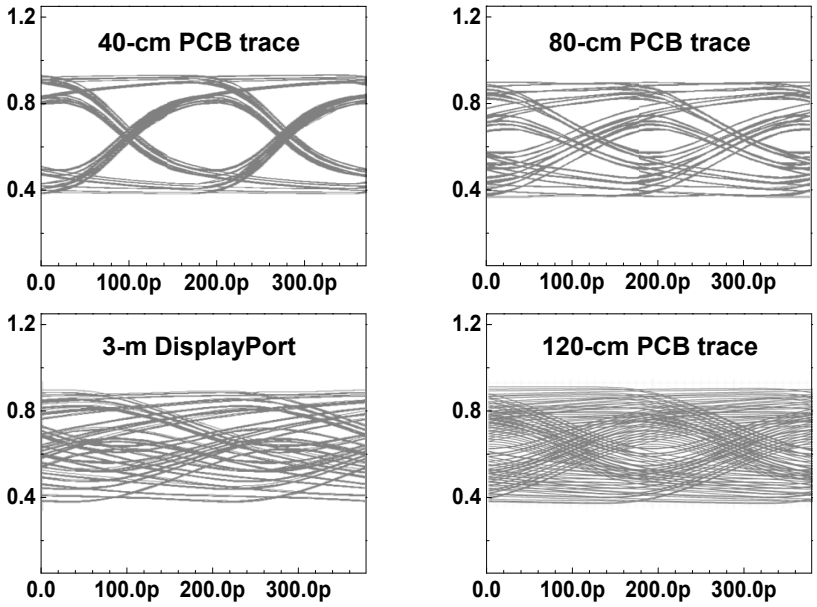


Fig. 3-1. S-parameter responses for 4-type different channels.



(a)



(b)

Fig. 3-2. Eye diagrams of (a) measurement and (b) simulation results.

3-2. Circuit Implementation

Fig. 3-3 shows the block diagram of proposed adaptive CTLE. It has an active equalizing filter with capacitive source degeneration and adaptive circuits which consist of four track-and-hold circuits, two unit gain buffers (UGBs), a comparator, two digital-to-analog converters (DACs), a 5-phase clock generator, and a digital controller. The track-and-hold circuit is transmission gate with n- and p-channel metal–oxide semiconductor (NMOS and PMOS) switches for avoiding voltage drop. The UGBs provide isolation from clock feed-through of the track-and-hold circuits.

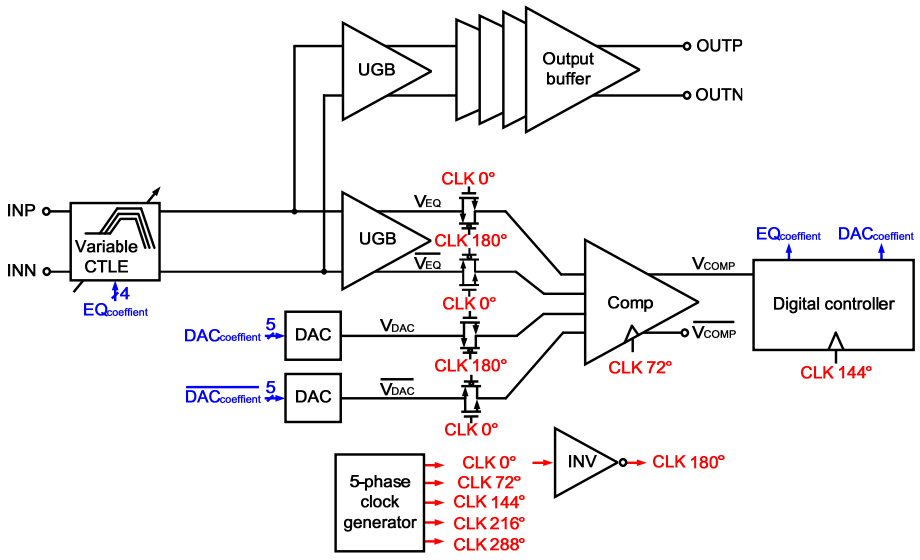


Fig. 3-3. Block diagram of proposed adaptive CTLE.

The two-stage capacitive degeneration filter, as shown in Fig. 3-4, contains a 4-bit NMOS resistor array, which provides 16 different levels of gain boosting with about 1.4-dB increment for channel-loss compensation. The desired filter range and resolution was determined from Matlab simulation of the target channels with various filter conditions. The frequency response of the equalizing filter can be estimated by pole-zero analysis. The transfer function of the filter with capacitive degeneration can be derived as:

$$H(s) \cong \left(\frac{g_m R_L}{1+\frac{g_m R_S}{2}} \cdot \frac{1+\frac{s}{\omega_z}}{\left(1+\frac{s}{\omega_{p1}}\right)\cdot\left(1+\frac{s}{\omega_{p2}}\right)} \right)^2 \qquad (3.1)$$

where $\omega_z = 1/(R_S C_S)$, $\omega_{p1} = (1+g_m R_S/2)/R_S C_S$, $\omega_{p2} = 1/(R_L C_L)$, and g_m is the transconductance of $M_{1,2}$. The transfer function has capacitive degeneration filter characteristics as shown in Fig. 3-5. The equalizing gain of the filter is $[(g_m R_L/(1+g_m R_S/2))(\omega_{p1}/\omega_z - 1)]^2$ which can be controlled by R_s from −4- to 18-dB. On-chip 50-Ω resistors are integrated for input impedance matching.

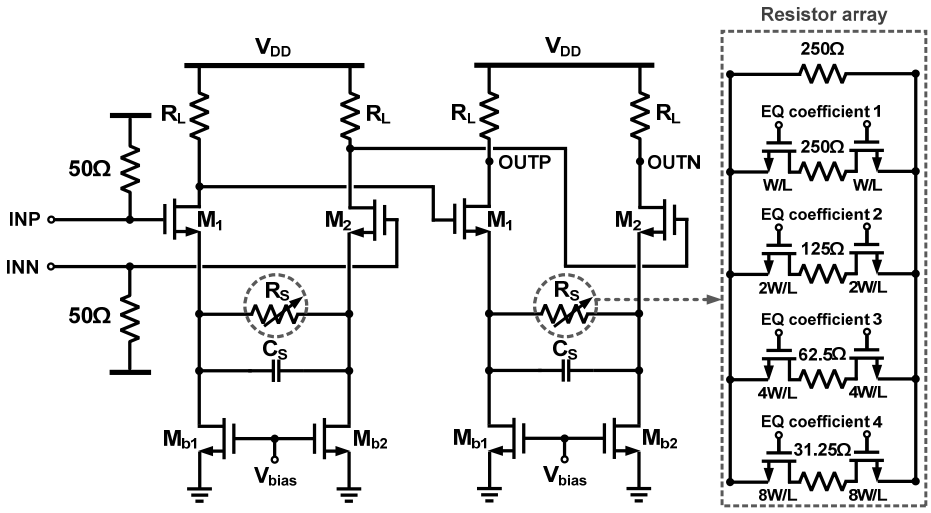


Fig. 3-4. Schematic diagrams of tunable CTLE filter.

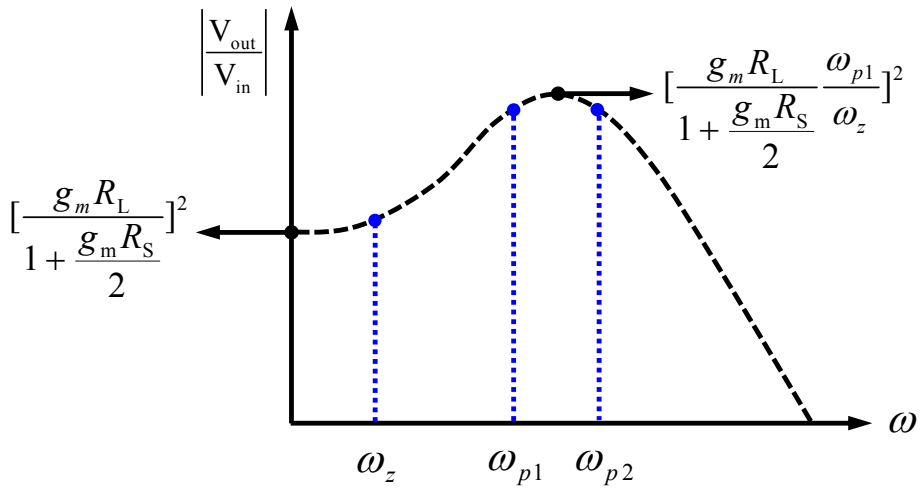
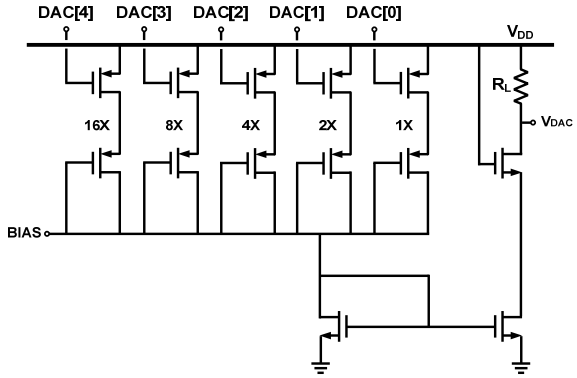


Fig. 3-5. Transfer function of CTLE with capacitive degeneration.

The 5-bit DAC as shown in Fig. 3-6(a) generates 32-level reference voltages. The reference level is controlled from 600 mV to 1.2 V by PMOS load switches with 5-bit DAC coefficients. The DAC resolution is 19.35 mV, which provides the desired filter coefficient resolution. The other DAC generates reverse reference voltage with inverted DAC coefficients. The comparator as shown in Fig. 3-6(b) is a fully differential dynamic latch-type comparator and compares input data with DAC references. The fully differential signaling provides power supply rejection and immunity to common mode noise.

The clock generator as shown in Fig. 3-6(c) has a five-stage inverter chain and generates about 114-MHz five-phase clocks which are asynchronous to the target data rate. For stable operation, we separate supply voltage of the clock generator from the rest of circuits. This sampling clock speed is chosen so that the prototype chip can be linked to a field-programmable gate array (FPGA), which allows external monitoring of histograms. The five-phase sampling clocks are sequentially provided to the track-and-hold circuits, the comparator, and the digital controller. These multiphase clocks provide sufficient timing margins for comparator and counter, thus resulting in stable adaptation operation. The digital controller selects the best equalization coefficient that produces the histogram with the largest peak value.



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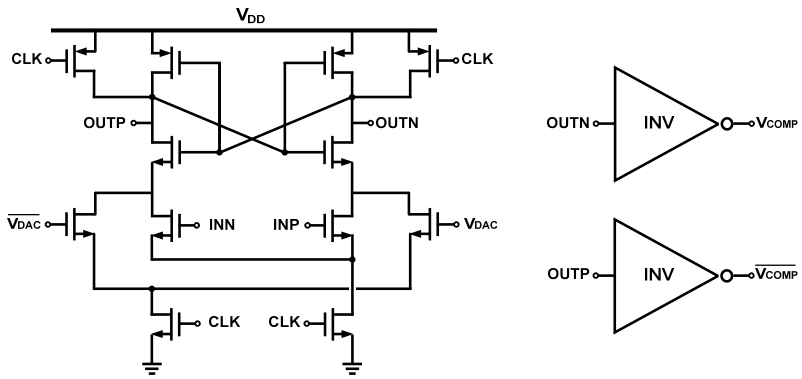

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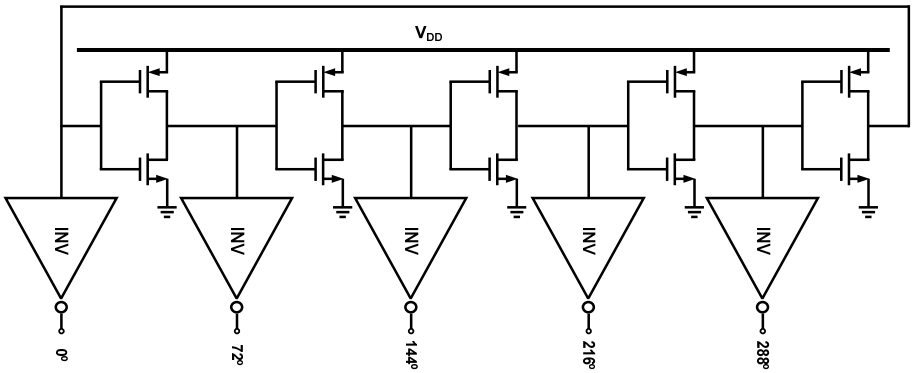


(c)

Fig. 3-6. Schematic diagrams of (a) 5-bit DAC, (b) comparator, and (c) clock generator.

3-3. Digital Controller Operation

The flow chart of adaptive equalization process is shown in Fig. 3-7. The controller is digitally synthesized and integrated on the chip. The adaptive equalization is performed as follows.

The filter coefficient is set to an initial value, and filter output V_{EQ} is compared with the reference voltage V_{DAC} from the DAC. When V_{EQ} is larger than V_{DAC}, the comparator generates a high pulse, and the counter counts up. The process is repeated for 4096 (12 bit) samples, and the register stores the counter value. Then, V_{DAC} is increased to a new value, and the aforementioned sampling and counting process is repeated for 32 DAC coefficients, resulting in the cumulative distribution function (CDF). When the CDF is differentiated, a histogram for the given filter coefficient is obtained. Then, the process is repeated for each of 16 (4 bit) filter coefficients. The controller chooses the filter coefficient having the largest peak value as the optimal equalization coefficient.

The controller produces 4096 samples with 12 bits. With this sample size, the total adaptation time required for determining the optimal filter coefficient can be estimated as follows:

$$
\begin{aligned}
&4096 \text{ (sample number)} \\
&\times 32 \text{ (reference voltage number)} \\
&\times 16 \text{ (filter coefficient number)} \\
&\times 8.7\ ns \text{ (time for each operation)} \simeq 18\ ms
\end{aligned}
\tag{3.2}
$$

It takes some time in order to determine the optimal filter coefficient for a given channel, but this scheme does not require any previous knowledge of the channel and relies on the digital block for adaptation. Thus, a promising solution for applications where the channel condition does not change after initial optimization can be achieved.

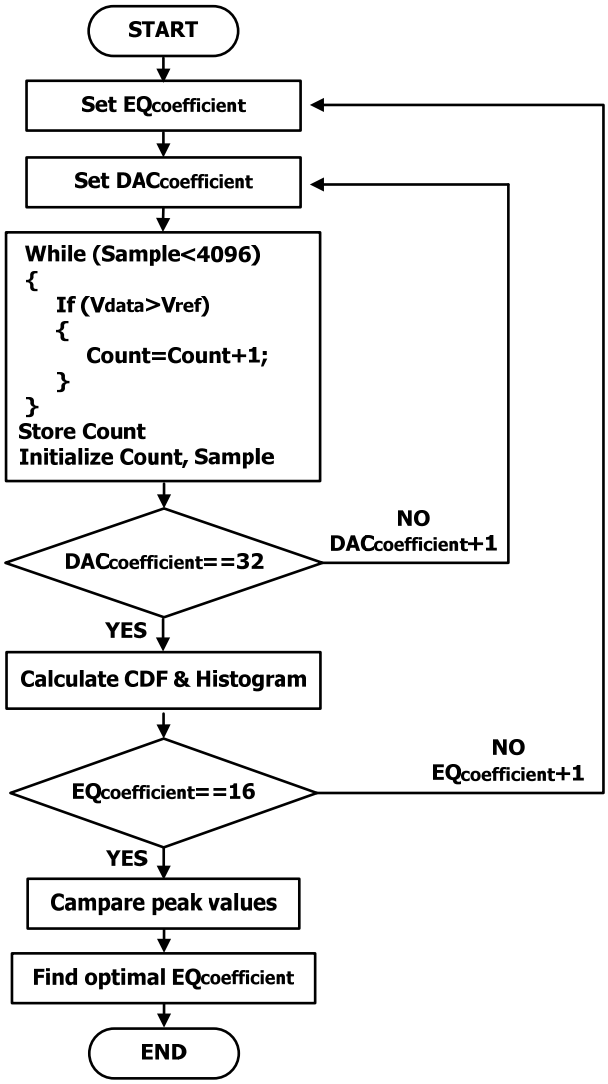


Fig. 3-7. Flow chart of equalization process.

4. Measurement Results

4-1. Chip Fabrication & Measurement Setup

Fig. 4-1 shows a die photograph of our adaptive CTLE chip fabricated in 0.13-μm CMOS technology. The chip occupies less than 340 μm × 525 μm excluding the output buffer. Our adaptation circuits consume 26 mW from 1.2-V supply.

Fig. 4-2 shows the measurement setup. A pulse pattern generator (PPG) provides differential 5.4-Gbit/s 250-mV PRBS $2^{31} - 1$ data to chip on a probe station through four different types of channels. The equalized output is observed by an oscilloscope and BER tester. The integrated digital controller can be operated in internal- or external-control mode. In the external-control mode, histograms for different filter settings are delivered to FPGA for testing purpose. In the internal-control mode, the digital controller automatically sets the optimal filter coefficient as the one producing the histogram with the largest peak value.

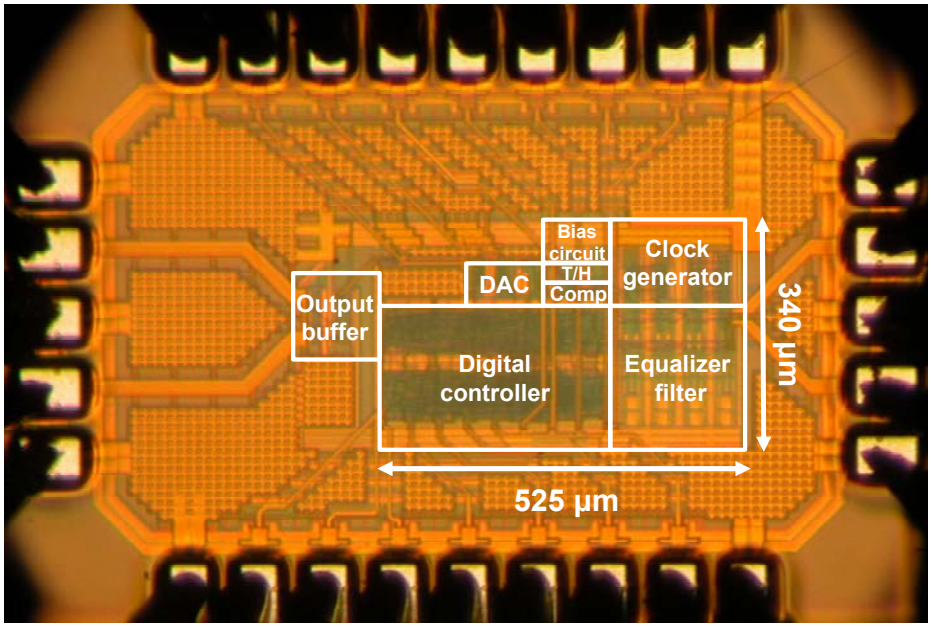


Fig. 4-1. Chip photograph of the proposed adaptive CTLE.

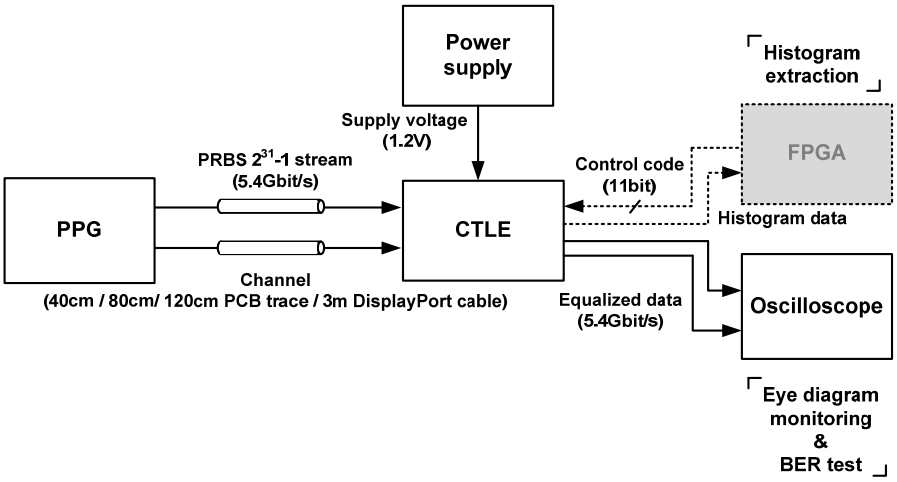
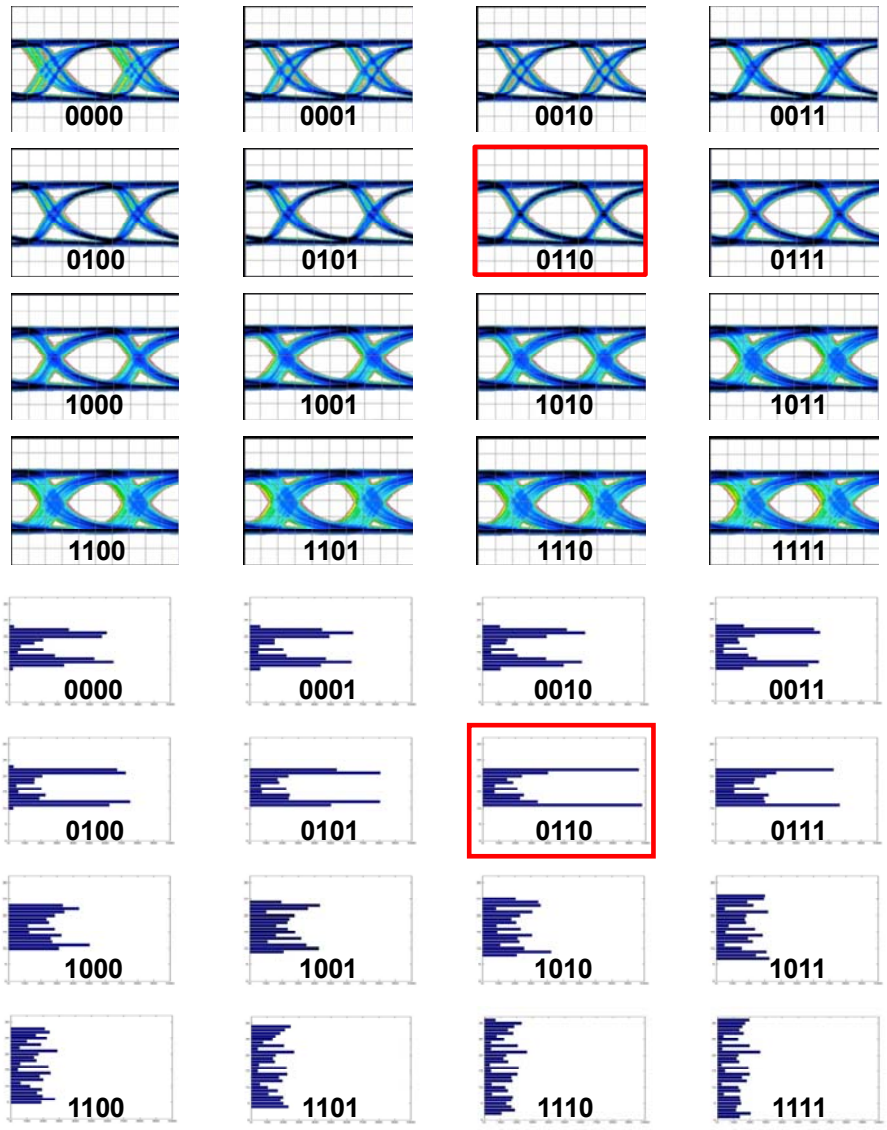


Fig. 4-2. Measurement setup.

4-2. Eye Diagram & Histogram

As the first verification, we measured the eye diagram and the histogram of equalized output for each of 16-equalization coefficients when data are transmitted through four different types of channels with the controller in the external-control mode. Fig. 4-3 shows measured eye diagrams and histograms of 16 different equalization coefficients for four different types of channels. As can be seen, different equalization coefficients with different amount of equalizing gain produce different eye diagrams and histograms.

As shown in the Fig. 4-3(a), equalization coefficient 0110 can be easily identified as the one producing the clearest eye diagram and the histogram having the largest peak value. Although histograms usually have two peaks, one of the two is larger due to uncertainty in the sampling. The digital controller simply searches for the peak having a larger value. With the controller in the internal-control mode, the controller correctly selects equalization coefficient 0110 as the optimal coefficient. Measurement with other 3 different channels showed the similar results verifying histogram scheme.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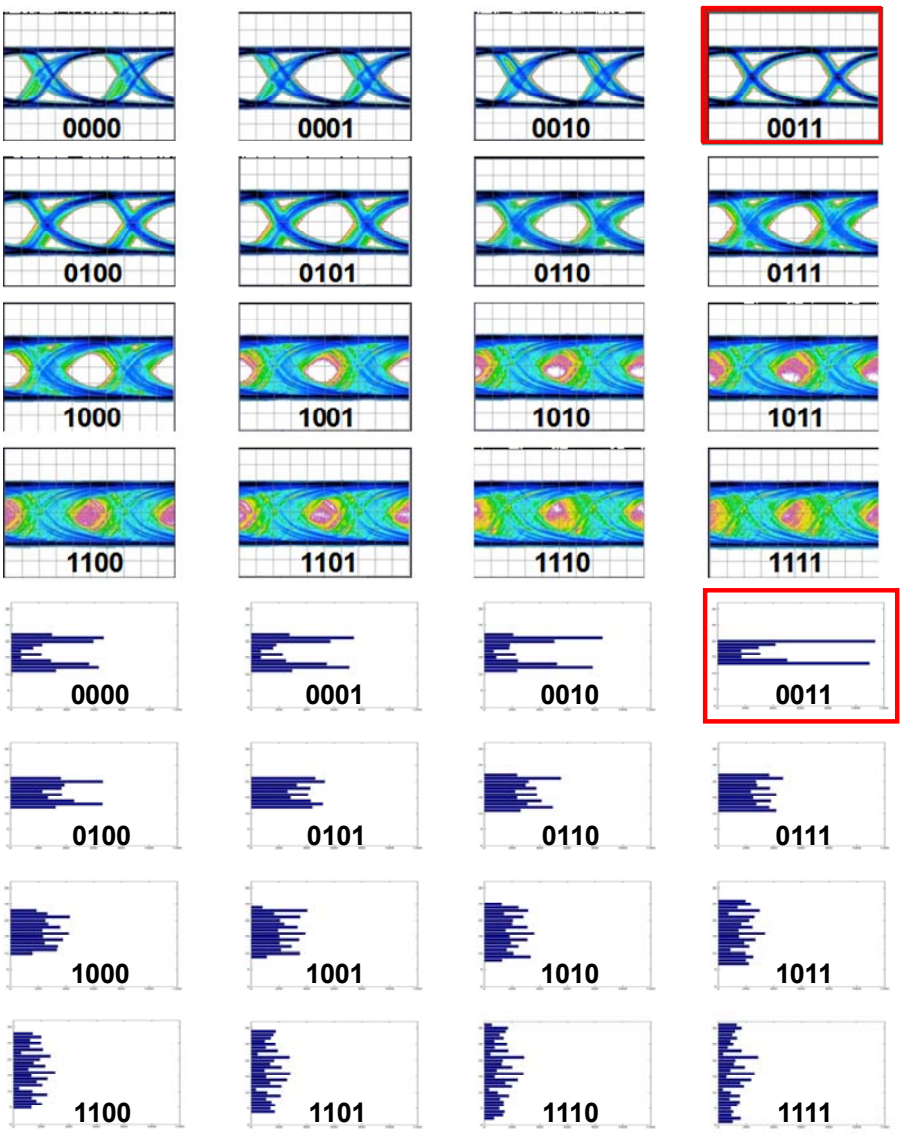
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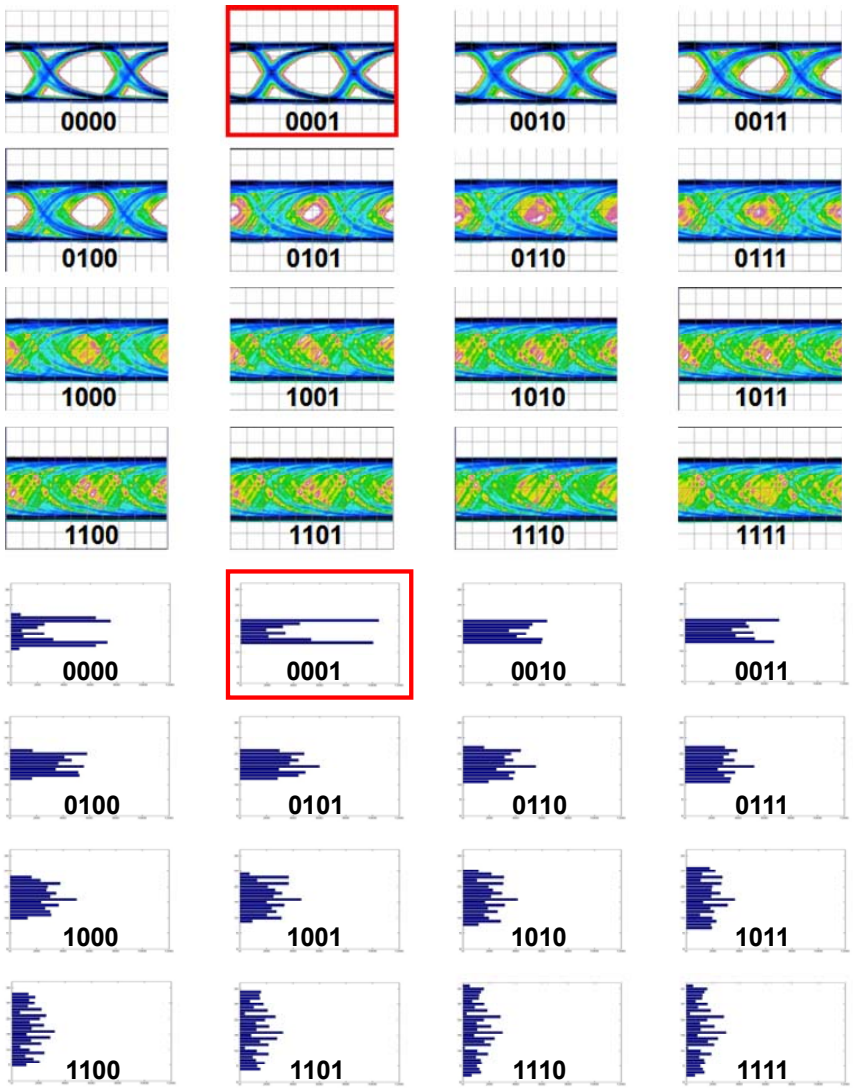
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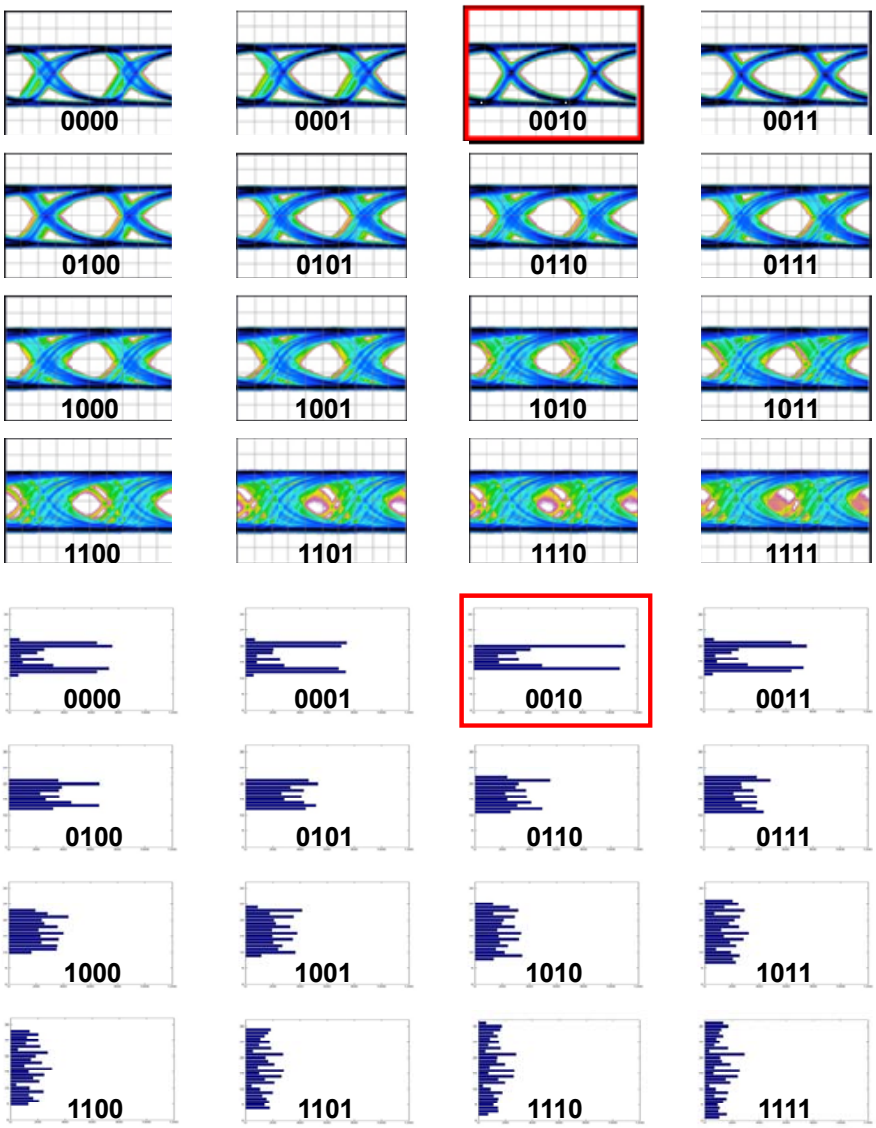


(d)

Fig. 4-3. Measured eye diagrams and histograms of each equalization coefficient for (a) 40-cm, (b) 80-cm, (c) 120-cm PCB traces and (d) 3-m DisplayPort cable.

Fig. 4-4 shows the channel response without any equalization for four different channels measured at 2.7 GHz by a network analyzer. It also shows the optimal equalizing gain automatically provided by our adaptive CTLE. As shown in the figure, the total response is close to zero indicating that our adaptive CTLE provides the optimal amount of equalizing gain that compensates channel loss for each of the four different channels.

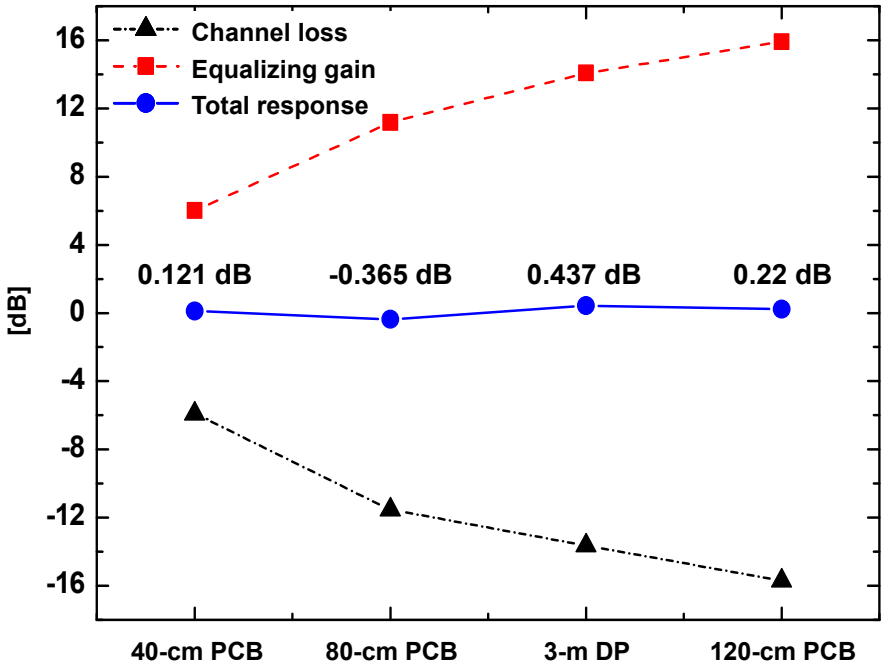


Fig. 4-4. Channel losses and corresponding optimal equalizing gains.

Fig. 4-5 shows measured eye diagrams before and after equalization for four different channels with 5.4-Gbit/s $2^{31} - 1$ PRBS data. As can be seen, all eyes are clearly open after equalization. The optimal filter coefficient for each case is adaptively determined by the circuit without any external control. The measured maximum peak-to-peak jitters are 33.62, 34.81, 36.41, and 34.73 ps, respectively. Our adaptive CTLE achieves 5.4-Gbit/s data transmission with less than error-free during 30 minutes through 40-, 80-, and 120-cm PCB traces and 3-m DisplayPort cable as shown in Fig. 4-6.

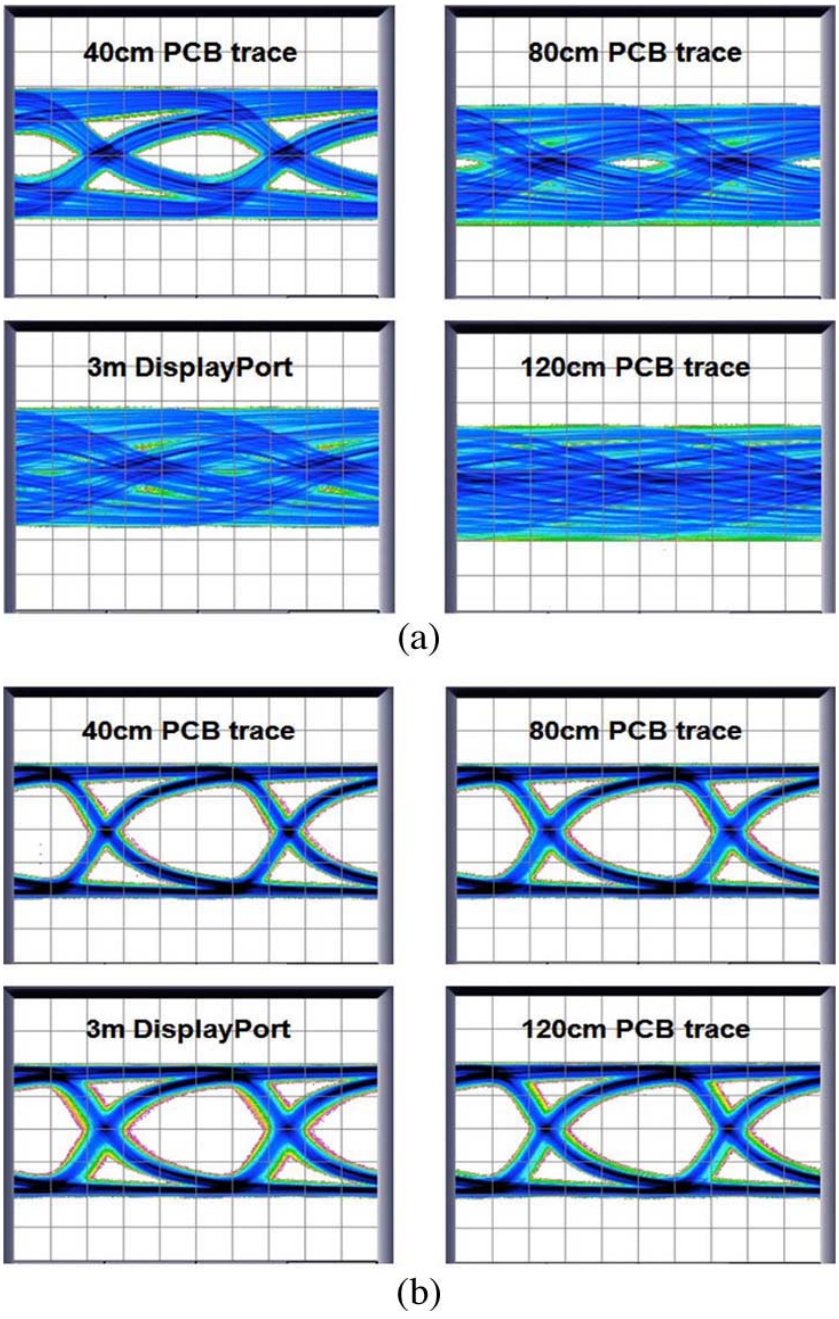


Fig. 4-5. Eye diagrams of (a) before and (b) after equalization [(a) X: 37 ps/div, Y : 100 mV/div; (b) X: 37 ps/div, Y :100 mV/div].

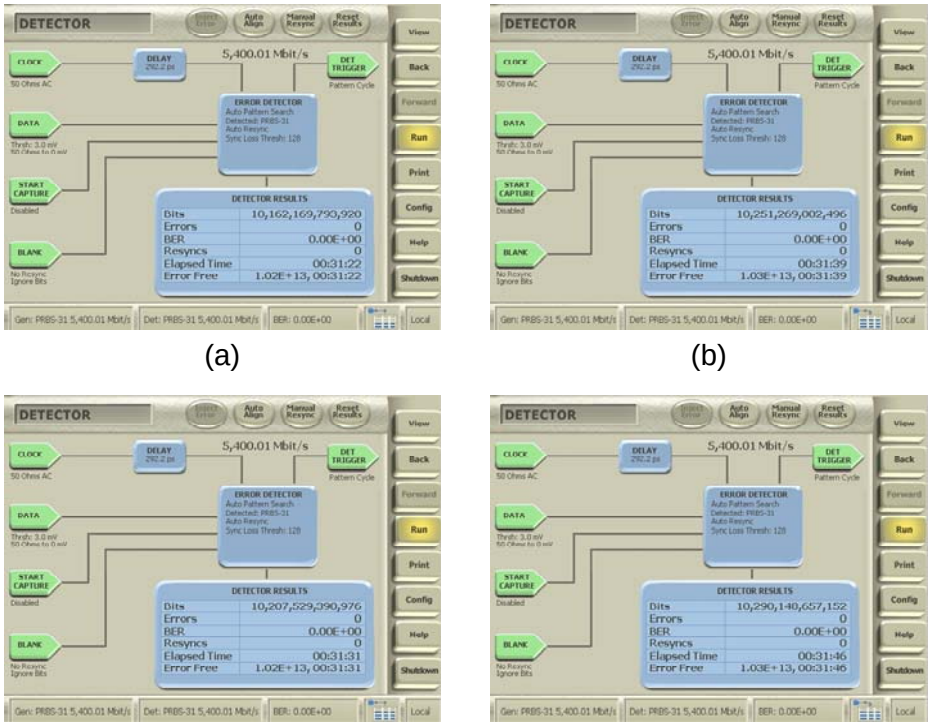


Fig. 4-6. Measured BERs for (a) 40-cm, (b) 80-cm, (c) 120-cm PCB traces and (d) 3-m DisplayPort cable.

4-3. Histogram Reliability

The prototype chip monitors the signal quality by the asynchronously under-sampled histograms. Therefore, the histograms guarantee the reliability of signal quality estimation. To verify reliability of our scheme, we measure in the external-control mode the peak value of the optimal histogram for each channel with varying sample sizes. The sample size is varied from 1000 to 7000 in increment of 1000. Measurement at each sample size is repeated 100 times, and their averages and variances are determined. Here, the results correspond to p and the variance e. Where the p is the probability of peak value in the histogram and e is the maximum variation to distinguish the largest peak among the near optimal peak value.

Fig. 4-7(a) shows measured p and e for 40-cm PCB trace for different sample sizes. As expected, measured e decreases as the sample size increases. When the sample size is larger than 4000, measured e is less than 1.8%. Fig. 10(e) shows the calculated p and e for different sample sizes. There is a good agreement between the results shown in Fig. 4-7(a) and (e), confirming accuracy in our analysis. Measurement results from other channel types showed the similar results.

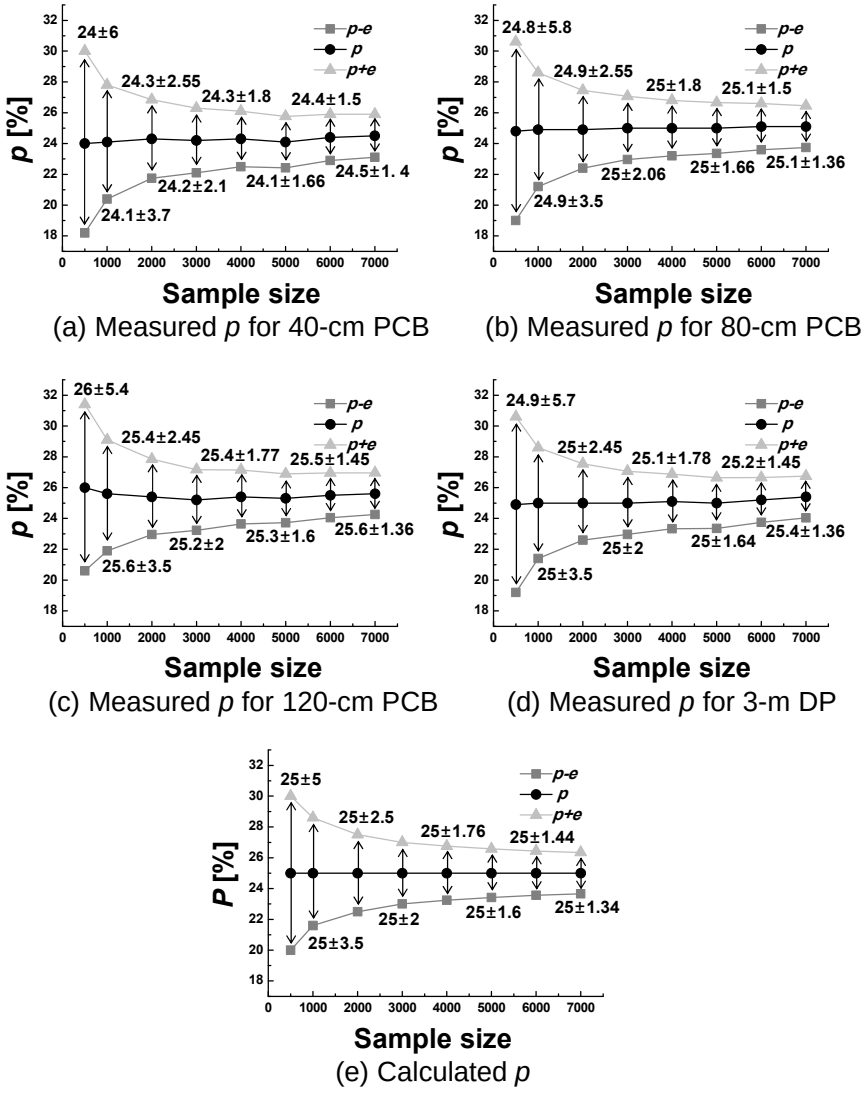


Fig. 4-7. Measured p and e of (a) 40-cm, (b) 80-cm, and (c) 120-cm PCB traces, (d) 3-m DisplayPort cable and (e) calculated *p* and *e* for different sample sizes.

4-4. Summary

We have demonstrated new adaptive CTLE using asynchronous under-sampled histograms. Using an asynchronous under-sampling clock, data amplitude histograms are obtained at various equalizing filter coefficient settings, and the one producing the histogram with the largest peak value is selected as the optimal coefficient. With a prototype chip fabricated in 0.13-μm CMOS technology, we successfully equalized 5.4-Gbit/s data transmitted through 40-, 80-, and 120-cm PCB traces and 3-m DisplayPort cable. In addition, we experimentally confirmed the reliability of our sampling method. We believe that our adaptive CTLE is simpler than any previously reported EOM-based equalizers because it eliminates high-speed clock paths and phase rotator circuitry, and reduces the number of required samplers.

Table 4-1 shows performance summary of our adaptive CTLE [29] in comparison with other previously reported EOM-based equalizers. Although a direct comparison of power consumption and chip size is not possible due to different data rates, we verify that our adaptation scheme can be extended to 10-Gbit/s operation while maintaining its advantages of small power consumption and chip size in next chapter.

Table 4-1

Performance comparison of the proposed adaptive CTLE.

	[16]	[17]	[18]	**[28]**
Year	2005	2009	2010	**2011**
Process	CMOS 0.13 μm	CMOS 0.18 μm	CMOS 65 nm	**CMOS 0.13 μm**
Signal quality monitoring	Sync. 2-D EOM	Sync. 2-D EOM	1-D EOM	**Async. amplitude histogram**
Adaptive equalization	Not implemented	Not implemented	Off-chip monitoring	**On-chip monitoring**
Data rate	12.5 Gbit/s	10 Gbit/s	10 Gbit/s	**5.4 Gbit/s**
Sampling clock speed	12.5 GHz	10 GHz	N/A	**114 MHz**
Power consumption	330 mW*	171 mW*	302 mW**	**35 mW***
Chip area	0.26 mm^2*	0.06 mm^2*	0.23 mm^2**	**0.18 mm^2***

*: contains only eye-opening monitoring circuit without equalizing filter

**: off-chip PDF extraction

***: includes integrated digital controller

5. Application Extension

5-1. Low-Power Adaptive CTLE

In high-speed serial link applications, the demand for power consumption reduction is becoming stronger. Various low-power adaptive equalizers have been reported. A tunable passive filter with power comparison adaptation can achieve low-power consumption but further improvement is required in input impedance matching and output swing levels [30]. Decision feedback equalizers (DFEs) have been used in low-power transceivers [31]. For DFEs, however, clock recovery and distribution circuits are required, making it difficult to use these equalizers if received data eyes are initially closed. CTLEs are widely used due to their simple architecture and good linearity for low-power application [9]-[11].

Table 5-1 compares performances of previously reported low-power CTLE filters. An active inductor technique with low voltage headroom provides area-efficient alternative for passive inductive terminations and offers channel loss compensation through tunable peaking, while consuming a small amount of overhead power. However, it cannot fulfill our design target due to limited equalizing gains [9]. An

interleaved active feedback topology incorporated with additional capacitive and resistive source degeneration achieves enough equalizing gain and bandwidth extension. But several cascading gain cells with interleaved active feedback cells cannot satisfy power constraint [10]. A filter using capacitive source degeneration and negative capacitance circuits provides enough high-frequency boosting without sacrificing DC gain and lowest power consumption [11].

Table 5-1

Performance comparison of the CTLE filter.

	[9]	[10]	[11]
Technology	CMOS 90 nm	CMOS 0.13 μm	CMOS 0.13 μm
Filter type	Active inductor	Active feedback	Negative cap.
Data rate	10 Gbit/s	10 Gbit/s	10 Gbit/s
Boosting gain	3.1 dB at 5 GHz	20 dB at 5 GHz	15 dB at 5 GHz
Chip area	425 μm^2	129000 μm^2	6500 μm^2*
Supply voltage	1 V	1.2 V	1.2 V
Power consumption	8.8 mW	14 mW	6 mW*

*: includes adaptation block

Our design goal is 10-Gbit/s data transmission over 40-cm FR4 PCB trace with low-power consumption. The minimum power consumption of analog circuits is basically determined by the supply voltage, the signal peak-to-peak amplitude and the required bandwidth. We set 250-mV peak-to-peak swing from 1-V supply as our design specification. Current-mode logic circuits are designed with small-size input pairs using low threshold voltage transistors for improvement in both power dissipation and circuit speed. Passive inductors are not used in order to reduce the silicon area.

The target channel has 10.48-dB loss at 5 GHz as show in Fig. 5-1. Our adaptive CTLE is designed to have up to 15 dB equalizing gain at 5 GHz. Fig. 5-2 shows the overall configuration of the proposed low-power adaptive CTLE. It has a 3-bit variable CTLE filter, two UGBs, output buffers, a 4-phase clock divider, two DACs, four track-and-hold circuits, a clocked sense amplifier, and an integrated digital controller. The digital controller turns off the circuit blocks such as DACs, clocked sense amplifier, clock divider, and unit gain buffer with high threshold voltage transistor switches after the adaptation process is completed. Also, the dynamic power of a digital controller is reduced due to operating clock off.

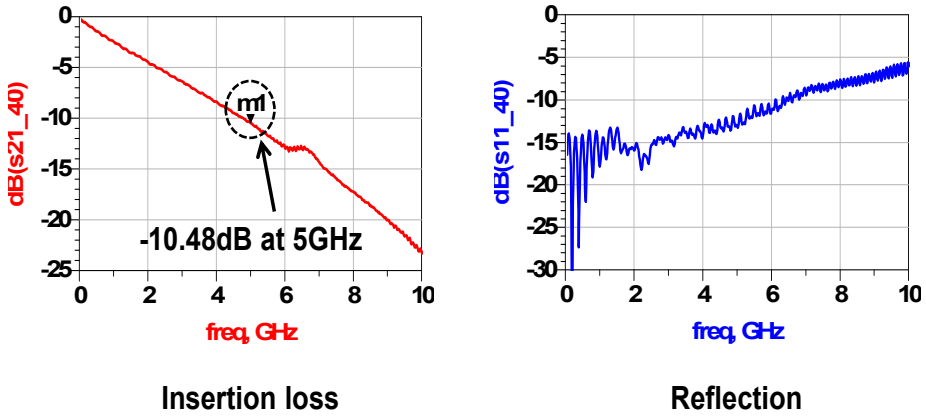


Fig. 5-1. Measured loss and reflection of 40-cm PCB trace.

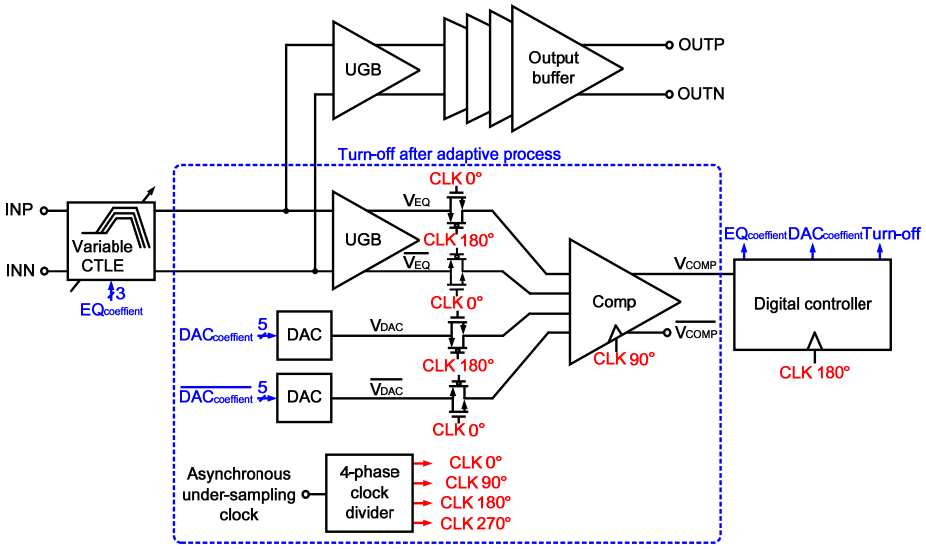


Fig. 5-2. Block diagram of low-power adaptive CTLE.

The 2-stage CTLE is designed to have 4.5-dB to 15-dB equalizing gain with 3-bit capacitor array, which provides 8-different gain levels with approximately 1.5-dB increment controlled by 3-bit equalization coefficients [11]. It guarantees uniform output swing despite changing equalization coefficient so that histogram is properly calculated with the fixed DAC resolution.

A 5-bit DAC generates 32-level reference voltages with 16.13-mV resolution. The reference level is controlled from 500 mV to 1 V by PMOS load switches with 5-bit DAC coefficients. The 4-input differentially clocked sense amplifier compares equalized data with DAC references. The clock divider provides 107-MHz quadrature clocks from external 214-MHz clock which are asynchronous to the target data rate. These quadrature sampling clocks are sequentially provided to track-and-hold circuits, the comparator, and the digital controller for stable operation.

The adaptive process in digital controller is similar to previously demonstrated version. The digital controller selects the equalization coefficient having the largest peak value as the optimal equalization coefficient. After adaptation, the digital controller turns off all the circuit blocks needed for adaptation so that power consumption can be minimized. They can be turned on again when demanded by a higher

level control (not implemented) if there is any degradation in received data quality. With 4096 samples used for each histogram, the total adaptation time is estimated 9.8 ms.

Fig. 5-3 shows a die photograph of our adaptive CTLE chip fabricated in 65-nm CMOS technology. The core occupies 0.0386-mm^2 die area excluding output buffers.

Fig. 5-4 shows measured eye diagrams before and after equalization for 40-cm FR4 PCB trace with 10-Gbit/s $2^{31} - 1$ PRBS data. Eyes are clearly open after equalization. For this eye measurement, the optimal equalization coefficient is adaptively determined without any external control. Our adaptive equalizer achieves 10-Gbit/s data transmission with less than error-free during 15 minutes. The measured maximum peak-to-peak jitter is 26.6 ps. The power consumption is 4.66 mW without output buffers from 1-V supply in the external-control mode when all the adaptation circuits are on. After adaptation in the internal-control mode, the power consumption is 2.49 mW.

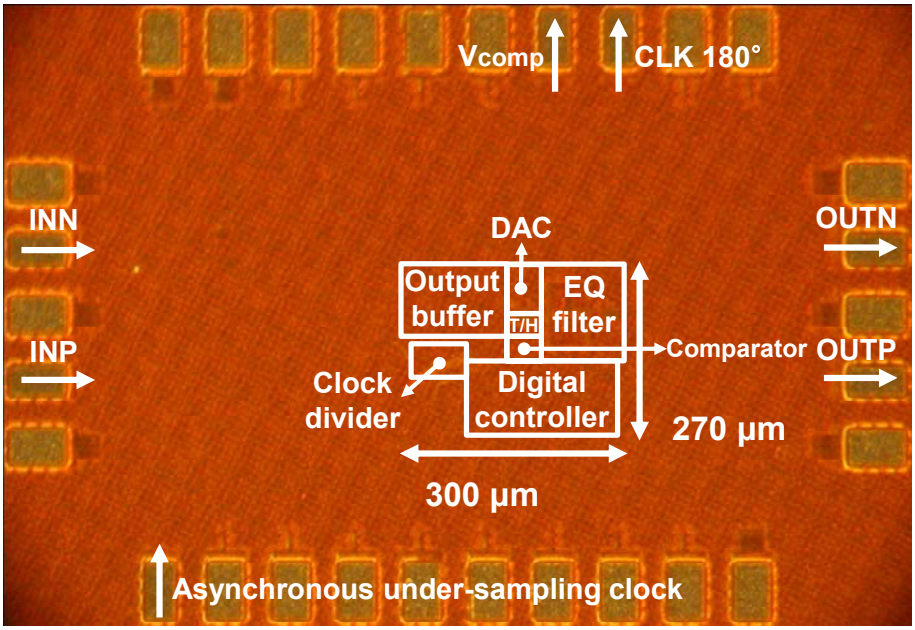


Fig. 5-3. Chip photograph of the low-power adaptive CTLE.

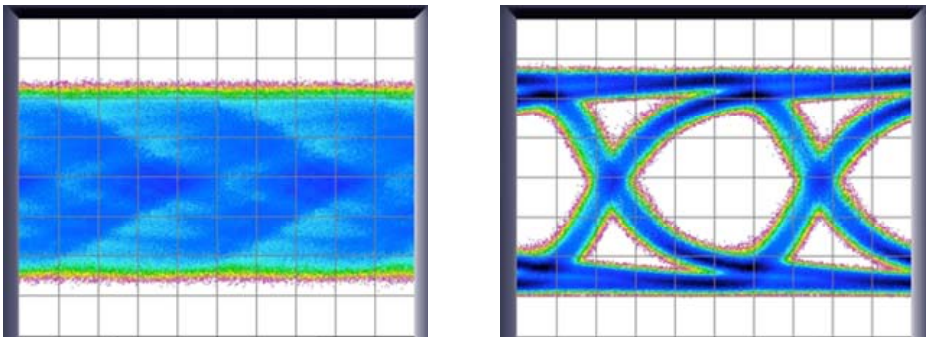


Fig. 5-4. Eye diagrams of (a) before and (b) after equalization.
[(a) X: 19 ps/div, Y : 100 mV/div; (b) X: 19 ps/div, Y :100 mV/div].

Table 5-2 compares the performance of our CTLE reported in this work [32] with previously reported low-power adaptive equalizers operating at around 10 Gbit/s. Although the passive adaptive equalizer in [30] has the lowest power consumption, it should be noted that the passive equalizer does not include a limiting amplifier, which is required for boosting up the output to the desired level and can consume a substantial amount of power at 10 Gbit/s. Although direct comparison of power consumption is difficult for CTLEs realized in different process technologies and having different amounts of peaking gain, our CTLE achieves the lowest power consumption. Furthermore, it has the advantage in that adaptation algorithm is performed with the integrated digital block, which consumes about 1mW little power, is robust against any process variations, and can be turned off when not needed. We believe our adaptive CTLE can be a promising solution for demanding high-speed wire-line applications, especially for systems whose channel conditions does not change frequently.

Table 5-2

Performance comparison of the proposed low-power adaptive CTLE.

	[30]	[31]	[8]	[11]	**[32]**
Technology	CMOS 90 nm	CMOS 65 nm	CMOS 0.11 μm	CMOS 0.13 μm	**CMOS 65 nm**
Filter type	Passive	DFE-IIR	CTLE	CTLE	**CTLE**
Adaptation	Power comparison	N/A	ISI monitoring	Power comparison	**Asynch. histogram**
Data rate	12 Gbit/s	10 Gbit/s	10 Gbit/s	10 Gbit/s	**10 Gbit/s**
BER	$< 10^{-10}$	$< 10^{-9}$	$< 10^{-12}$	N/A	**$< 10^{-13}$**
Boosting gain	13 dB at 6 GHz	27 dB at 5 GHz	20 dB at 5 GHz	15 dB at 5 GHz	**15 dB at 5 GHz**
Chip area	0.0336 mm^2	0.01725 mm^2	0.0156 mm^2	0.0065 mm^2	**0.0386 mm^2**
Supply voltage	1 V	1 V	1.2 V	1.2 V	**1 V**
Power consumption	1 mW	7 mW	23.2 mW	6 mW	**4.66 mW* / 2.49 mW****
Figure of Merit [33] (pJ/bit/dB)	0.006	0.026	0.116	0.04	**0.031* / 0.016***

Power consumption and chip area without output buffers.

*: During adaptation

**: After adaptation

We presented a 10-Gb/s low-power adaptive CTLE which automatically selects the optimal equalization coefficient among several pre-determined values by searching for the equalization coefficient that produces the largest peak value in histograms obtained with asynchronous under-sampling. The blocks used for adaptation are turned off for power reduction after the optimal equalization condition is achieved. A prototype chip realized in 65-nm CMOS technology successfully achieves adaptive equalization for 10-Gbit/s $2^{31} - 1$ PRBS data through 40-cm FR4 PCB trace. It consumes 4.66 mW during adaptation and 2.49 mW after adaptation from 1-V supply and occupies 0.0386 mm^2 of die area.

5-2. Adaptive Single-Ended EQ-DCC

As the performance of computer systems continues to improve, the required interface data rates increase. Although differential signaling is often used for high-speed interfaces, there are applications such as memory interfaces where single-ended signaling is required for cost effectiveness. Differential signaling requires twice as many signal pins compared to single-ended signaling and it may not be suitable for applications in which the pin number or routing area is limited.

For single-ended signaling, duty-cycle distortion (DCD) and ISI can be a serious problem [34]. DCD is often due to asymmetries caused by threshold offsets and slew rate mismatches in transmitter [35]. DCD can be represented by the eye crossing level where rising edges intersect falling edges in the eye diagram as shown in Fig. 5-5. ISI is produced when one symbol interferes with subsequent symbols due to limited bandwidth of data transmission media. Influences of DCD and ISI on the eye diagram are shown in Fig. 5-6. As can be seen, DCD and ISI can seriously degrade the eye diagram and they should be mitigated in order to achieve high-speed single-ended interfaces. Often equalizers (EQs) are used for compensating ISI due to channel bandwidth limitation and duty-cycle correctors (DCCs) for correcting DCD.

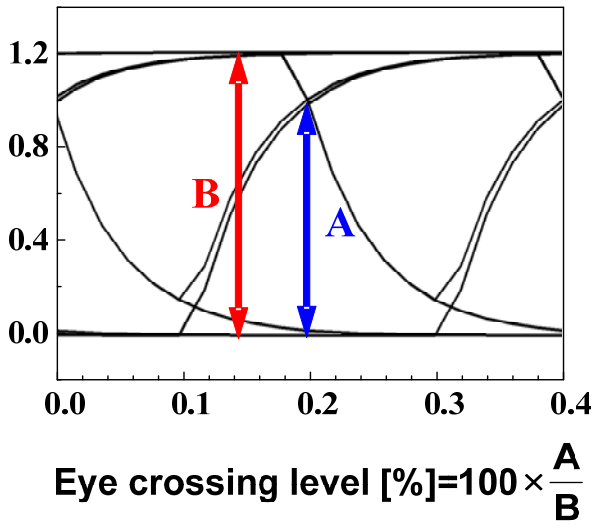


Fig. 5-5. Eye diagrams with DCD and eye crossing level definition.

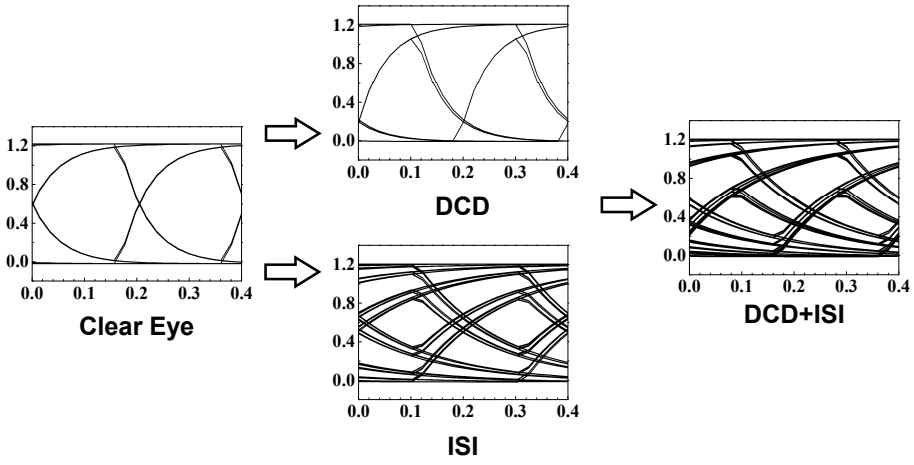


Fig. 5-6. Influence of ISI and DCD on eye diagrams.

Previously reported single-ended EQs are based on the differential structure [36], [37]. They convert single-ended signals into differential signals with pre-drivers and then perform equalization, which results in increased power consumption. Although previously reported DCC circuits work for clock signals [38], [39], they do not for none-return-to-zero (NRZ) data. Therefore, a new approach is needed that can compensate both DCD and ISI for single-end NRZ signals. Furthermore, it is highly desirable that the technique operates in an adaptive manner so that the optimal compensation can be achieved even with different transmitter conditions and process variations.

We demonstrate that our previously reported adaptive equalization based on asynchronously under-sampled histograms [29] can be extended for compensating both DCD and ISI for single-ended signaling [40]. Asynchronously under-sampled histograms can provide useful information on the impairments caused by DCD and ISI without necessity of clock recovery, which greatly reduce the required system complexity. In addition, low-speed asynchronous under-sampling causes less voltage spikes and electro-magnetic interferences (EMIs). In this chapter, we present a 5-Gbit/s adaptive single-ended EQ-DCC based on this adaptation technique.

Our adaptation scheme is based on the simple observation that the clearest eye diagram produces the largest peak value in the asynchronously under-sampled histograms. In addition, the same histograms can be used for DCC since the eye diagram for signals with 50% duty-cycle has two peaks with equal height in the histogram which representing the equal probability of capturing logic high or low. Fig. 5-6 shows the matlab simulation results that confirm these observations. For the simulation, 5-Gbit/s $2^7 - 1$ PRBS data having 25% eye-crossing level are transmitted through 80-cm FR4 PCB trace. The transmitted signals are asynchronously sampled with 113-MHz clock and compared with 16-amplitude levels for obtaining amplitude distribution histograms. The sample size for each histogram is 4096. As can be seen in Fig. 5-7(a), the eye without any equalization nor duty-cycle correction is almost closed. This eye can be open first by an EQ whose filter coefficient is determined so that the resulting histogram produces the largest peak as shown in Fig. 5-7(b). Then, 50% duty-cycle is achieved by DCC whose optimal setting is determined so that top and bottom peaks have the smallest difference as shown in Fig. 5-7(c).

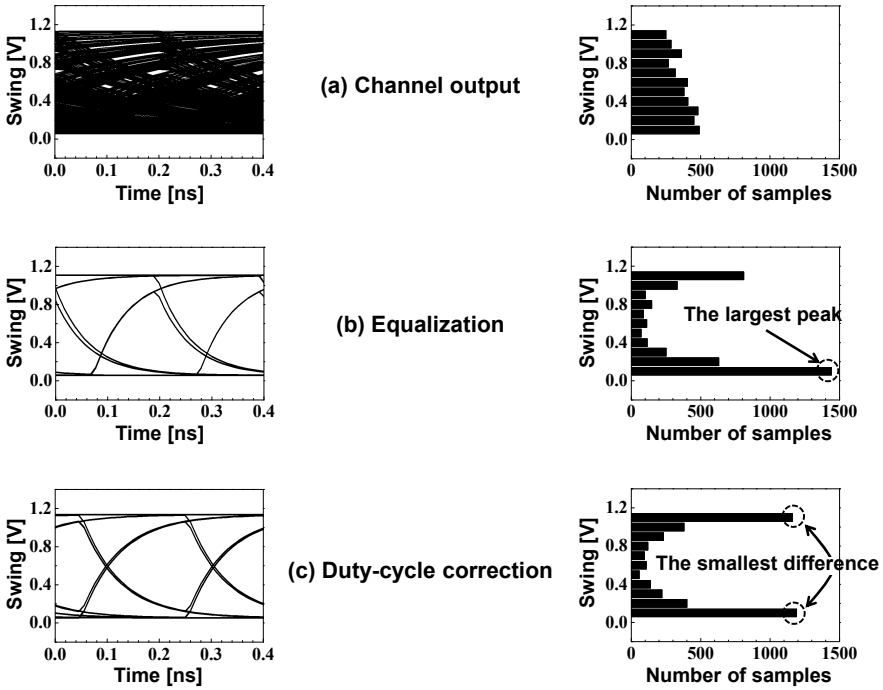


Fig. 5-7. Simulated eye diagrams and histograms: (a) Channel output (b) After equalization (c) After duty-cycle correction.

Fig. 5-8 shows the block diagram of the implemented circuit. It has a 3-bit single-ended EQ filter, a 4-bit single-ended DCC, five UGBs, a 4-phase clock divider, two 4-bit DACs, four track-and-hold circuits, two comparators, a multiplexer, and an integrated digital controller. Fig. 5-9(a) shows the UGB incorporating active inductor to provide isolation from clock feed-through. The UGB has 8-GHz 3-dB bandwidth with 0.6-mW power consumption. In addition, Thevenin parallel termination is used for input impedance matching at input UGB. Fig. 5-9(b) shows the comparator incorporating NMOS and PMOS type input pairs for full rail common mode range to extract histograms by comparing EQ and DCC output with reference voltage. The comparator offset was confirmed less than 5 mV from post layout simulation. The 4-bit resister ladder DAC as shown in Fig. 5-9(c) generates 16-level reference voltages with 0.1 mW power consumption. The reference level is controlled from 0 V to 1.2 V with 80 mV resolution. The digital controller chooses the optimal EQ coefficient that produces the largest peak value in histograms and the optimal DCC coefficient that produces the smallest difference in peak values in histograms. Track-and-hold circuits offer sufficient timing margin for the sampling process. The multiplexer adjusts sequential operation of equalization and duty-cycle correction. The clock divider generates 113-MHz

quadrature clocks which are asynchronous to data.

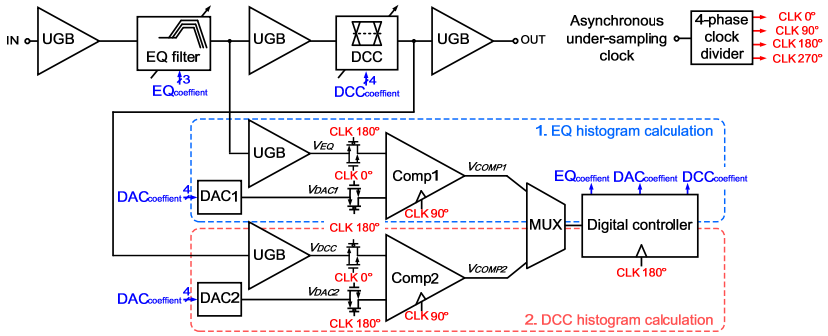


Fig. 5-8. Block diagram of proposed adaptive single-ended EQ-DCC.

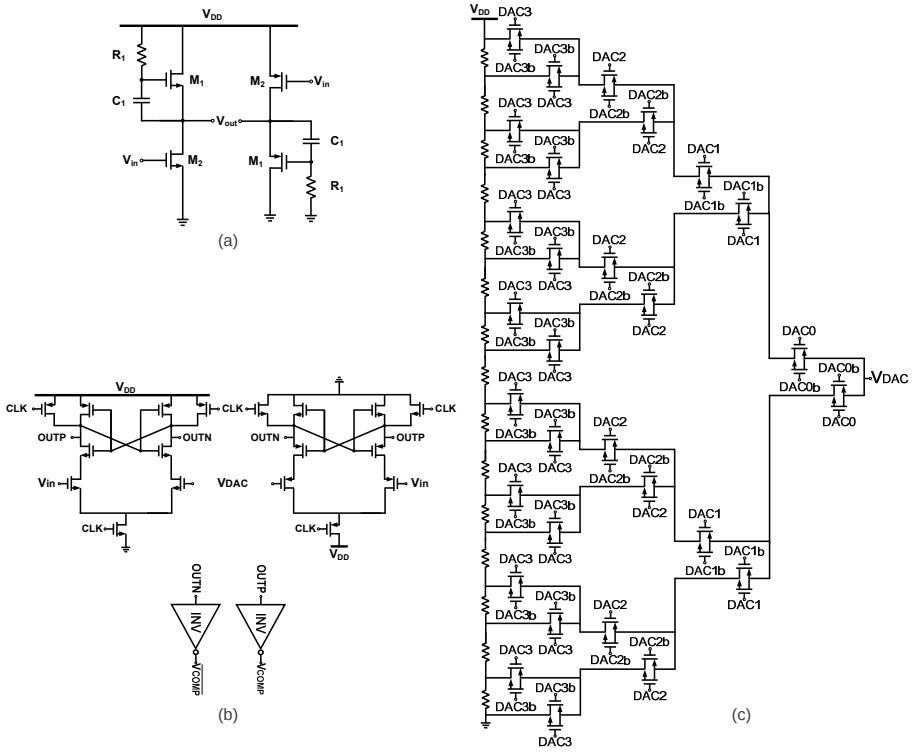


Fig. 5-9. Schematic diagrams of (a) single-ended UGB, (b) comparator and (c) DAC.

As shown in Fig. 5-10, the target channel is 80-cm FR4 PCB trace having 10.9-dB insertion loss at 2.5 GHz. Fig. 5-11 shows the schematic of single-ended EQ filter and DCC. As shown in Fig. 5-11(a), 5-stage single-ended EQ filter incorporating source degeneration and active inductor generates 6.5- to 17-dB tunable boosting at 2.5 GHz for 10.9-dB channel loss. The EQ transfer function can be determined as

$$\frac{V_{out}}{V_{in}} \cong -\frac{g_{m2}(1+sC_1R_1)}{sC_1+g_{m1}} \cdot \frac{1+sC_sR_s}{1+sC_sR_s+g_{m2}R_s} \tag{5.1}$$

where $g_{m1} = (g_{mN1}+g_{mP1})/2$ and $g_{m2} = (g_{mN2}+g_{mP2})/2$ represent the transconductance of input and load transistors. Two zeros for equalization are generated by C_S and R_S of source degeneration as well as C_1 and R_1 of the active inductor. Other 4-stage filter is identical to upper one. R_1 is digitally controlled by 3-bit thermometer decoder for 8-different levels having 1.5-dB equalizing gain resolution. The NP-type input pair can drive the full CMOS input range. As shown in Fig. 5-11(b), single-ended DCC is a 6-stage cascaded slew-rate controlled inverter [41]. Each stage can adjust the falling transition of data by a digitally switching load. The most significant bit (MSB) DCC3 represents the direction of DCC so that the multiplexer can select either even or odd DCC unit cell. Remaining 3-bits control the 16-level DCC

slew rate with binary incremented MOSFET size for compensating 25~75% eye crossing level.

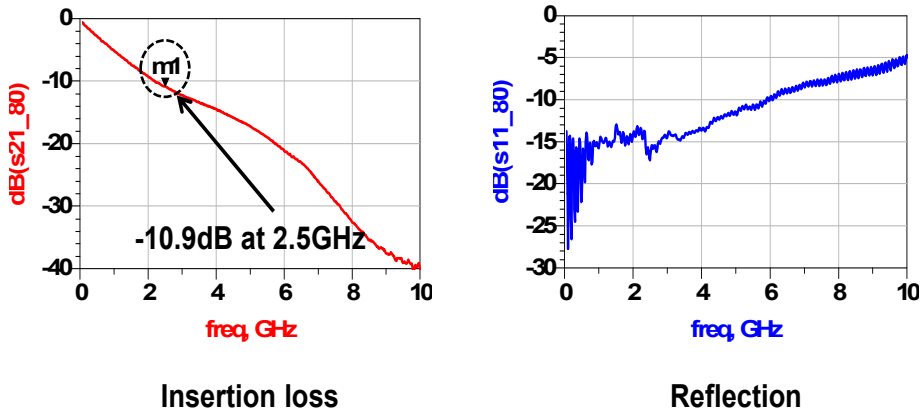


Fig. 5-10. Measured loss and reflection of 80-cm PCB trace.

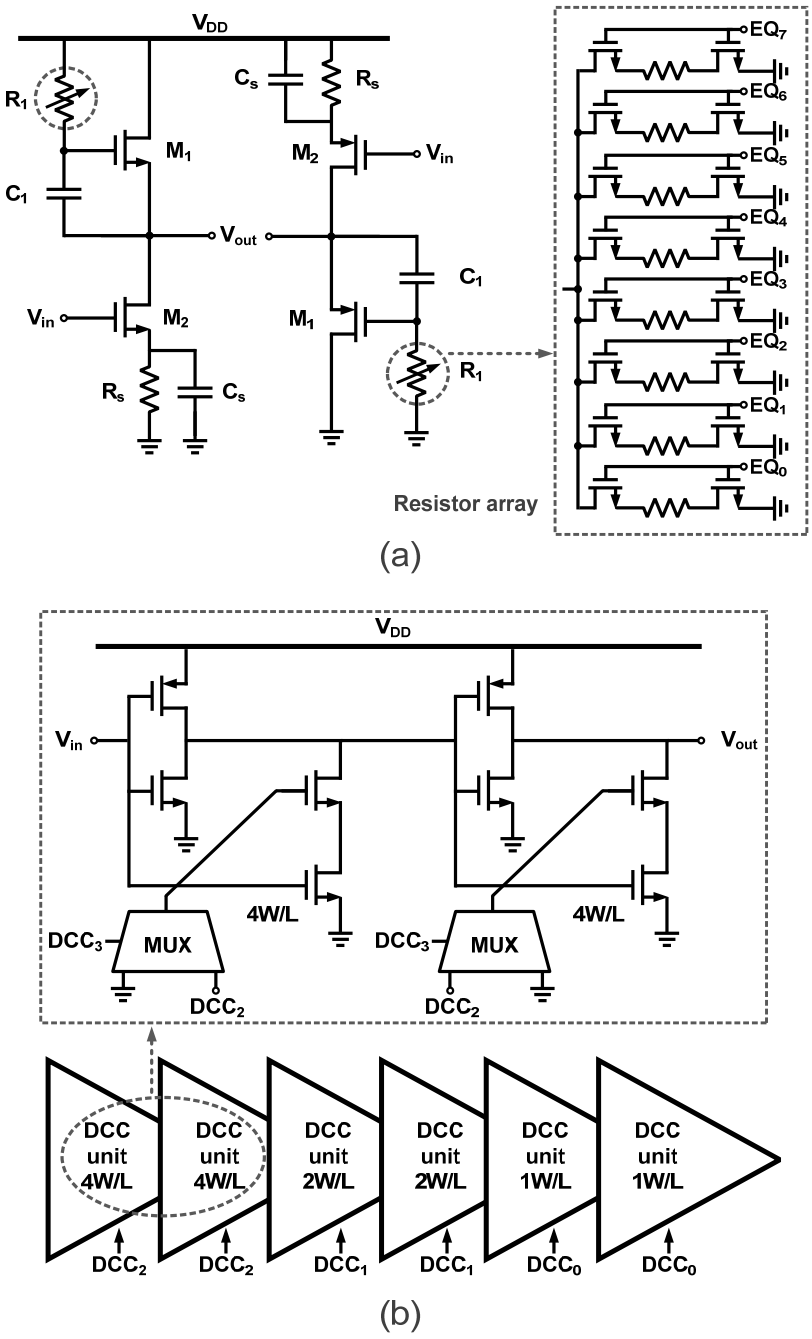


Fig. 5-11. Schematic diagrams of single-ended (a) EQ filter and (b) DCC.

Fig. 5-12 shows the adaptive equalization and duty-cycle correction process. Initially, an EQ coefficient is applied to the single-ended EQ filter and the DAC coefficient is also applied to DAC1. After that, a reference voltage, V_{REF1}, is applied to the comparator. When the signal level, V_{EQ}, is higher than V_{REF1} at the sampling point, a comparator generates a high pulse, V_{COMP1}. A counter counts up by one and the register stores the accumulated value during 4096 samples. With a full scan of reference voltages, the resulting CDF for the given EQ coefficient is obtained, differentiating which produces a histogram. This process is repeated for each of 8-EQ coefficients. The digital controller determines the EQ coefficient having the largest peak value in histograms and chooses this as the optimal EQ coefficient. After equalization, adaptive duty-cycle correction process is repeated for 16-DCC coefficient. Finally, the digital controller determines the DCC coefficient producing the smallest peak difference in histograms and chooses this as the optimal DCC coefficient. With 4096 samples used for each histogram, the total adaptation time is estimated 13.9 ms.

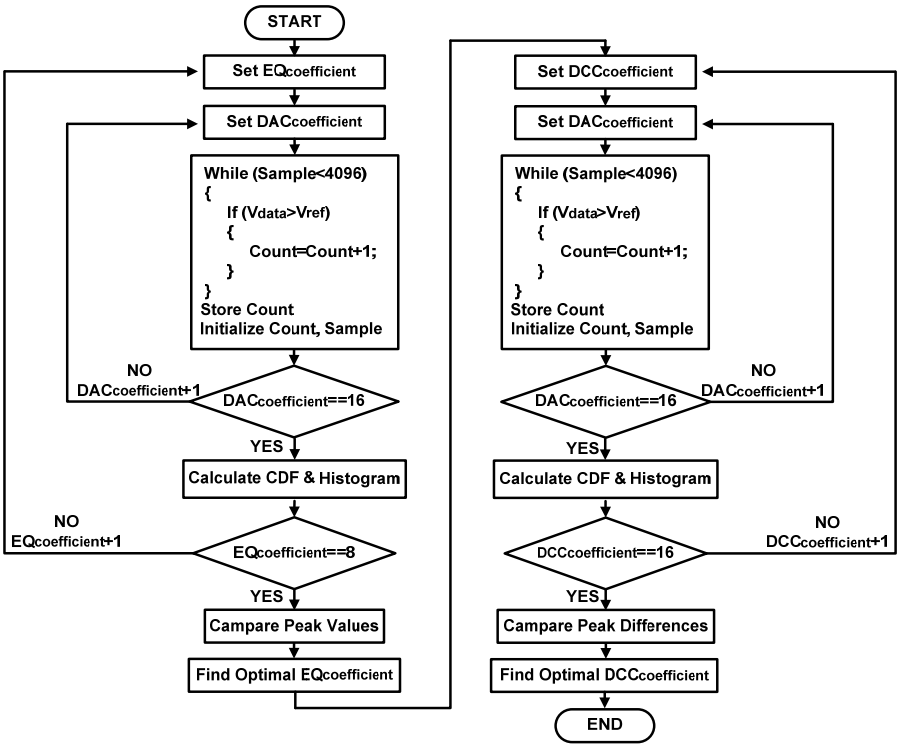


Fig. 5-12. Flow chart of adaptive equalization and duty-cycle correction process.

The prototype chip is fabricated with a standard 0.13-μm CMOS technology. Fig. 5-13 shows the microphotograph of the fabricated chip. The chip core occupies 0.17-mm^2 die area and consumes 25 mW from 1.2-V power supply.

Fig. 5-14 shows measured eye diagrams and histograms without any compensation, after adaptive equalization, and duty-cycle correction. The eye is clearly open after adaptive equalization and duty-cycle is well corrected after adaptive duty-cycle correction. For this measurement, selected EQ coefficient and DCC coefficient are automatically determined by the built-in digital controller. The measured peak-to-peak jitter is 51.9 ps.

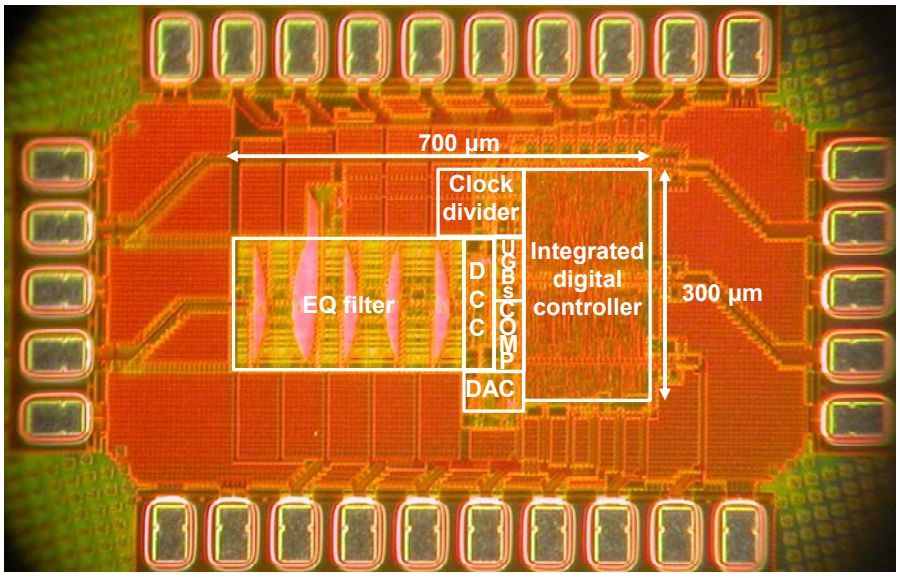
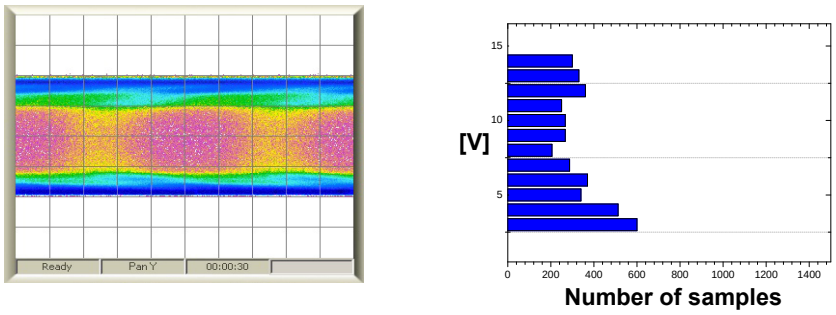
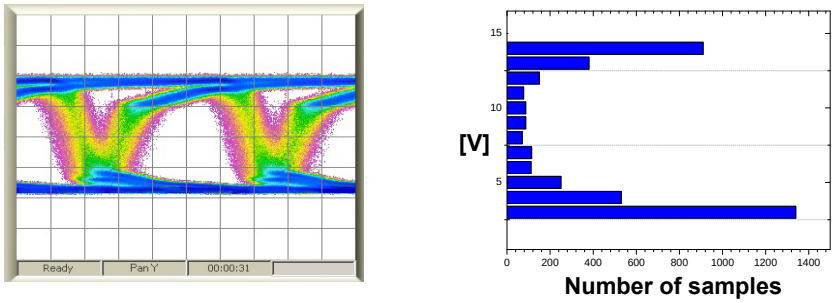


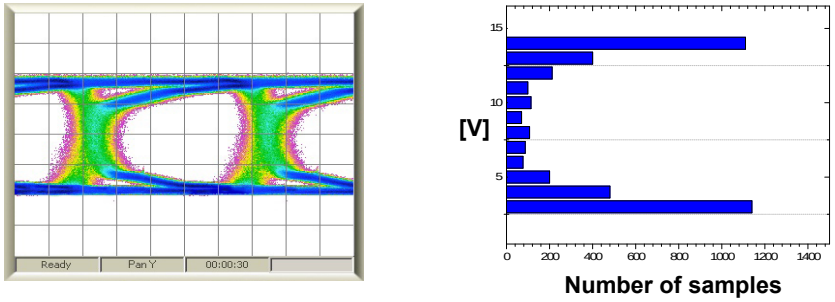
Fig. 5-13. Chip photograph of the single-ended adaptive EQ-DCC.



(a)



(b)



(c)

Fig. 5-14. Measured eye diagrams and histograms (a) without adaptation, (b) after adaptive equalization, and (c) after adaptive duty-cycle correction.
[X: 39 ps/div, Y: 200 mV/div].

We also measure the histograms with each of 8-EQ coefficients and 16-DCC coefficients in the external-control mode. As show in Fig. 5-15, EQ coefficient 4 has the histogram having the largest peak value and DCC coefficient 14 has the smallest difference of peaks in histograms. The digital controller automatically selects these EQ and DCC coefficients for optimal ISI and duty-cycle distortion compensation.

Fig. 5-16 shows measured peak-to-peak jitter performance with and without duty-cycle correction for input data having different amounts of eye crossing levels. As can be seen, jitters are much reduced with duty-cycle correction. The maximum peak-to-peak jitter is 53.2 ps. Table 5-3 summarizes the performance of our EQ-DCC along with that of prior works for single-ended interface.

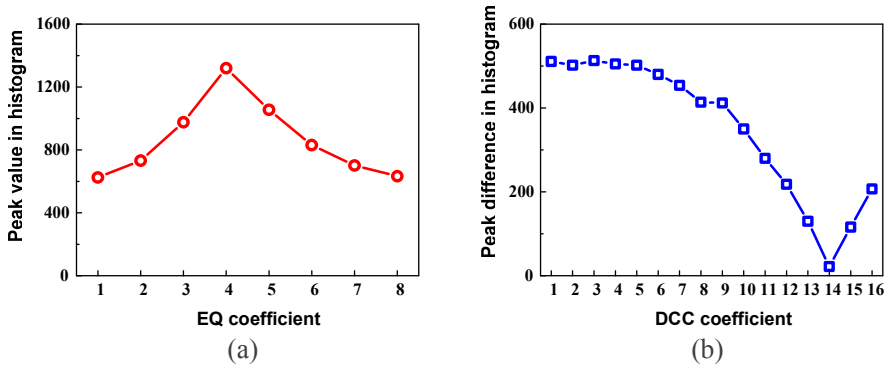


Fig. 5-15. Measured (a) peak value in histograms for EQ coefficients and (b) peak difference in histograms for DCC coefficients.

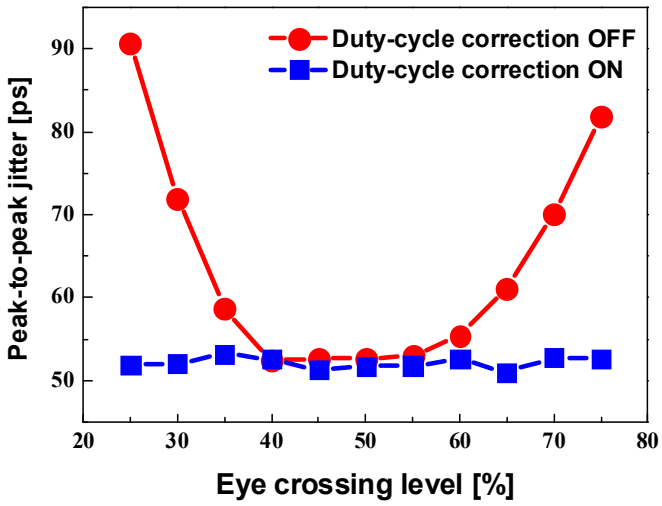


Fig. 5-16. Jitter performance with and without duty-cycle correction.

Table 5-3

Performance comparison of the proposed single-ended EQ-DCC.

	[36]	[37]	[38]	[39]	**This work**
Technology	CMOS 0.25 μm	CMOS 0.25 μm	CMOS 0.18 μm	CMOS 0.35 μm	**CMOS 0.13 μm**
Filter type	DFE	FFE	DCC	DCC	**CTLE+DCC**
Adaptation	N/A	Preamble pattern	N/A	N/A	**Asynch. histogram**
Data rate	2 Gbit/s	3 Gbit/s	0.8 ~ 1.2 GHz	70 ~ 500 MHz	**5 Gbit/s**
BER	$< 10^{-12}$	$< 10^{-12}$	N/A	N/A	**$< 10^{-13}$**
Boosting gain	3.17 dB at 1 GHz	N/A	N/A	N/A	**10.9 dB at 2.5 GHz**
Duty cycle	N/A	N/A	40 ~ 60 %	5 ~ 95 %	**25 ~ 75 %**
Chip area	0.0264 mm^2	0.0687 mm^2	0.23 mm^2	0.275 mm^2	**0.204 mm^2**
Power consumption	10 mW	37 mW	15 mW	23.1 mW	**25mW (9.23 mW* / 2.3 mW**)**

*: CTLE filter

**: DCC

A novel adaptive single-ended EQ-DCC based on asynchronously under-sampled histograms are demonstrated. Our EQ-DCC is capable of compensating ISI and DCD due to limited channel bandwidth and transmitter asymmetry. The prototype chip fabricated in 0.13-μm CMOS technology can successfully compensate 5-Gbit/s data having 25~75 % eye crossing levels transmitted through 80-cm PCB trace. Our adaptation technique is simple and robust without the need for clock synchronization, resulting in reduced power consumption and chip area.

5-3. PVT Tolerant Fast Adaptive Equalizer

As the technology scaling improves with smaller dimensions, smaller number of doping atoms and aggressive lithographic techniques, accurate control of the manufacturing process is deteriorating. It becomes a process variation which causes uncertainty in electrical characteristics of circuits and interconnects. The variation of device electrical parameters such as threshold voltage, transistor length and width, oxide thickness, and doping density can make the operating current of the circuits different form its nominal value which consequently affect the reliability of the system [42].

The impact of mounting currents to the enormous number of active circuits on a chip, and the effect of parasitics on package and on-chip power supply wires, leads to runtime supply voltage variations. Increasing operating frequencies and power densities in high performance integrated circuits leads to an increase in voltage drops in the power delivery network. For instance, a voltage drop of 18% of the nominal voltage has been reported in POWER6^{TM} dual-core processor fabricated in 65nm SOI process [43]. Similarly, temperature variation increases owing to the distributed circumstance of integrated circuits, and some components consume more power than others. In the silicon

substrate, heat generated at one part spreads and causes an increase in temperature at nearby parts. Runtime temperature variations also occur with time, as the subsystems switch between idle and active periods. Supply voltage and temperature variations cause fluctuation in device's operating current which make the system performance worse. Therefore, the PVT variation compensation technique is necessary at the system, architecture and circuit level for providing the optimal performance [44].

Previously reported adaptation scheme based on asynchronously under-sampled histograms [29] can be applied for process variation. It is based on the simple observation that the clearest eye diagram produces the largest peak value in histograms, and is ensuring tolerance to process variation and reliable communication by making the link adaptive to the effects of process variations. However it is unable to deal with the runtime supply voltage and temperature variations because it is a one-time adaptive equalization. Moreover it has drawback that the adaptation time is about scores of milliseconds which cannot satisfy the link training time of standard specifications, for example, 10 ms in DisplayPort 1.2 [45] or 1 ms in USB 3.0 [46].

In this chapter, we propose our improved histogram algorithm can adapt to a new environment by PVT variations with continuous-time

peak value monitoring. It also reduces the adaptation time under millisecond with peak position detection. We realize 10-Gbit/s adaptive CTLE in 0.13-μm CMOS technology and demonstrate the circuit can adaptively provide optimal data transmission characteristics through 40-cm FR4 PCB traces for 1.0-V to 1.5-V supply voltage variations.

Fig. 5-17 shows the block diagram of proposed PVT tolerant fast adaptive CTLE circuit. It consists of a 3-bit variable CTLE filter, a four-phase clock divider, two UGBs, two DACs, four track-and-hold circuits, a four-input differentially clocked sense amplifier, and an integrated digital controller. The CTLE filter is optimized by the comparison of the peak value of histogram with 4096 samples and 19.35-mV DAC resolution. The 5-bit DAC generates reference voltages from 600mV to 1.2V. The histogram sample size is determined by 99% confidence interval and 1.75% margin of error [29]. The digital controller contains peak position detection logic for reducing adaptation time and continuous-time peak value monitoring logic for continuous-time adaptive calibration.

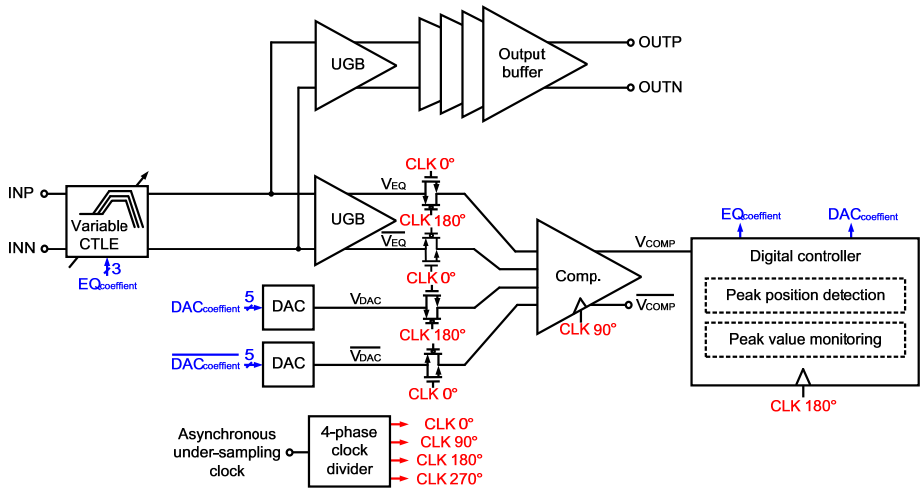


Fig. 5-17. Block diagram of PVT tolerant fast adaptive CTLE.

The 40-cm PCB trace shows the 10.48-dB loss at 5 GHz as shown in Fig. 5-1. The 10-Gbit/s CTLE filter is generated 10.5-dB equalizing gain for compensating frequency dependent channel loss. A CTLE filter is designed in a differential structure with capacitive degeneration and negative capacitance [11], [13] as shown in Fig. 5-18. The 2-stage filter is used for our design specification. With the filter, adaptation is achieved by tuning the zero of negative capacitor. The transfer function of the filter can be derived as:

$$H(s) \cong \frac{g_m}{1+\frac{g_m R_S}{2}} \cdot \frac{1+\frac{s}{\omega_{z1}}}{1+\frac{s}{\omega_{p1}}} \cdot R_L \cdot \frac{1+\frac{s}{\omega_{z2}}}{1+\frac{\varsigma s}{\omega_n}+\frac{s^2}{\omega_n^2}} \tag{5.2}$$

$$\begin{aligned} &\omega_{z1} = 1/(R_S C_S),\ \omega_{p1} = (1+g_m R_S/2)/(R_S C_S),\ \omega_{p2} = 1/(R_L C_L), \\ &\omega_{z2} = 1/(R_{NC} C_C),\ \varsigma = \omega_n (R_L C_L + R_{NC} C_C - R_L C_C), \\ &\omega_n = 1/\sqrt{R_L C_L R_{NC} C_C},\ R_{NC} = (C_{gsNC}/C_C + 2)/g_{mNC} \end{aligned} \tag{5.3}$$

where ω_{z1} and ω_{z2} represent the zeros, ω_{p1} and ω_{p2} represent the ploes, g_m is the transconductance of $M_{1,2,}$ and g_{mNC} is the transconductance of $M_{3,4}$. ω_n is the center frequency of the filter peaking, and R_{NC} is the resistance of negative capacitance circuit. Tunable zeros for equalization are generated by C_S and R_S of source degeneration and C_C and R_{NC} of the negative capacitance. The zero location is adjusted by C_C which is digitally controlled by 3-bit equalization coefficients for 8-different levels having 1.5-dB equalizing gain resolution.

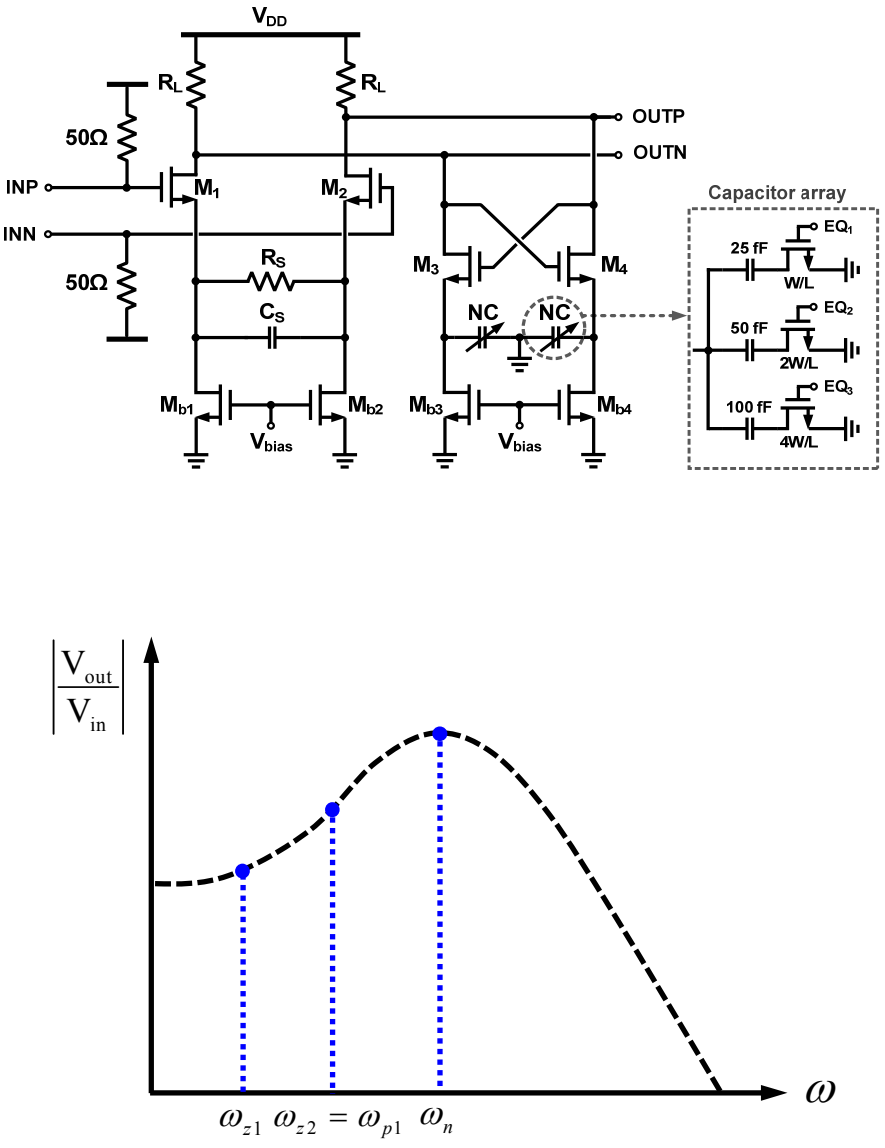
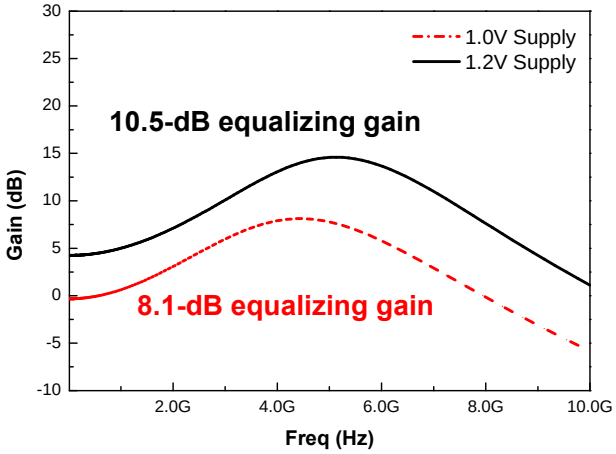


Fig. 5-18. Schematic diagrams of tunable CTLE filter and corresponding frequency response.

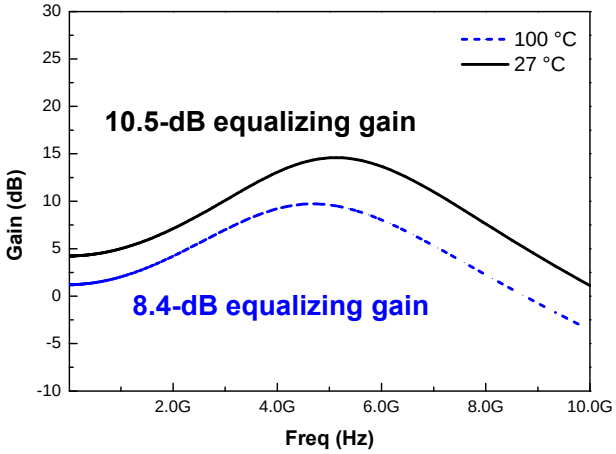
For proper histogram calculation, the equalizing filter maintains the low-frequency swing despite changing equalization coefficient. Similarly, histograms show the identical height until the over equalization. In previously demonstrated version, the 32-level DAC reference voltages are fully scanned at every equalization coefficient. On the other hand, peak position detection logic of the proposed adaptive CTLE initially sets the DAC coefficient representing the edge of histogram, and the peak of the histogram can be founded with detected DAC coefficient. Therefore, the total adaptation time can be reduced to 1/16 by peak position detection logic with starting the under equalization coefficient.

After adaptive equalization, when the environmental variations in the supply voltage and temperature occur, the operating conditions of the circuit are influenced. The equalizing gain of the CTLE filter is set to 10.5 dB from 1.2-V supply voltage at room temperature for channel loss compensation. As the supply voltage drops to 1.0 V, the saturation current of the equalizing filter decreases which reduces the transconductance. Therefore, the center frequency, ω_n, is moved down, and the equalizing gain is attenuated. As can be seen in Fig. 5-19(a), the g_{mNC} reduced to 1.04 mA/V (18 % reduction), thus the equalizing gain becomes 8.1 dB. Similarly, when the temperature rises to 100 °C, the

g_{mNC} reduces to 1.13 mA/V (11 % reduction) and the equalizing gain is 8.4 dB as shown in Fig. 5-19(b).



(a)



(b)

Fig. 5-19. Equalizing gain attenuation by (a) supply voltage variation and (b) temperature variation.

Signal quality monitoring is an important task of any adaptive system for compensating PVT variations. The peak value monitoring logic in digital controller monitors the peak value status of the histogram which represents the runtime operating conditions of the circuit. The peak value is regularly monitored with 177MHz asynchronous sampling clock and 4096 samples. When peak value becomes less than 512 which represents the minimum sample size for 80 % confidence interval according to Eq. (2.3), the digital controller starts continuous-time adaptive calibration as shown in Table 5-4. By comparing peaks of present equalization coefficient and near equalization coefficients, the optimal equalization condition can be compensated. The 512 samples prevent local maximum point for stable calibration process.

Table 5-4

Continuous-time adaptive calibration process.

Peak comparison	Equalization coefficient setting
$Peak_{EQ-1} < Peak_{EQ} < Peak_{EQ+1}$	$EQ_{coefficient} = EQ_{coefficient} + 1$
$Peak_{EQ-1} > Peak_{EQ} > Peak_{EQ+1}$	$EQ_{coefficient} = EQ_{coefficient} - 1$
$Peak_{EQ-1} < Peak_{EQ} > Peak_{EQ+1}$	Set optimal $EQ_{coefficient}$

The PVT tolerant fast adaptive CTLE is performed as shown in Fig. 5-20. Initially, a finite state machine initializes the equalization coefficient and DAC coefficient for under equalization condition. The DAC coefficient increased until the edge of the histogram. We set the more than 50 samples to distinguish the edge of the histogram for sampling margin. After that, The DAC coefficient is fixed by peak position detection logic. When the data level is higher than DAC reference voltage at the sampling point, counter counts up by one and register stores the accumulated value. With repetition of this process which is the just comparison of the peak value in histogram for each 3-bit 8-level equalization coefficient and 4096 samples, the digital controller choses the histogram having the largest peak value as the optimal equalization coefficient. After adaptive equalization, peak value monitoring logic regularly monitors the peak values of histograms for continuous-time adaptive calibration. All processes are synchronized with 177-MHz asynchronous under-sampling clock from external clock source and total adaptation time decrease to about 505 μs.

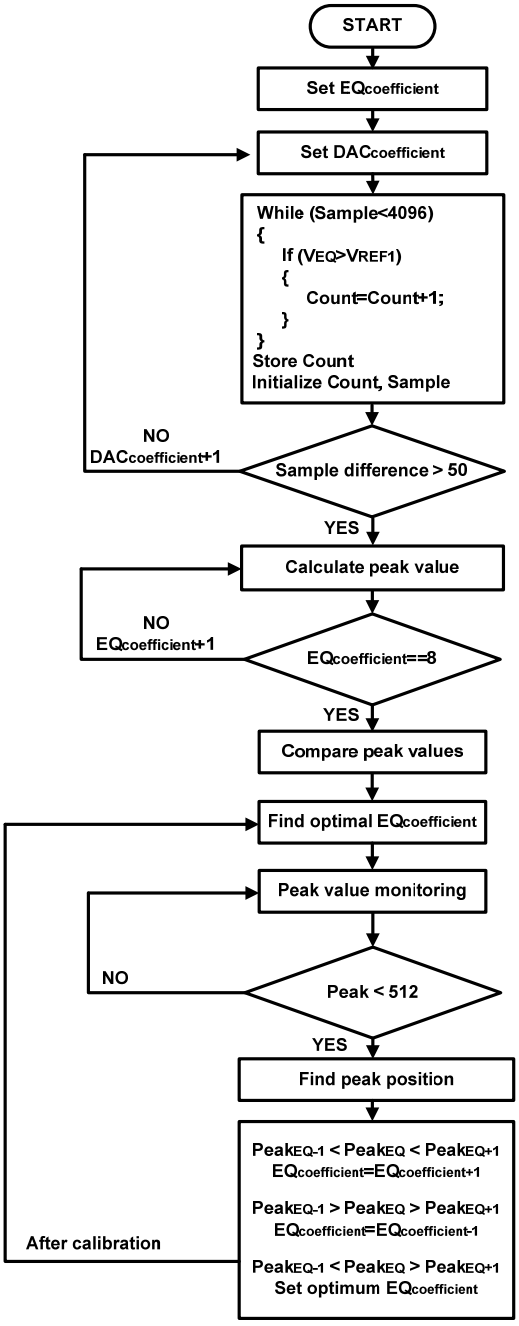


Fig. 5-20. Flow chart of PVT tolerant fast adaptive equalization process.

Conventional power supply used decoupling capacitors for mitigating power supply variations. In our case, 20μF decoupling capacitor is applied for power supply variation reduction. However, supply voltage variation cannot be exhaustively prevented. In order to verify the effects of supply voltage variations, power supply gain which is transfer function form the power node to the output node is presented [47]. Fig. 5-21 shows the simulation setup and power supply gain. It presents the 450 Hz 3-dB bandwidth for power supply rejection. Therefore, low-speed supply voltage variations should be calibrated to maximize the operating circuit performance.

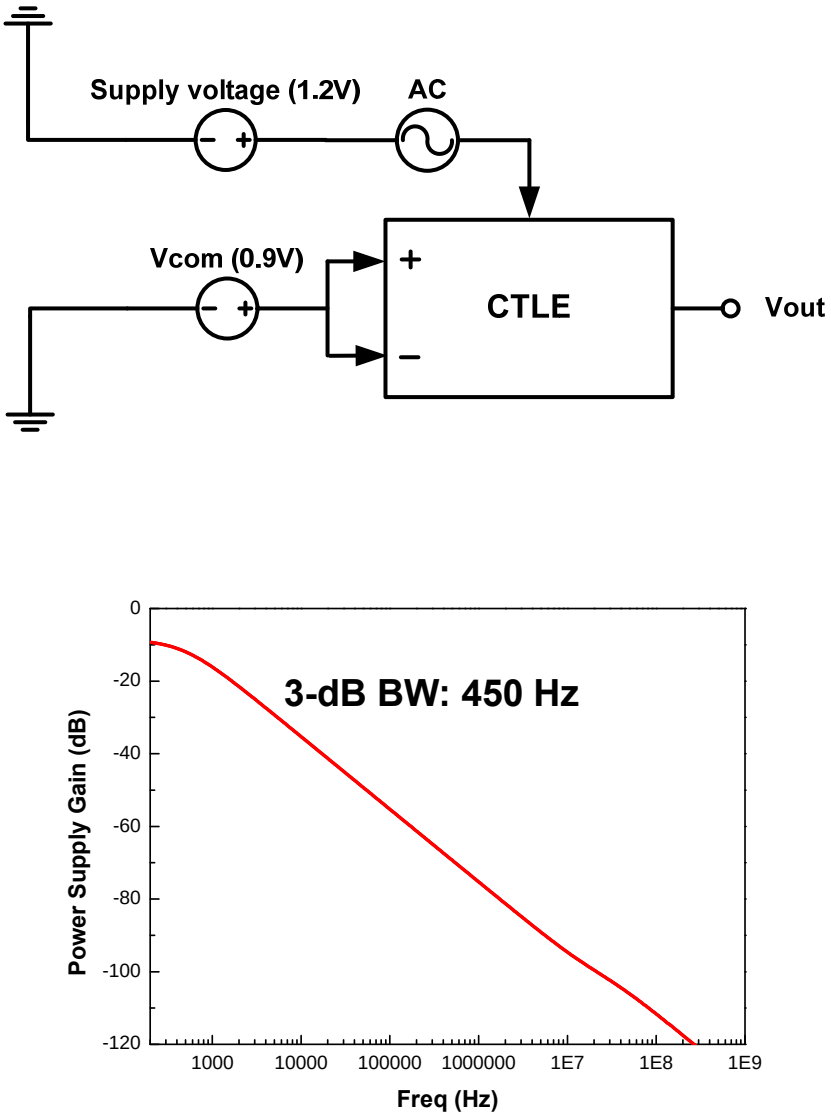


Fig. 5-21. Simulation setup and power supply gain.

The peak value monitoring logic compares with peaks of histograms with 4096 samples and 177 MHz asynchronous under-sampling clock for continuous-time adaptive calibration. The total calibration time required for resetting the optimal filter coefficient can be estimated as:

$$
\begin{aligned}
&4096\ \text{(sample number)} \\
&\times 8\ \text{(reference voltage for edge detection)} \\
&\times 5.6\ ns\ \text{(time for each operation)} \\
&+ \\
&4096\ \text{(sample number)} \\
&\times 2\ \text{(reference voltage for peak calculation)} \\
&\times 3\ \text{(3-point peak comparison)} \\
&\times 3\ \text{(worst case detection)} \\
&\times 5.6\ ns\ \text{(time for each operation)} \cong 596\ \mu s \cong \frac{1}{1.6\ KHz}
\end{aligned}
\tag{5.4}
$$

It takes under millisecond time in worst case situation which means the continuous-time adaptive calibration is easily able to compensate the under 450 Hz supply voltage variations by 1.6 KHz operating speed.

Fig. 5-22 is a micro-photograph of fabricated chip in standard 0.13-μm CMOS technology. The power consumption is 20.4 mW from 1.2-V supply voltage, and the core area occupies 0.09-mm^2.

Fig. 5-23 shows the measurement setup. A PPG provides differential 10-Gbit/s PRBS 2^{31}-1 data is transmitted to the adaptive CTLE through 40-cm PCB traces. A frequency synthesizer provides 354-MHz asynchronous under-sampling clock. The equalized data are observed with an oscilloscope and a BER tester. The integrated digital controller can be operated in internal- or external-control mode. With internal control mode, the optimal equalization coefficient is automatically determined by the integrated digital controller. With external control mode, equalization coefficients can be externally controlled by FPGA for the testing purpose. In addition, a computer controls the power supply to generate the variable supply voltage and trigger, and the equalization coefficients are observed by real-time oscilloscope for continuous-time adaptive calibration monitoring.

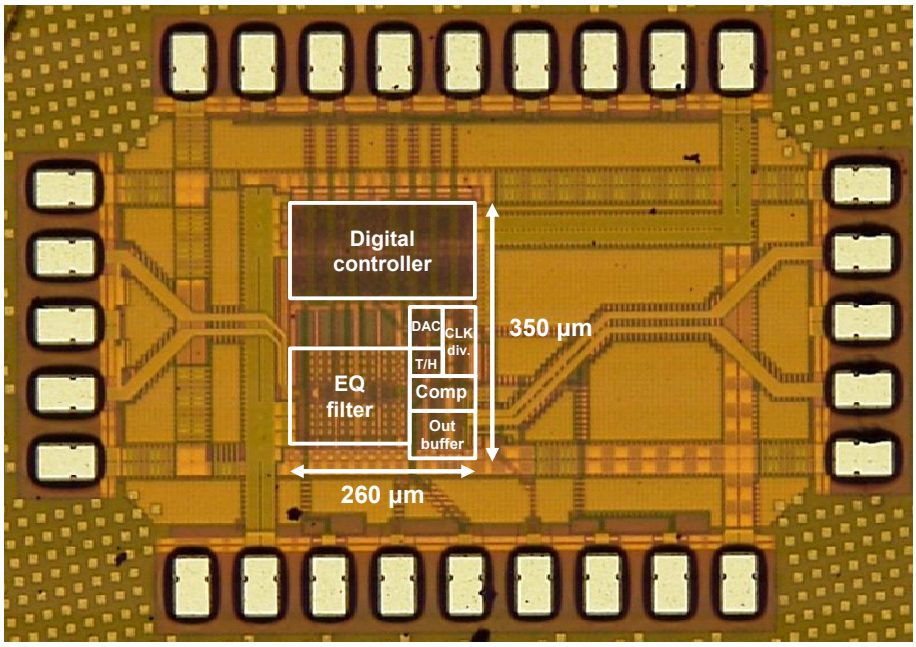


Fig. 5-22. Chip photograph of the PVT tolerant fast adaptive equalizer.

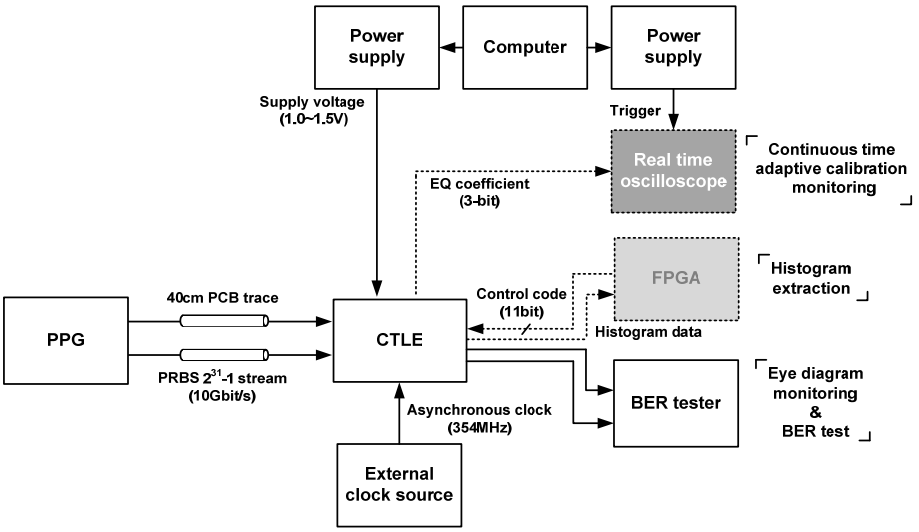
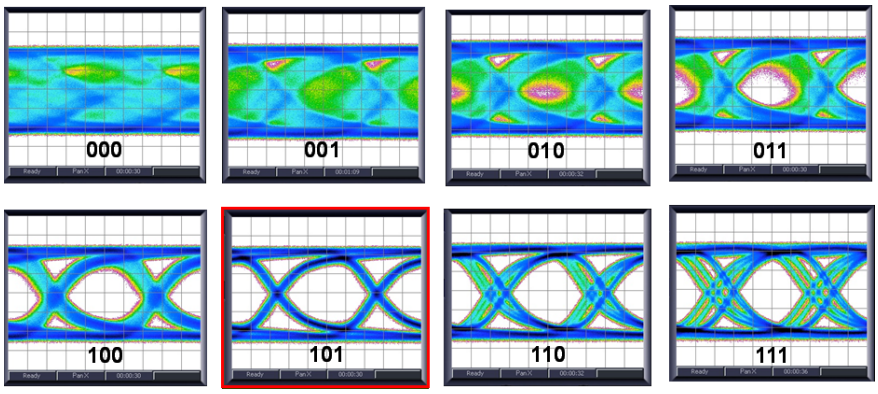
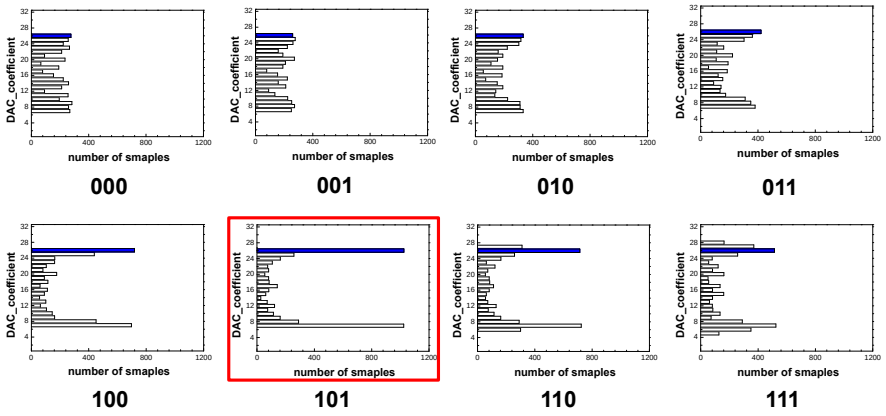


Fig. 5-23. Measurement setup.

Fig. 5-24 shows eye diagrams and histograms measured in the external-control for 10-Gbit/s data transmission through 40-cm PCB traces for various equalization coefficients. As can be seen, equalization coefficient 101 can be easily identified as the one producing the clearest eye diagram and histogram having the largest peak value.



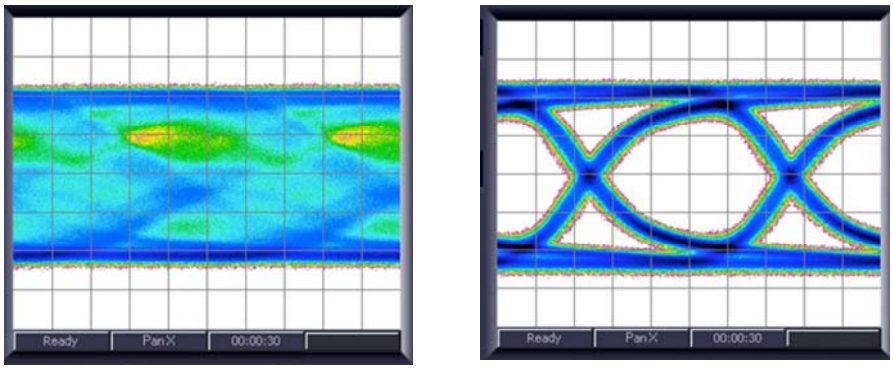
(a)



(b)

Fig. 5-24. Measured (a) eye diagrams and (b) histograms of each equalization coefficient for 40-cm PCB traces.

Fig. 5-25 shows measured eye diagrams and histograms before and after equalization for 40-cm PCB trace with 10-Gbit/s 2^{31} – 1 PRBS data. The optimal equalization coefficient is adaptively selected by the integrated digital controller without any external control. As can be seen, all eyes are clearly open after equalization by searching the histogram having the largest peak value. The measurement result shows error-free during 15 minutes after equalization and the measured peak-to-peak jitters are 18.9 ps.



(a) (b)

Fig. 5-25. Eye diagrams of (a) before and (b) after equalization.
[(a) X: 19 ps/div, Y : 162 mV/div; (b) X: 19 ps/div, Y :162 mV/div].

Fig. 5-26 shows measured peak-to-peak jitter performance before and after adaptive calibration for variable supply voltage level. As can be seen, jitters are much reduced with adaptive calibration. When the supply voltage reaches about 1.07 V, the peak value monitoring logic finds the peak value less than 512, simultaneously the continuous-time adaptive calibration is operated. The inset of Fig. 5-26 also shows the measured 10-Gb/s eye diagram before and after adaptive calibration at 1.0 V supply voltage. The maximum peak-to-peak jitter reduces from 34.9 ps before calibration to 21.6 ps after calibration.

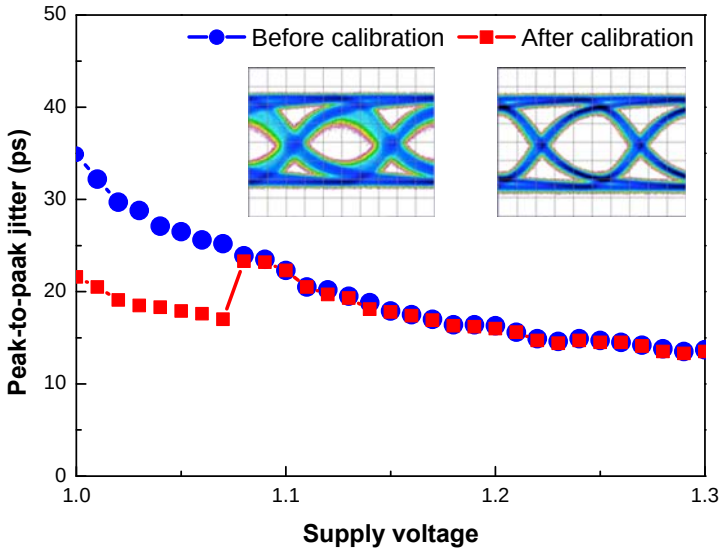


Fig. 5-26. Jitter performance before and after adaptive calibration.

Fig. 5-27 shows measured equalization coefficient during continuous-time adaptive calibration. For this measurement, we control the supply voltage from 1.5 V to 1.0 V. As can be seen in the figure, equalization coefficient automatically changes from 101 to 110 at about 1.07 V supply voltage. Therefore, continuous-time adaptive calibration successfully provides the optimal equalization condition with respect to supply voltage variation.

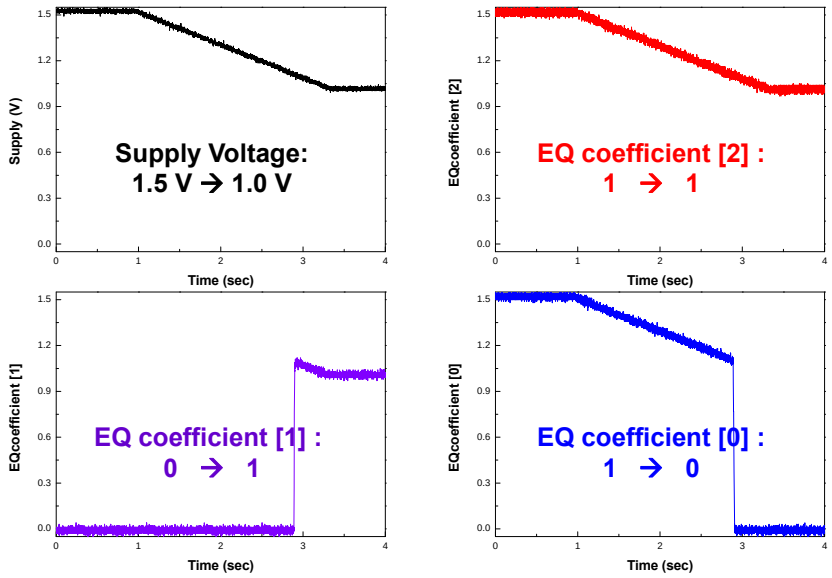


Fig. 5-27. Equalization coefficients during continuous-time adaptive calibration.

In summary, a PVT tolerant fast adaptive CTLE are presented. The technique for process variation tolerance is based on detecting the largest peak value in histograms and performing adaptive equalization at power start-up of the system. During adaptive equalization process, peak position detection logic can reduce the total adaptation time to less than millisecond. After adaptive equalization, peak value monitoring logic regularly monitors the peak values in histograms. If an error is detected, continuous-time adaptive calibration will be operated. This makes the CTLE adaptive to the effect of VT variation, therefore enabling its continuous and reliable CTLE operation. Table 5-5 compares the performance of the proposed adaptive CTLE with previously reported adaptive CTLE fabricated in same CMOS technologies.

Table 5-5

Performance comparison of the PVT tolerant fast adaptive CTLE.

	[29]	**This work**
Technology	CMOS 0.13 μm	**CMOS 0.13 μm**
Data rate	5.4 Gbit/s	**10 Gbit/s**
BER	$< 10^{-13}$	**$< 10^{-13}$**
Compensation	Process variation	**PVT variation**
Boosting gain	15.7 dB at 2.7 GHz	**10.5 dB at 5 GHz**
Power consumption	35 mW	**20.4 mW**
Chip area	0.18 mm^2	**0.09 mm^2**
Adaptation time	18 ms	**505 μs**
Figure of Merit (pJ/bit/dB)	0.413	**0.194**

6. Conclusion

In this dissertation, we propose adaptive equalization based on asynchronously under-sampled histograms for high-speed wireline links. The main motivation for asynchronous under-sampling is the absence of clock recovery which makes it less expensive than synchronous sampling and enables it to work at a wide variety of bit rates. In addition, it presents the stable operation by low-speed asynchronous under-sampling clock, thus pilot sequence does not required. This is a clear advantage in simple and robust architecture for the adaptive equalization.

As the first verification, we implemented a 5.4-Gbit/s adaptive CTLE in 0.13-μm CMOS technology. It analyzed for design specification such as sample size, sampling clock, and BER estimation. It successfully demonstrated 5.4-Gbit/s data transmission through 40-, 80-, and 120-cm PCB traces and 3-m DisplayPort cable. In addition, we verify our adaptive CTLE can be easily extended to various applications while maintaining its advantages of small power consumption and chip size.

A 10-Gb/s low-power adaptive CTLE is realized in 65-nm CMOS technology. To reduce the power consumption, the integrated digital controller turns off the circuit blocks used for the adaptation process

once adaptation is complete. A prototype equalizer realized in 65-nm CMOS technology consumes 4.66 mW during adaptation and 2.49 mW after adaptation.

A 5-Gbit/s adaptive EQ-DCC for single-ended high-speed interface applications is presented in 0.13-μm CMOS technology. The monitoring scheme based on asynchronously under-sampled histograms can provide DCD and ISI information with simple and robust implementation. In addition, low-speed asynchronous under-sampling causes less voltage spikes and EMIs. It can compensate 10.9-dB channel loss at 2.5 GHz and 25~75 % duty-cycle distortion.

Finally, a 10-Gbit/s fast adaptive CTLE for compensating PVT variations is implemented in 0.13-μm CMOS technology. The improved digital controller can reduce the total adaptation time by peak position detection and compensate the run time VT variations by continuous-time peak value monitoring. It demonstrated 10-Gbit/s data transmission through 40-cm FR4 PCB traces for 1.0-V to 1.5-V supply voltage variations.

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Abstract (In Korean)

비동기식 저속 샘플링 히스토그램을 이용한 적응형 등화 방법

고속 시리얼 인터페이스에서 채널의 주파수 의존 소실은 시간 축에서 심볼 간 간섭으로 나타나게 되고 이에 따라 비트 에러율이 높아지는 문제로 나타나게 된다. 이를 해결하기 위해 주파수 부스팅 필터를 통해 Nyquest 주파수 범위까지 평탄한 주파수 응답을 얻어주기 위한 여러 등화 기법이 필요하게 된다. 등화기를 설계하기 위해 목표가 되는 채널의 정확한 특성을 알아야 하지만 실제 회로는 공정·온도·전압 변화의 영향으로 인해 정확한 채널의 특성을 예측할 수 없다. 따라서, 여러 환경에 적용 가능한 적응형 등화기가 많은 응용에서 선호 되고 있다.

본 논문에서는 표준 0.13-μm CMOS 공정을 이용하여 비동기식 저속 샘플링 히스토그램을 이용한 새로운 방법의 적응형 등화기를 구현하였다. 제안하는 연속 시간 선형 등화기는 비동기식 저속 샘플링을 통해 얻어진 히스토그램을 분석하여 가장 큰 첨점을 지니는 히스토그램을 나타내는 등화 계수로 설정해줌으로써 심볼 간 간섭 문제를 해결해줄 수 있게 된다. 이러한 등화방법은 저속의 비동기

클럭을 사용함으로써 클럭 복원 회로 및 이를 적용하는 알고리즘이 제거할 수 있어 간단한 구현과 강건한 동작을 보장할 수 있다.

제작된 프로토 타입 칩은 40-, 80-, and 120-cm PCB trace 및 3-m 디스플레이포트 케이블에 대하여 5.4-Gbit/s $2^{31} - 1$ 의사 랜덤 이진열 데이터 전송을 성공적으로 완수하였다. 측정된 peak-to-peak 지터는 각 33.62, 34.81, 36.41, 및 34.73 ps 이다. 칩 면적은 0.18 mm^2 이며, 전력 소모는 1.2 V 전원에서 약 35 mW 이다. 또한, 통계적인 분석을 통해 얻어진 히스토그램 샘플 수에 대한 신뢰도를 실험을 통해 검증하였다. 그 결과 이론 값과 실제 측정 값이 일치됨을 확인 하였다.

본 논문에서 제안하는 히스토그램 알고리즘은 여러 응용 분야에 확장 할 수 있다. 먼저, 저전력 적응형 등화기를 표준 65-nm CMOS 공정을 이용해 구현하였으며, 등화 중 4.66 mW, 등화 후 2.49 mW의 전력 소모를 확인할 수 있었다. 제작된 칩으로 10-Gbit/s 데이터를 40-cm FR4 PCB trace를 통해 전송 성공하였으며, 15분 데이터 전송 간 에러가 없는 결과 및 26.6 ps peak-to-peak 지터 성능을 확인할 수 있었다. 다음으로 표준 0.13-μm CMOS 공정을 이용하여 single-ended용 적응형 등화기 및 듀티 사이클 보정기를 구현하였다. 제작된 칩으로 5-Gbit/s 데이터를 80-cm FR4 PCB trace 및 25 ~ 75 % 듀티 사이클 왜곡을 극복하여 전송하였으며, 30분 데이터 전송 간 에러가 없는 결과 및 53.2 ps peak-to-peak 지터 성능을 얻을 수 있었다.

마지막으로 공정·온도·전압 변화에 둔감한 빠른 적응형 등화기를 표준 0.13-μm CMOS 공정을 이용하여 구현하여 40-cm FR4 PCB trace를 대상으로 10-Gbit/s 데이터 전송을 성공하였다. 이 칩을 통해 1.0 V 에서 1.5 V 전원에 대해서 15분 데이터 전송 간 에러가 없는 결과 및 21.6 ps peak-to-peak 지터 성능을 얻을 수 있었다.

핵심 단어: 심볼 간 간섭, 적응형 등화기, 비동기식 저속 샘플링 히스토그램, 비트 에러율, CMOS 표준 공정, 연속 시간 선형 등화기, 듀티 사이클 보정기, 저전력 설계, 공정·온도·전압 변화

List of Publications

International Journal Papers

[1] **Wang-Soo Kim**, Chang-kyung Seong, and Woo-Young Choi, "A 5.4-Gbit/s adaptive continuous-time linear equalizer using asynchronous undersampling histograms," *IEEE Trans. Circuits Syst. II*, vol. 59, no. 9, pp. 553–557, Sep. 2012.

[2] **Wang-Soo Kim**, and Woo-Young Choi, "A 10-Gb/s low-power adaptive continuous-time linear equalizer using asynchronous under-sampling histogram", *IEICE Electron. Express*, vol. 10, no. 4, pp. 1–8, Feb. 2013.

International Conference Presentations

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