Bandwidth and SNR Optimization of Integrated Si Optical Receivers

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Bandwidth and SNR Optimization of Integrated Si Optical Receivers

by

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Abstract

Bandwidth and SNR Optimization of Integrated Si Optical Receivers

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High-speed and design optimized Si based optical receivers are investigated and realized for monolithic and hybrid integration. The realized optical receivers are design-optimized with accurate circuit model of photodetector as well as wire-bonding inductance for hybrid integration. The design optimization can achieve not only better performances but also enhanced bandwidth with speed-limited

photodetector. To obtain accurate circuit model of the integrated photodetectors, DC and photodetection frequency response are investigated and applied to accurate circuit model. Also, wire-bonding inductance is verified with measurement and simulation results.

A design-optimized hybrid-integrated optical receiver circuit is presented. The receiver circuits are designed with consideration for parasitic inductance and capacitance due to bonding wires connecting the photodetector and the circuit realized separately. The receiver circuit is composed of a transimpedance amplifier (TIA) with DC-balancing buffer, a post amplifier (PA), and an output buffer (OB). The receiver circuit is verified with photodetector equivalent circuit. The measured transimpedance gain and 3-dB bandwidth is 84 dBΩ and 12 GHz, respectively. 20-Gb/s $2^{31}-1$ electrical pseudo-random bit sequence (PRBS) data are successfully received with bit-error rate (BER) less than 10^{-12}. The chip area is 0.5 mm × 0.44 mm and power consumption excluding the output buffer is 84 mW with 1.2-V supply voltage.

CMOS integrated optical receiver having under-damped TIA and CMOS avalanche photodetector (APD) realized in 65-nm CMOS technology. The under-damped TIA compensates the bandwidth limitation of CMOS APD and provides enhanced receiver bandwidth

performance with reduced power consumption and better sensitivity compared with previously reported techniques. 10-Gb/s $2^{31}-1$ PRBS and 12.5-Gb/s $2^{7}-1$ PRBS operation with the BER less than 10^{-12} at the incident optical power of −6 and −2 dBm are successfully demonstrated, respectively. The realized optical receiver has core size of 0.24 mm × 0.1 mm and power consumption excluding output buffer of 13.7 mW with 1.2-V supply voltage.

A high-performance integrated optical receiver is realized in photonic BiCMOS technology. The optical receiver includes waveguide type Ge photodetector (Ge PD), TIA, single-to-differential converter (SDC), PA and OB. All of which are monolithically implemented on a Si wafer. It achieves BER of 10^{-12} for 25-Gb/s $2^{31}-1$ PRBS at the incident optical power of −10 dBm with energy efficiency of 1.5 pJ/bit. In addition, with the accurate Ge-PD circuit model, the simulated optical receiver eye diagrams and BER performances accurately predict the measured results.

With accurate circuit model and understanding of photodetectors and connecting with them, monolithic- and hybrid-integrated optical receiver can achieve design optimization. It is expected that these design techniques can be a promising solution for realization of the design-optimized optical receiver.

Keywords**:** Avalanche photodetectors (APDs), bit-error rate (BER), equivalent circuit model, hybrid integration, limiting amplifier, monolithic integration, optical interconnect, optical receiver, optoelectronic, photodetector, frequency response, post amplifier, power efficiency, Si photonics, signal-to-noise ratio (SNR), transimpedance amplifier (TIA), wire-bonding inductance.

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1. Introduction

1.1. Optical Interconnect

There are various interface applications for interconnect as different distance from thousands of kilometers to less than millimeter. Fig. 1-1 shows trends in high-speed optical and electrical interconnects for different distances. As shown in the figure, optical interconnect and electrical interconnect has been mainly used for long distance interconnection such as telecommunications, metro and long haul, and short distance interconnection such as board-to-board and chip-to-chip interconnect, respectively [1, 2].

Recently, with big data explosions and bandwidth requirement increases, the existing electrical interconnects face severe performance problem with interconnect distance limitation as well as limited bandwidth, electro-magnetic interferences, and high attenuation [3]-[7]. To overcome these problems, optical interconnect is receiving a great amount of research and development efforts [8, 9]. As shown in Fig. 1-1, the boundary between optical and electrical interconnect applications is moving from left to right [10].

There are requirements to replace electronic interconnect with

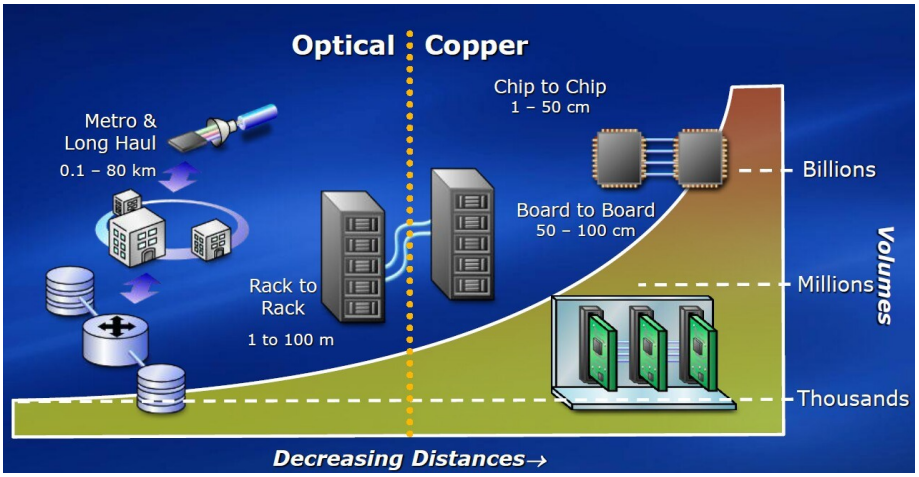


Fig. 1-1. Trends in high-speed optical and electrical interconnects [10].

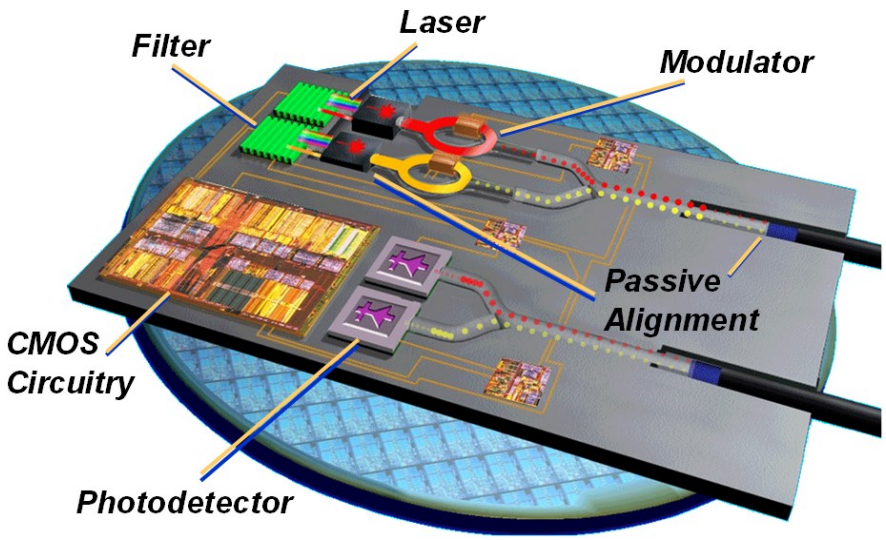


Fig. 1-2. Conceptual block diagram of silicon photonics [11].

optical interconnect. The optical devices and electronic circuits should be cost effective, easy to integrated and compatible with existing electronic circuits. And optical interconnect with 1.3- and 1.5-μm light having low loss in fiber is usually used for long distance interconnect as well as rack-to-rack and board-to-board interconnect for data center [12]-[14]. Moreover, as silicon photonics which makes photonic device on Si platform possible is developed, the optical interconnect has become the center of interconnect interest. The Fig. 1-2 shows the conceptual block diagram of silicon photonics. In addition, there is also 850-nm optical interconnect based on vertical-cavity surface-emitting lasers (VCSELs). It can be cost effective with cheaper laser and multimode fibers (MMFs) [15]. Also, CMOS photodetectors (PDs) can be used in 850-nm optical interconnect, which can be fabricated in existing Si technology such as complementary metal-oxide-semiconductor (CMOS) or bipolar CMOS (BiCMOS) technology and easily fully-integrated with electronic circuits [16]-[18].

Fig. 1-3 shows the block diagram of the optical interconnect systems. The optical transmitter consists of laser, modulator, and electronics circuits such as driver, serializer, phase-locked loop and pre-emphasis. The optical receiver includes PD and electronic circuits such as amplifiers, equalizer, de-serializer, and clock and data recovery.

Among the optical transmitters and receivers, the optical receiver front-end will be mainly discussed in this dissertation.

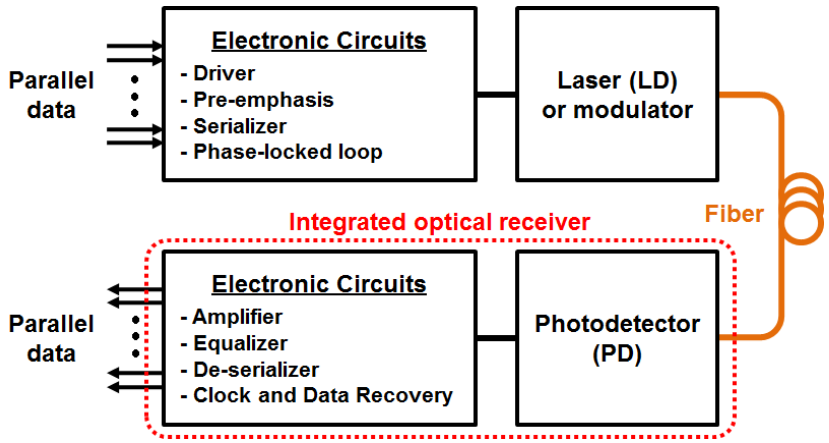


Fig. 1-3. Block diagram of the optical interconnects.

1.2. Optical Receiver System and Design Consideration

Fig. 1-4 shows block diagram of the general optical receiver system. PD transforms the light intensity to a proportional current and transimpedance amplifier (TIA) subsequently amplifies and converts from the current to the voltage. After that, the broadband amplifier such as a limiting amplifier or a post amplifier amplifies the voltage signal of the TIA output to satisfy required input voltage level of subsequent clock and data recovery or digital circuits.

Fig. 1-5 shows two types of the integrated optical receiver front-end, which are monolithically and hybrid-integrated optical receiver. Most integrated optical receivers for high-speed applications have been based on III-V semiconductors with hybrid integration. In this case, PDs and optical receiver circuits are designed and fabricated separately without optimized design as well as with parasitic pad capacitance and wire-bonding inductance [19]-[21]. However, recently, PDs can be fabricated in Si technology, PDs and electronic circuits can be integrated monolithically on a same chip.

For design optimization of the optical receiver, there are lots of efforts researches for circuit design with innovative configuration and structure [22] - [24]. However, TIA and other receiver blocks have been

recently designed with several fixed structure, and consideration of the integration with PDs is very essential to improve and optimize optical receiver design. First of all, equivalent circuit model of the PDs should be constructed. In the past, PDs have been considered as a capacitor from depletion region, but more optimized design can be possible with more accurate circuit model of the PDs. Also, in hybrid integration, pad capacitance and wire-bonding inductance should be considered to achieve proper optical receiver design.

In the next section, basic knowledge of PDs, TIA, and broadband amplifiers will be presented.

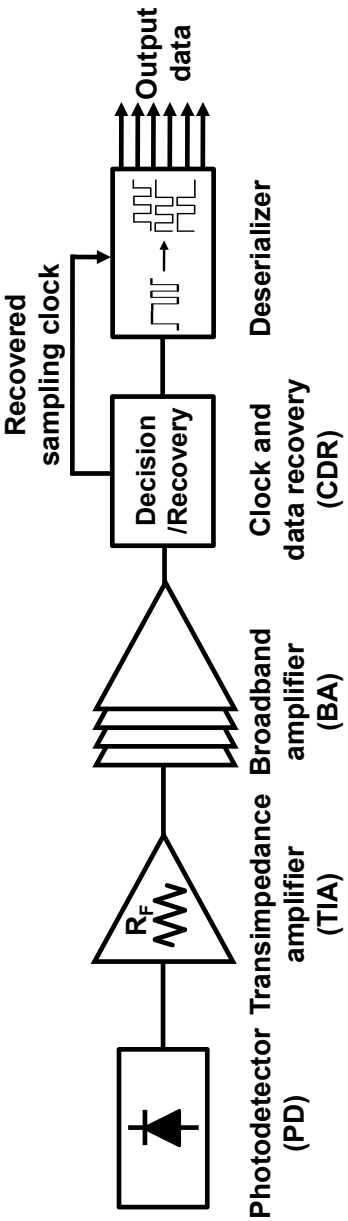


Fig. 1-4. Block diagram of the optical receiver system.

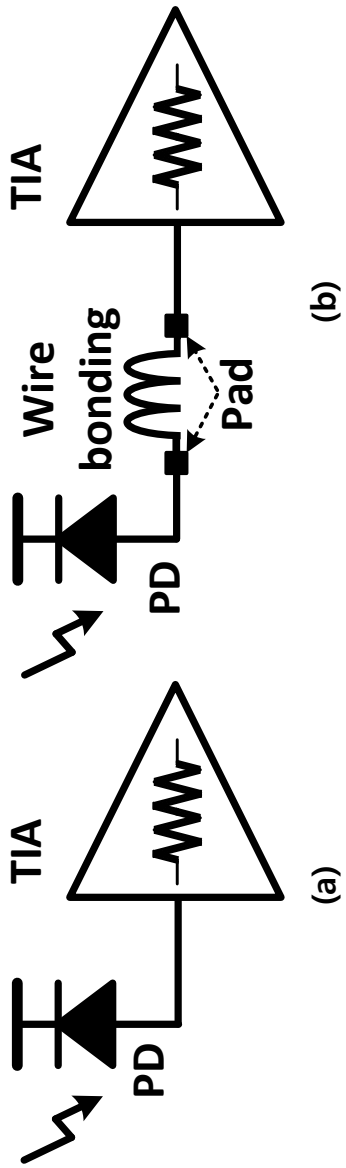


Fig. 1-5. Block diagram of the optical receiver front-end for (a) monolithic and (b) hybrid integration.

1.3. Optical Receiver System Blocks

1.3.1 Photodetector (PD)

PD having a PN junction converts the light carried by a fiber to the electrical signal, current, at the receiver front-end. If a PN junction is illuminated with light, the electrons in the valence band are raised to the conduction band as shown in Fig.1-6. As a result, a photon is absorbed and an electron-hole pair capable of conducting current is generated [25].

Various properties of PD affect absorbable light wavelength, sensitivity and speed of the receiver front end. As mentioned, accurate circuit model of the PD is necessary to design optical receiver. The Fig. 1-7 shows the equivalent circuit block of the PD [26, 27]. The 3-dB bandwidth of PD is determined as

$$f_{PD} = \frac{1}{\sqrt{\left(\frac{1}{f_{tr}}\right)^2 + \left(\frac{1}{f_{RC}}\right)^2}}. \quad (1.1)$$

f_{tr} represents 3-dB bandwidth of photogenerated carriers and it affects to an optical receiver as a lossy channel, and f_{RC} is from the passive elements with load impedance. For a long time, regardless of PD type, optical receiver designs have been done with considering PD circuit

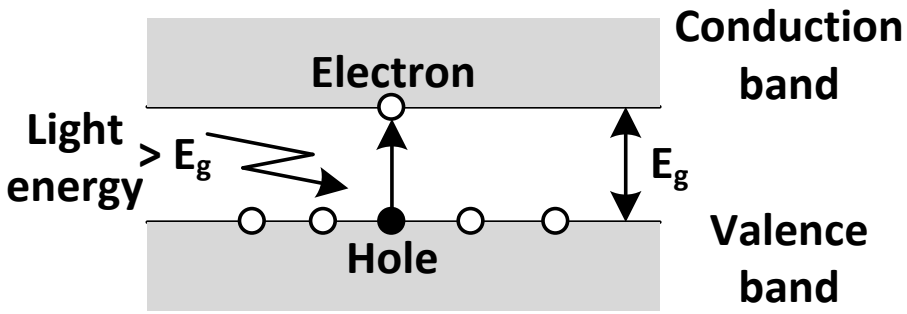


Fig. 1-6. Generation of an electron-hole pair by a photon [25].

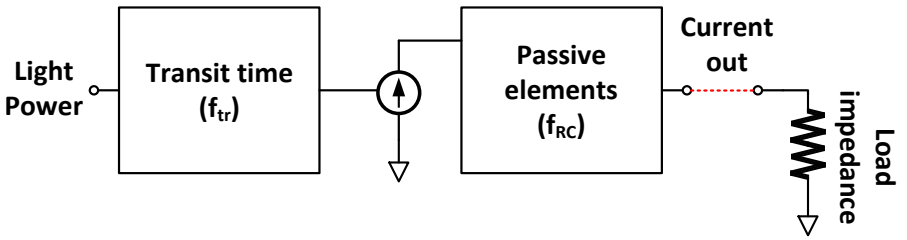


Fig. 1-7. Equivalent block diagram of the photodetector [26, 27].

model as a capacitor for PN junction, because transit time of PD is usually much faster than f_{RC}. Moreover the capacitance of PD is very large enough to mainly determine f_{PD} with f_{RC}. However, as the bandwidth of PD has been increased higher than tens of GHz with decreasing junction capacitance, f_{RC} has been reached to f_{tr} and other passive elements as series resistance has affected to the bandwidth [28]. Consequently, not only f_{tr} should be considered, but also other passive elements besides junction capacitance should be precisely extracted. Extracting the passive elements can be achieved by fitting with measurement and simulation results of the electrical reflection coefficient, and f_{tr} can be determined with fitting measurement and simulation results of the photo-detection frequency response [26, 27].

The accurate models of the PD extracted by this method are used in the optical receiver design presented in the next sections. Additionally, the accurate model of PD can become strength for electronic-photonic integrated circuit (EPIC) technology with existing accurate model of Si technology, which enables more optimized and precise optical receiver design.

1.3.2 Transimpedance Amplifier (TIA)

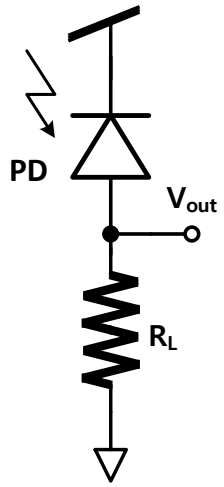
TIA converts current of PD output to the voltage with amplification to be handled by subsequent electronic circuits. As a front end of optical receiver, TIA mainly determines the entire performance such as noise, gain, and bandwidth. Hence, the main performances of TIA are high gain, large bandwidth, low noise and low power dissipation. The simplest way to realize TIA is adding the resistive load at the PD as shown in Fig. 1-8(a). The circuit model of this TIA can be presented as Fig. 1-8(b), and the transimpedance gain, 3-dB bandwidth and input-referred noise current can be given as

$$\text{Trnasimpedance gain} = R_L , \tag{1.2}$$

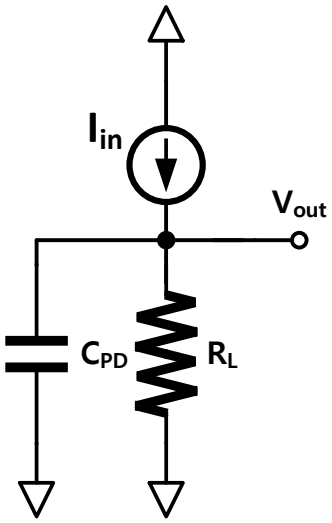
$$\text{3-dB bandwidth} = \frac{1}{2\pi R_L C_{PD}} , \tag{1.3}$$

$$\text{Input-referred noise} = \frac{4kT}{R_L}(\text{neglecting } C_{PD}) , \tag{1.4}$$

where k and T is Boltsmann constant and absolute temperature, respectively. C_{PD} represents PD junction capacitance. However, simple resistive load TIA has low gain-bandwidth product and poor noise characteristic. To solve this problem, there are representative configurations usually used in TIA design such as common gate (CG),



(a)

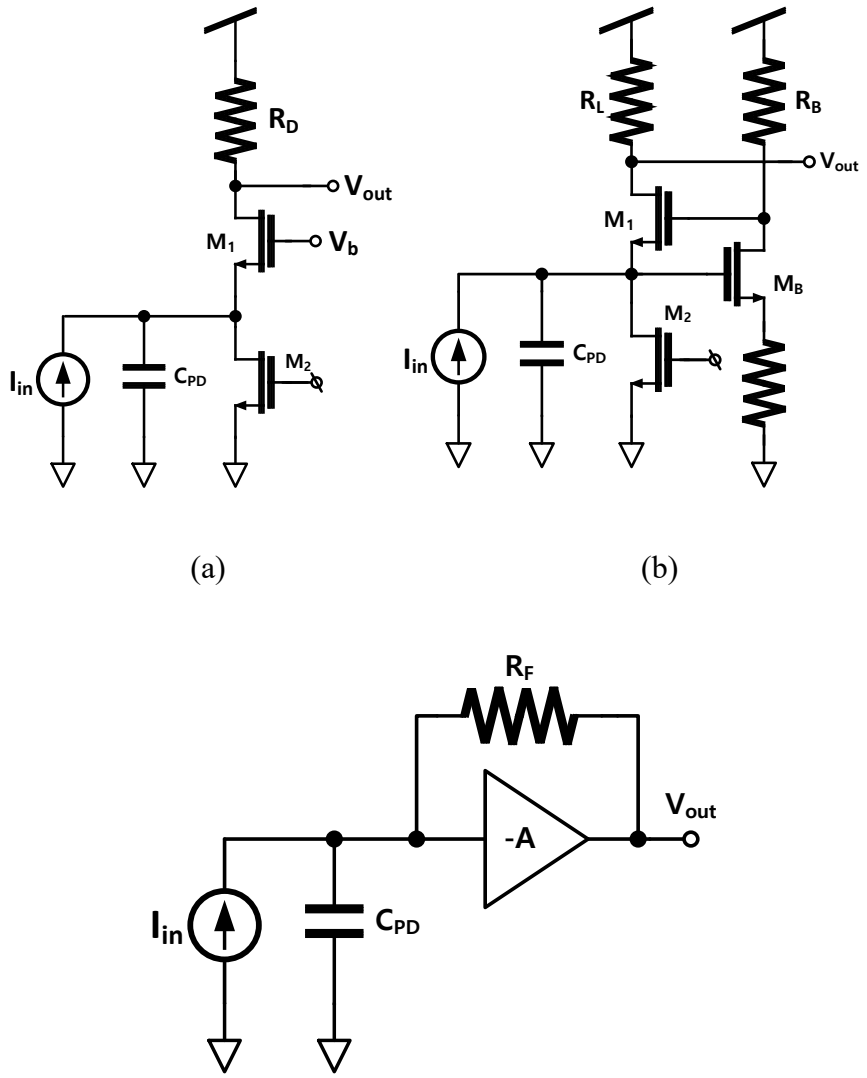


(b)

Fig. 1-8. (a) Resistive load TIA and (b) equivalent circuit.

regulated cascode (RGC) TIA [22] and negative feedback (NF) [29]. Fig. 1-9 shows the schematic and block diagram for the TIAs, and Table 1-1 shows transimpedance gain, 3-dB bandwidth and noise. CG TIA can achieve high gain and low input impedance, but it has relatively poor performance compared to other TIAs. NF has very large gain-bandwidth product and low noise, but it has stability problem unless core amplifier has infinite 3-dB bandwidth. It will be treated in section 4. RGC TIA has also large gain-bandwidth product, but it has voltage headroom problem with scaling technology, and increased noise from the common source.

As presented, among the configurations having nice performances, TIA should be carefully designed with trade off with design parameters and characteristics of PD to optimize optical receiver performances.



(a) (b)

(c)

Fig. 1-9. Schematic diagrams of (a) a common gate (b) a regulated cascode and (c) a negative feedback configurations.

Table 1-1

Performance summary of the representative TIAs.

	Transimpedance Gain	**3-dB bandwidth**	**Input referred noise**
CG	R_D	$\frac{1}{2\pi C_{PD}/g_{m1}}$	$4kT(\gamma g_{m2}+\frac{1}{R_D})$
RGC	R_L	$\frac{1}{2\pi Z^*_{in} C_{PD}}$	$4kT(\gamma g_{m2}+\frac{1}{R_L})$ + noise from CS
NF	$-\frac{A}{A+1}R_F$	$\frac{1+A}{2\pi R_F C_{PD}}$	$\frac{4kT}{R_F}+\frac{\overline{V^2_{n,amp}}}{R^2_F}$

$Z^*_{in}=\frac{1}{g_{m1}(1+g_{m2}R_B)}$ γ = transistor noise coefficient

1.3.3 Broadband Amplifier (BA)

The broadband amplifier (BA) provides high gain for achieving sensitivity of the subsequent circuits or measurement equipment. The BA should be designed with large bandwidth as well as high gain to without any performance degradation due to inter-symbol interference (ISI) penalty. To have large gain-bandwidth product, various broadband amplifier techniques are researched [30]-[34].

Table 1-2 shows summary of the broad circuit techniques and drawbacks [35]. Inductive peaking is generally used to achieve high speed, but it occupies large chip area. Other approaches such as active feedback and degenerations. They can efficiently increase gain-bandwidth product, but has drawbacks with power consumption and DC-gain reduction, respectively.

Cascaded BA is also broadly used, but number of stages should be carefully determined. Assuming that BA has n-identical gain stage, and each gain stage has m^{th}-order frequency response, overall bandwidth (BW_{total}) of cascaded BA can be expressed as [23]

$$BW_{total} = BW_{cell} \cdot \sqrt[2m]{\sqrt[n]{2} - 1}\,, \tag{1.5}$$

where BW_{cell} is the bandwidth of the each gain stage. With gain-bandwidth trade off, a gain-bandwidth product of an identical gain

Table 1-2

Summary of broadband circuit techniques and drawbacks [35].

	Technique	**Drawbacks**
Inductive peaking (Passive inductors)	Resonates out load capacitance	Large chip area
Inductive peaking (Active inductors)	Use transistors as passive inductors	Voltage headroom
Capacitive degeneration	Adds pole-zero pair	DC gain reduction
Negative miller capacitance	Compensates input capacitance	Capacitance matching
Cherry-hooper amplifier	Shunt feedback	Voltage headroom
Active feedback	Signal feedback w/o resistive loading	Power consumption
Reverse scaling	Stage sizing	Power consumption and input capacitance
Negative capacitance	Compensates load capacitance	Gain peaking and ringing

stage (GBW_{cell}) can be fixed by process, and GBW_{cell} can be detenmined as

$$GBW_{cell} = \frac{BW_{total}}{\sqrt[2m]{\sqrt[n]{2}-1}} \cdot \sqrt[n]{A_{total}}, \tag{1.6}$$

where A_{total} is the required total voltage gain of the entire BA. With Eq. (1.6), the BW_{total} with given process can be expressed as Eq. (1.7) below.

$$\frac{BW_{total}}{GBW_{cell}} = \frac{\sqrt[2m]{\sqrt[n]{2}-1}}{\sqrt[n]{A_{total}}}. \tag{1.7}$$

Fig. 1-10 shows the normalized total bandwidth with different number of stages for m^{th} order is 1, 2 and 3 if the required total BA gain is 40 dB (100). As shown in the Fig. 1-10, possible bandwidth is increased as number or stages increased or maximum at 10 of the number of stages for different m^{th} order, but the cascaded BA is typically designed with no more than five or six gain stages because of large power consumption as well as poor noise performance.

As discussed, techniques and number of stages should be chosen with consideration of target such as sensitivity of subsequent circuit, power consumption, process, and chip area

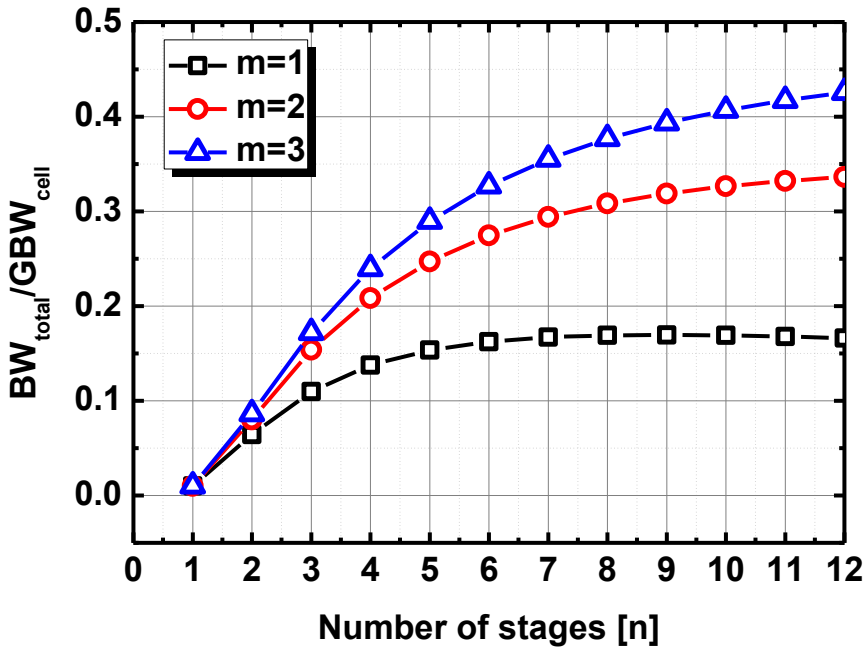


Fig. 1-10. Normalized total bandwidth as a function of n for A_{total} = 100 with various m^{th} order.

1.4. Outline of Dissertation

This dissertation focuses on bandwidth and SNR optimization of Si optical receivers with various design techniques. The main contribution of this work is establishing unified design for photonics and electronics by developing accurate model of photodetector and parasitic components for interconnect, which allows more optimized design. For monolithic optical receivers, better performances can be achieved based on the accurate circuit models of photodetectors, and for hybrid optical receiver, optimized performance can be achieved with considering model of the PD as well as the parasitic components such as pad capacitance and wire-bonding inductance in this dissertation. The remainder of this dissertation is organized as follows.

Chapter 2 shows various design techniques. Section 2-1 shows wire-bonding modeling and design optimization will be described. In section 2-2, design technique of under-damped TIA will be presented. Section 2-3 illustrates SNR consideration for optimized optical receivers.

Chapter 3 shows design-optimized hybrid optical receiver circuit. In section 3-3, circuit implementation is described. Section 3-4 presents measurement results of 20-Gb/s data transmission using fabricated

optical receiver circuit with PD equivalent circuit.

Chapter 4 shows a high-speed optical receiver with low-speed CMOS APD. In section 4-3, an equivalent circuit and characteristics of CMOS APD are illustrated. Section 4-4 presents implementation of the optical receiver circuit with under-damped transimpedance amplifier. Section 4-5 shows measurement results and demonstration of 12.5-Gb/s optical data transmission using the fabricated CMOS monolithic optical receiver.

Chapter 5 shows a 25-Gb/s monolithic optical receiver with Ge PD. Section 5-3 illustrates structure, characteristics, and an equivalent circuit of the Ge PD. Section 5-4 describes implementation of the optical receiver circuit. Section 5-5 shows measurement results and demonstration of the 25-Gb/s optical data transmission. In addition, measurement results are compared with simulation results with established circuit model of the photodetector.

Finally, this dissertation will be summarized with conclusion and discussion in Chapter 6.

2. Design Optimization Techniques

2.1. Bandwidth Optimization for Hybrid-Integrated Optical Receivers

There are many packaging methods for hybrid integration such as wire bonding, ball grid array, and flip-chip bonding. Among these, hybrid integration with wire bonding which is the simplest and the most cost-effective way will be discussed in this section. Fig. 2-1(a) and (b) show the equivalent circuit model for monolithic and hybrid integration of the part connecting PD and the receiver circuit, respectively. I_{PD} and C_{PD} represent the photocurrent and junction capacitance of PD, C_{IN} and R_{IN} indicate the input capacitance and resistance of the TIA, C_{PAD1} and C_{PAD2} are pad capacitances for PD and TIA, L_{BW} denotes bonding-wire inductance [36].

The 3-dB bandwidth of a monolithically integrated optical receiver can be continuously increases by reducing R_{IN} as the transfer function for

$$\frac{I_{IN}}{I_{PD}} = \frac{1}{2\pi R_{IN}(C_{PD}+C_{IN})}. \tag{2.1}$$

However, for hybrid integration, smaller R_{IN} does not guarantee larger

bandwidth. In this case, the transfer function is given as

$$\frac{I_{IN}}{I_{PD}} = \frac{1}{s^3 L_{BW} C_1 C_2 R_{IN} + s^2 L_{BW} C_1 + s(C_1 + C_2) R_{IN} + 1}. \quad (2.2)$$

where $C_1 = C_{PD} + C_{PAD1}$ and $C_2 = C_{PAD2} + C_{IN}$. In optical receiver design, R_{IN} is usually small so that $R_{IN} \ll | 1/sC_2 |$ can be assumed in the frequency range of interest. Then the Eq. (2.2) can be simplified as second-order system as

$$\frac{I_{IN}}{I_{PD}} \sim \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \quad (2.3)$$

with ω_n, the natural frequency, given as $1/\sqrt{L_{BW}C_1}$ and ζ, the damping ratio, given as $(R_{IN}/2)(C_1+C_2)/\sqrt{L_{BW}C_1}$. For critical damping with $\zeta = \sqrt{2}/2$, ω_n becomes the 3-dB bandwidth, which is determined by C_1 and L_{BW}.

Among the parameters used above, C_1 is determined by the characteristics of the target PD and pad capacitance. For this investigation, C_{PD} of 177 fF and C_{PAD1} of 50 fF are assumed resulting in the 14-GHz bandwidth of assumed PD with 50-Ω load. According to Eq. (2.3), in order to achieve large bandwidth, L_{BW} should be minimized. Fig. 2-2 shows a microphotograph of a bonding wire connecting two chips for wedge bonding is 0.5 mm with the wedge bonder available; the smallest bonding wire length is about to 1 mm.

Since the wire-bonding inductance for the wire used in this investigation is 0.8 nH/mm [37]. Consequently, the minimum L_{BW} is about 0.8 nH.

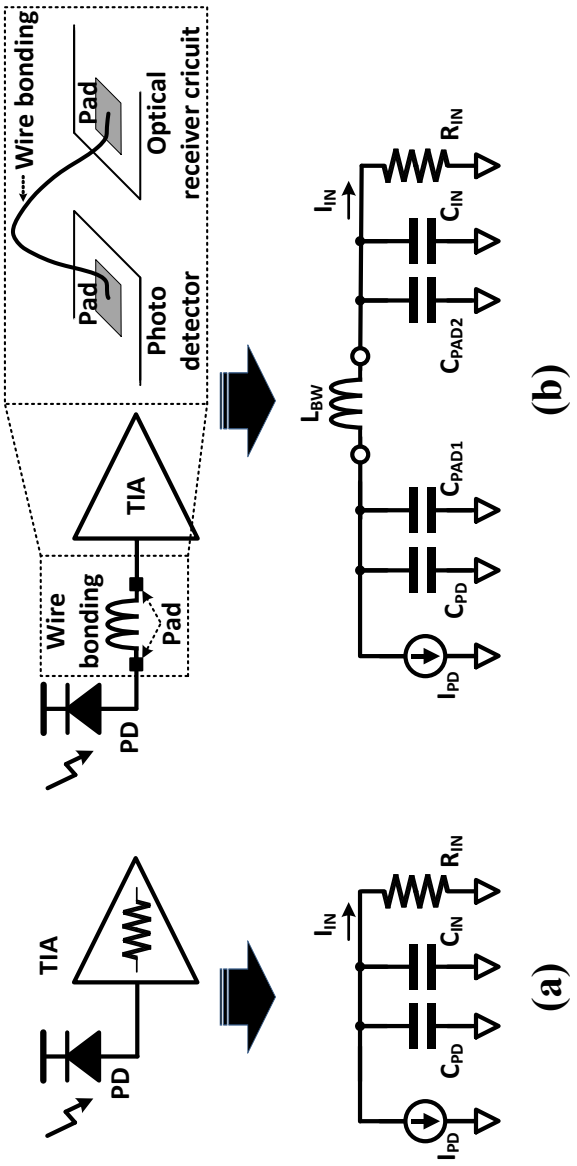


Fig. 2-1. Equivalent circuit model for (a) monolithic integration and (b) hybrid integration.

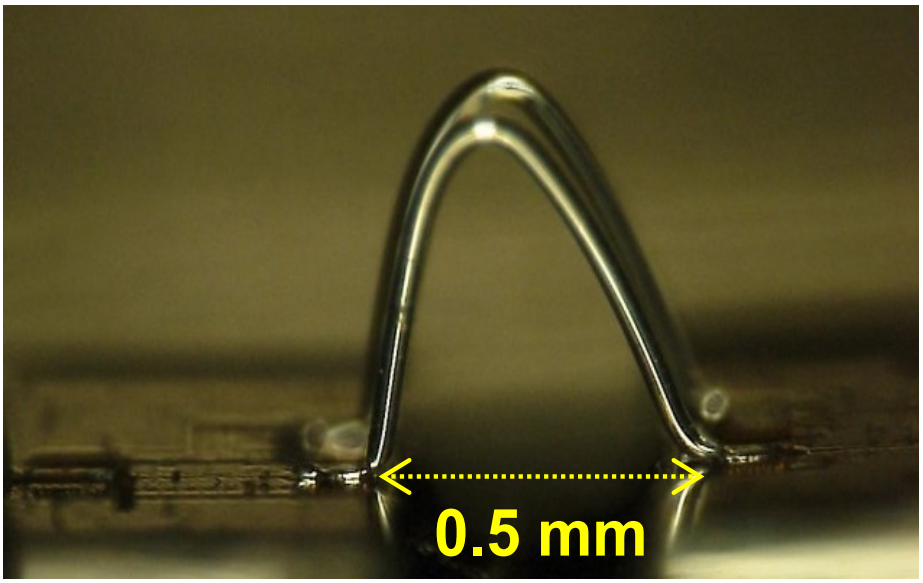


Fig. 2-2. Microphotograph of wire-bonding face in profile.

Since $R_{IN} = \sqrt{2L_{BW}C_1}/(C_1+C_{PAD2}+C_{IN})$ for critical damping, relationship between R_{IN} and C_{IN} for the parameter values can be determined as shown in Fig. 2-3. For C_{PAD2}, 50-fF is used assuming the pad size is 90 μm × 50 μm which is designed in the fabricated chip.

Fig. 2-4(a) shows the ideal simulation result of hybrid-integrated optical receiver for various R_{IN} with estimated parasitic capacitance, inductance and 30 fF of C_{IN}. As mentioned, unlike monolithic integration, the optical receiver with smaller R_{IN} does not have better performance. Large R_{IN} causes bandwidth loss, and small R_{IN} produces damping problem producing ringing in data transmission. Additionally, L_{BW} also causes similar problem as shown in the Fig. 2-4(b). Small and large L_{BW} can cause bandwidth and damping problem, respectively. According to Fig. 2-4(a) and (b), optimized bandwidth is about 12 GHz with design optimized R_{IN} and L_{BW} with assumed PD capacitance.

The optimized hybrid-integrated optical receiver will be verified with realized optical receiver in section 3.

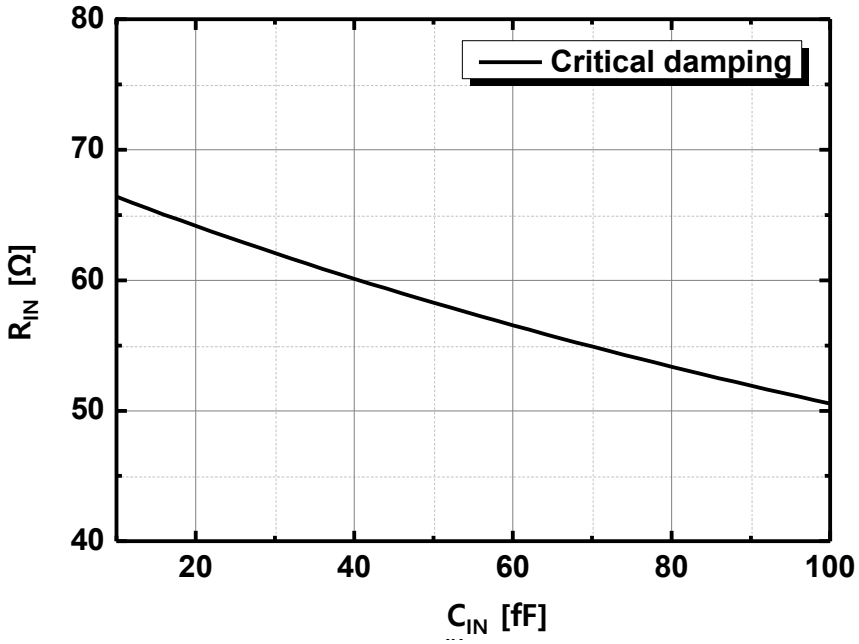
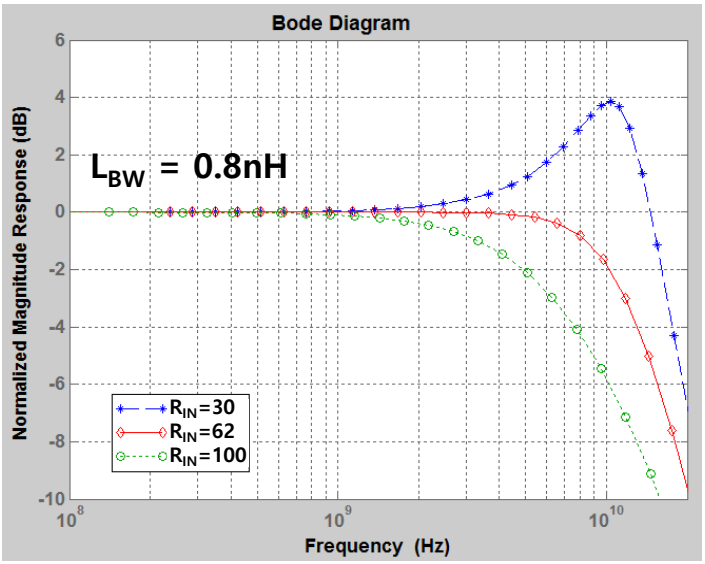
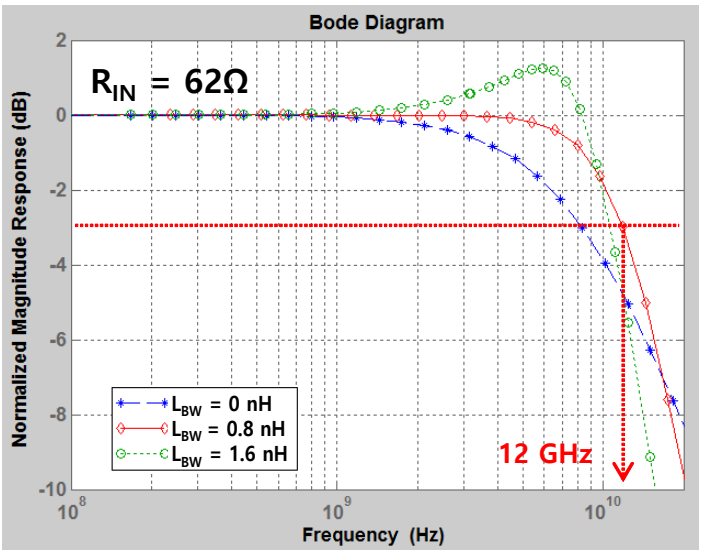


Fig. 2-3. Relation between R_{IN} and C_{IN} for critical damping.



(a)



(b)

Fig. 2-4. Simulated and normalized magnitude response for various (a) R_{IN} and (b) L_{BW} in hybrid-integrated optical receiver design.

2.2 Bandwidth Enhancement with Under-Damped TIA

For integrated optical receivers, their speeds can possibly suffer the bandwidth limitation from slow transit-time photocurrents of the PDs. Although several high-speed integrated optical receivers with low-bandwidth PDs have been reported, they rely on either PD structure modification such as spatially-modulated PDs (SM PDs) [38, 39] or electronic equalizers [17, 18]. However, SM PDs has low responsivity and electronic equalizers require additional power and chip area.

In this section, a new and simple technique of compensating PD bandwidth limit with an under-damped TIA will be shown, which can have better power efficiency and small chip area.

2.2.1 Under-Damped Transimpedance Amplifier

As shown in section 1.3.1, TIA bandwidth is determined by transit time of PD and RC time decided by RC components of PD and input impedance of TIA. With conventional TIA having flat and large bandwidth, the bandwidth of the optical receiver cannot exceed the transit time of the PD. However, the limited bandwidth of PD can be compensated by an under-damped TIA, which gives peaked frequency response and, consequently, enhanced optical receiver bandwidth.

Fig. 2-5(a) shows the block diagram of the under-damped TIA. The shunt-shunt feedback configuration is used, which provides low noise characteristics and high gain-bandwidth product. Since the transfer function of the core voltage amplifier can be approximated as [25]

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_0}}, \tag{2.4}$$

the closed loop transfer function of the TIA is given a

$$\frac{V_{out}}{I_{PD}} = -\frac{A_0\omega_0}{C_{PD}} \frac{1}{s^2 + \frac{R_F C_{PD} + 1/\omega_0}{R_F C_{PD}/\omega_0} s + \frac{(A_0+1)\omega_0}{R_F C_{PD}}}, , \tag{2.5}$$

which results in low-frequency transimpedance gain of $A_0R_F/(A_0+1)$. The denominator of Eq. (2.5) can be expressed as the standard second-order system function as $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ζ is the damping

factor and ω_n is the natural frequency with [25]

$$\zeta = \frac{1}{2}\frac{R_F C_{PD}\omega_0 + 1}{\sqrt{(A_0+1)\omega_0 R_F C_{PD}}} \quad \text{and,} \tag{2.6}$$

$$\omega_n = \sqrt{\frac{(A_0+1)\omega_0}{R_F C_{PD}}}\,. \tag{2.7}$$

The limited bandwidth of PD can be compensated by the peaked response of the under-damped TIA. For the under-damped response, we need $\zeta < \sqrt{2}/2$ and the peaking magnitude, M_P, and the peaking frequency, ω_p, are given as [40]

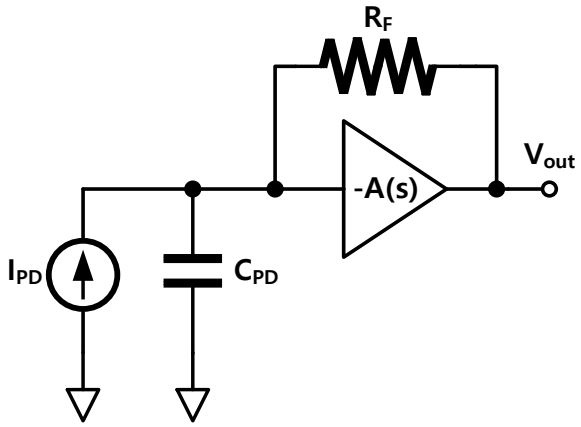
$$M_p = \frac{1}{2\zeta\sqrt{1-\zeta^2}} \quad \text{and} \tag{2.8}$$

$$\omega_p = \omega_n\sqrt{1-2\zeta^2}\,, \tag{2.9}$$

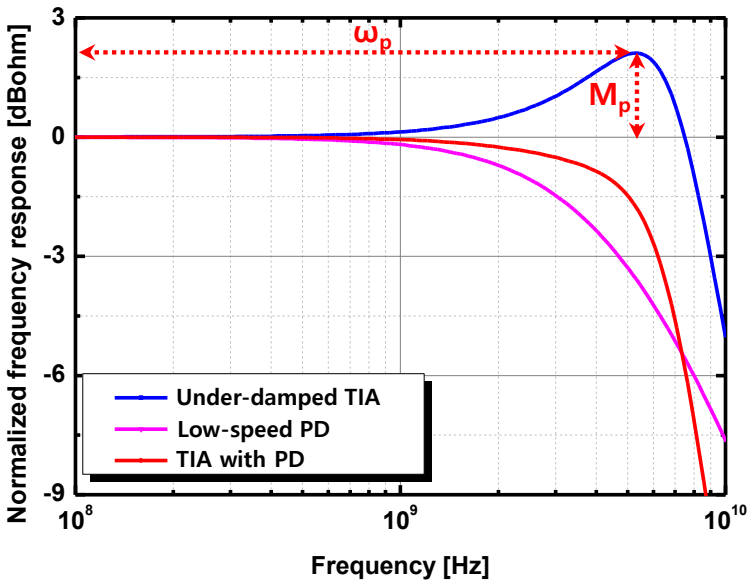
M_p and ω_p should be carefully determined so that the limited bandwidth of PD can be effectively compensated. Fig. 2-5(b) shows simulated frequency response of low-speed PD, under-damped TIA and TIA with PD. As can be seen the simulated frequency response, under-damped TIA can well compensate bandwidth limitation of PD. This enhancement can be achieved without any additional active circuits consuming additional power or SM PD decreasing responsivity only with circuit-model understanding of PD and TIA design modification.

The performance improvement with under-damped TIA will be

verified by realized monolithically-integrated optical receiver with CMOS APD in section 4.



(a)



(b)

Fig. 2-5. (a) Block diagram and (b) simulated frequency response of the under-damped TIA.

2.3 Optical Receiver Design with SNR Consideration

2.3.1 Sensitivity and SNR

Sensitivity is one of the most important evaluation parameters of the optical receivers. The sensitivity is determined the minimum optical power for target performance. The three important factors which influences optical receiver sensitivity are bit-error rate (BER), minimum received power and quantum limit of photodetection. BER is defined as the probability of incorrect identification of a bit by the decision circuit of the receiver. Minimum received power is a cut-off value below which receiver operation ceases. Use of avalanche PD can improve receiver sensitivity, but excess noise factor may degrade receiver sensitivity. Quantum limit of photodetection in almost all practical optical receivers is more than 20 dB or exceeds 1000 photons and is highly affected by light wavelength.

In this section, a technique of SNR consideration from sensitivity will be investigated, which can optimize power consumption and bandwidth of optical receivers.

2.3.2 Receiver Design with SNR Consideration

There are published optical receivers with noise simulations or considerations, but noise can be further optimized with target sensitivity for optimized power and bandwidth. For sensitivity of optical receiver specification, there are parameters given such as minimum sensitivity optical power, extinction ratio, and targeted BER.

Fig. 2-6 shows the flow chart of the SNR consideration. The first step of SNR consideration is SNR calculation from BER. The BER for on-off keying (OOK) is given as

$$\mathrm{BER}=\frac{1}{2}erfc\left(\frac{\mathrm{SNR}}{2\sqrt{2}}\right), \tag{2.10}$$

where SNR is signal-to-noise ratio and SNR is determined as

$$\mathrm{SNR}=\frac{\mathrm{I_{s,pp}}}{\sqrt{\mathrm{I^2_{n,total,rms}}}}, \tag{2.11}$$

where $\mathrm{I_{s,pp}}$ and $\mathrm{I_{n,total,rms}}$ are signal current and rms noise current peak-to-peak swing, respectively. Fig. 2-7 shows BER with different SNR. As can be seen in fig. 2-7, target SNR can be obtained from the target BER.

As a second step, total noise can be estimated from SNR of the integrated optical receiver and sensitivity as [41]

$$\text{Sensitivity} = 10\log\left(\frac{\text{SNR} \times I_{n,total,rms}(r_e+1)}{2\rho(r_e-1)}\right), \quad (2.12)$$

where r_e represents extinction ratio of modulated optical data and ρ indicates responsivity of the integrated PD. Total noise can be achieved from PD noise and input-referred noise of the receiver circuit as

$$I_{n,total,rms} = \sqrt{\overline{I^2_{n,PD,rms}} + \overline{I^2_{n,Rx,rms}}}, \quad (2.13)$$

where $I_{n,PD,rms}$ and $I_{n,Rx,rms}$ represents PD noise current and input-referred noise current of the receiver circuit, respectively. PD noise can be measured and modeled individually, and input-referred noise current can be applied to design and simulation of the optical receiver circuit with PDK form process vendors.

As a last step, the SNR with designed noise can be confirmed by simulation. Fig. 2-8 shows a block diagram of the optical receiver for SNR verification including a noise current source which represents total noise of PD and receiver circuit. Fig. 2-9 shows the eye diagrams with input-referred noise for BER of 1E−12 and 1E−3.

This design flow can be applied to not only OOK data but other modulated data. Table 2-1 shows BERs given with E_s/N_0 where E_s and N_0 represents signal and noise power ratio, respectively. Fig. 2-10 shows BER curve with different SNRs.

As start of this research, relationship between BER and SNR will be simulated and calculated. The calculated and measured BER will be verified with realized optical receiver in section 5.

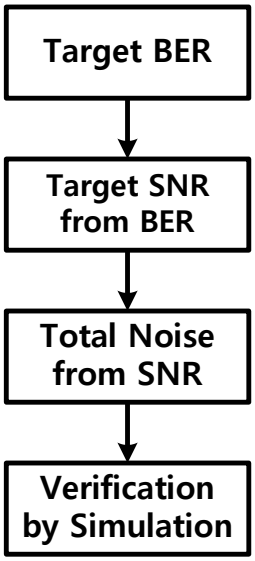


Fig. 2-6. Flow chart of the SNR consideration.

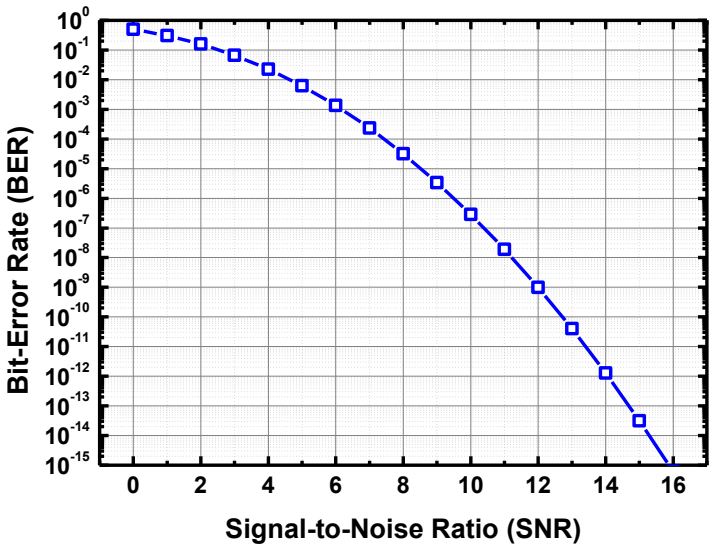


Fig. 2-7. BER curve with different SNR for OOK.

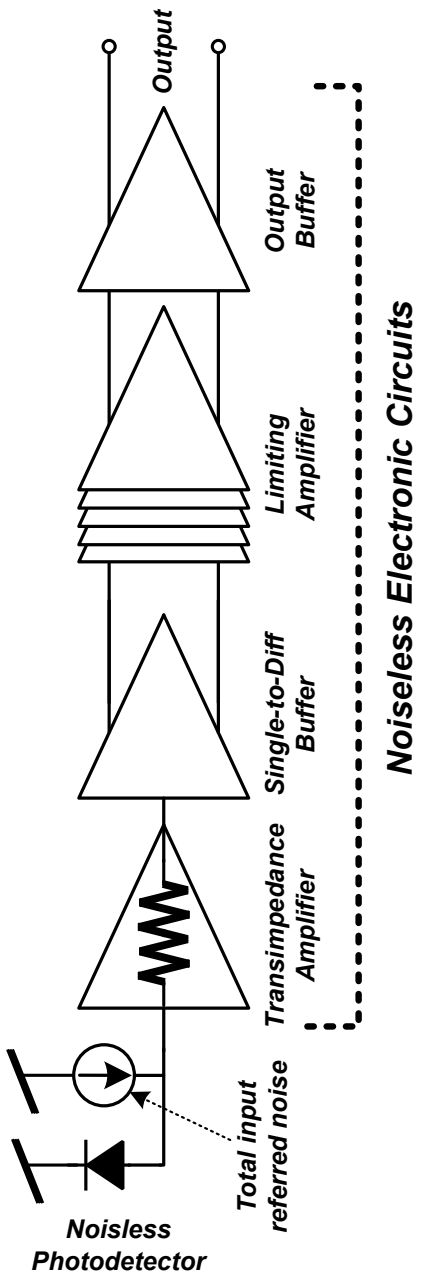


Fig. 2-8. Block diagram of the integrated optical receiver for signal-to-noise ratio verification.

<SNR=14, BER=1E-12 >

(a)

<SNR = 6.2, BER = 1E-3 >

(b)

Fig. 2-9. Simulated eye diagrams with noise current source for BER of 1E−12 and 1E−3.

Table 2-1.

Relationship between BER and SNR for various modulations.

	Bit-Error Rate
BPSK	$\frac{1}{2}erfc(\sqrt{E_s/N_0})$
QPSK	$erfc(\sqrt{E_s/2N_0})$
4-QAM	$erfc(\sqrt{E_s/2N_0})$
4-PAM	$\frac{3}{4}erfc(\sqrt{E_s/5N_0})$
16-QAM	$\frac{3}{2}erfc(\sqrt{E_s/10N_0})$
16-PSK	$erfc(\sqrt{E_s/N_0} \times sin(\frac{\pi}{16}))$

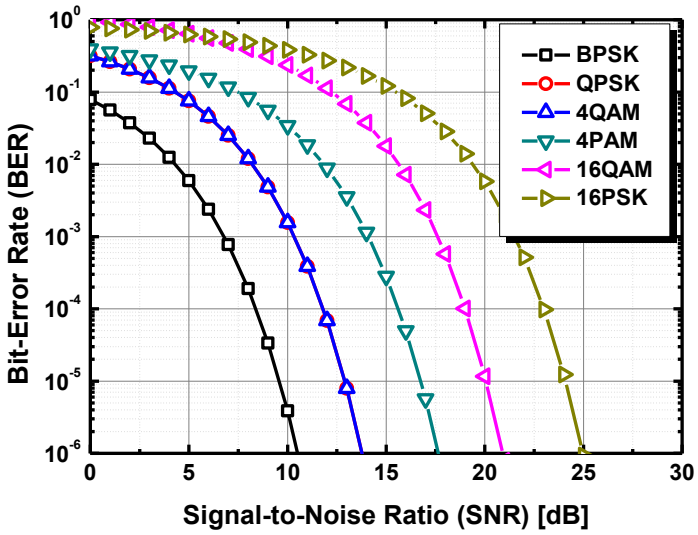


Fig. 2-10. BER curves with different SNR for various modulations.

3. Design Optimization of Hybrid Optical Receiver Circuit

3.1. Hybrid-Integrated Optical Receiver

Although monolithically integrated optical receivers that contain both PDs and electronic circuits are highly desirable, most integrated optical receivers for high-speed application routinely employ hybrid integration, because PDs and optical receivers are separately investigated or III-V semiconductors which may have disadvantages in cost consideration are widely used. A hybrid approach has advantages as photodetectors and receiver circuits having better performances are implemented in different technologies and are electrically connected on a board. However, such a hybrid approach necessarily includes undesired parasitic capacitance and inductance as mentioned in section 2.1, which can limit the high-speed operation and distort the frequency response of the optical receiver. There have been efforts which are mostly additional inductors are used between PD and input stage of the receiver to enlarge bandwidth with the undesired parasitic terms [20, 36]. However, there has been no report of optical receiver design optimization that fully considers the influence of bonding wires and

other parasitic components.

In this section, characterized parasitic capacitance, inductance due to bonding wires and calculated TIA design parameters in section 2.1 will be applied to the optical receiver circuit design. It will be verified with the realized optical receiver that the influence of parasitic inductance on bonding wires can be optimized with careful design, which can enhance the receiver circuit bandwidth using less passive inductors.

3.2 Overall Structure

Fig. 3-1 shows the block diagram of the realized optical receiver circuit. An equivalent circuit for PD is used for evaluating receiver circuit performance. The receiver circuit includes TIA with DC-balancing buffer, post amplifier (PA) and output buffer with 50-Ω termination for measurement instruments. The PD equivalent circuit includes on-chip capacitor emulating PDs. The TIA is designed in shunt-shunt feedback configuration and DC-balancing buffer including on-chip low-pass filter is added for fully differential signal. Also, PA amplifies the output signal of TIA to large signal enough to be detected by test instruments.

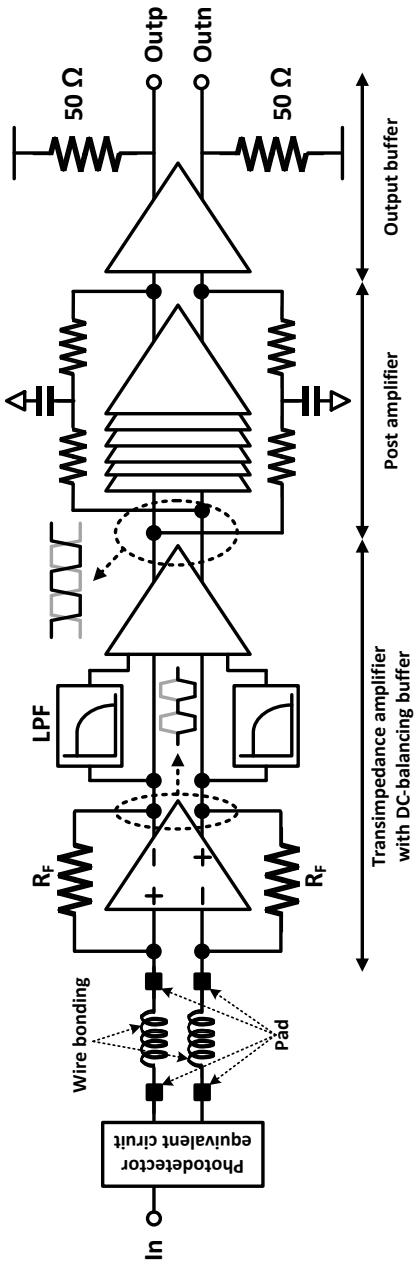


Fig. 3-1. Block diagram of the fabricated optical receiver circuit.

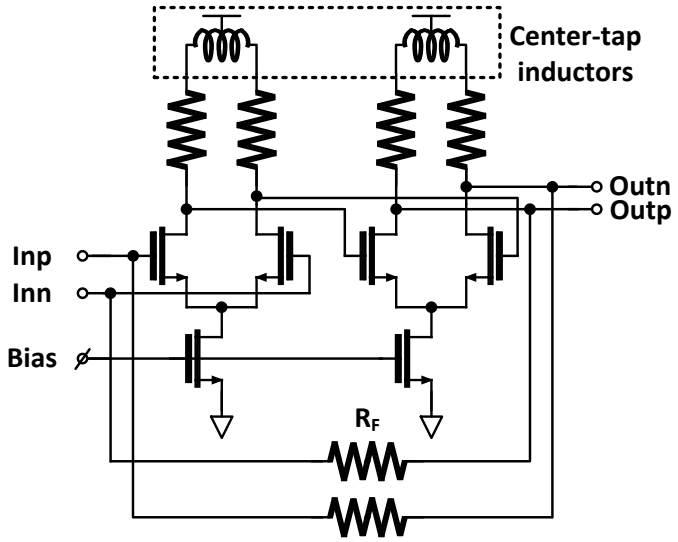
3.3 Optical Receiver Circuit

3.3.1 TIA with DC Balancing Buffer

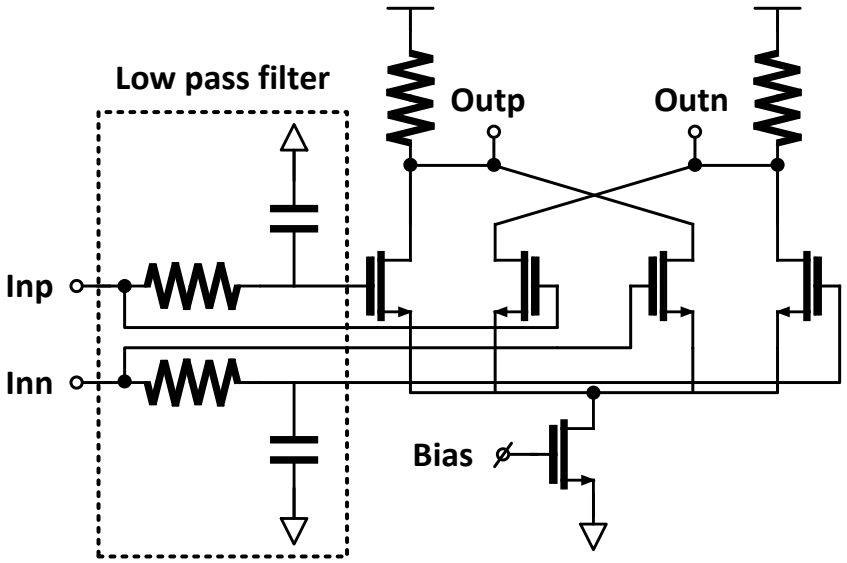
Although several TIA configurations are possible for high-speed TIA operation such as current-mode TIA [36], TIAs with regulated cascode input stage [42] or π-type inductive peaking [24], these have relatively low gain-bandwidth products, large chip area, and high input noises. Instead, a shunt-shunt feedback TIA is used in this design. Fig. 3-2(a) shows the schematic diagram of the shunt-feedback TIA. It consists of two feedback resistors and a core amplifier which is a two-stage differential amplifier with inductive peaking. The core amplifier employs two center-tap inductors to achieve large bandwidth with a small chip area. The realized TIA is designed with consideration of design parameters which is calculated in section 2.1. C_{IN} of shunt-feedback TIA is determined by the input MOSFET size of TIA core amplifier and R_{IN} is simply given as $R_F/(1+A_{core})$ where R_F indicates feedback resistance and A_{core} is voltage gain of TIA core amplifier. C_{IN} of 30 fF is used for this design that provides sufficient gain and bandwidth for the TIA core amplifier. Then, with A_{core} of 12 dB [V/V] and R_F of 300 Ω, R_{IN} is determined to 60 Ω. Fig. 3-3 shows the

normalized magnitude response of the designed TIA in post-layout simulation done with the PD equivalent circuit. As can be seen in Fig. 3-3, 3-dB bandwidth with 0.8-nH bonding-wire inductance is enhanced to 12 GHz compared to 4 GHz of 3-dB bandwidth without bonding-wire inductance as calculated in section 2.1.

Since the photo-generated currents are supplied to only one port of differential TIA inputs, TIA produces output differential signals with a DC offset, which causes a decision threshold problem. To solve this, a DC-balancing buffer is added at the TIA output. Fig. 3-2(b) shows the schematic of the DC-balancing buffer which consists of two low-pass filters and f_T-doubler. The low cut-off frequency of the buffer is set to 5 MHz to avoid any DC wander.



(a)



(b)

Fig. 3-2. Schematic diagram of designed (a) transimpedance amplifier and (b) DC-balancing buffer.

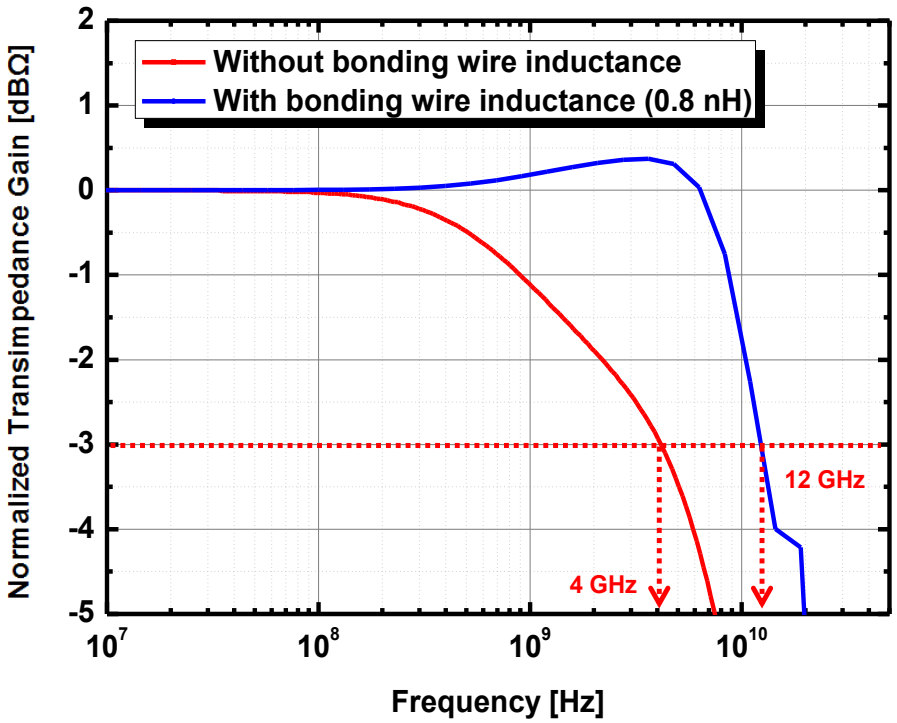
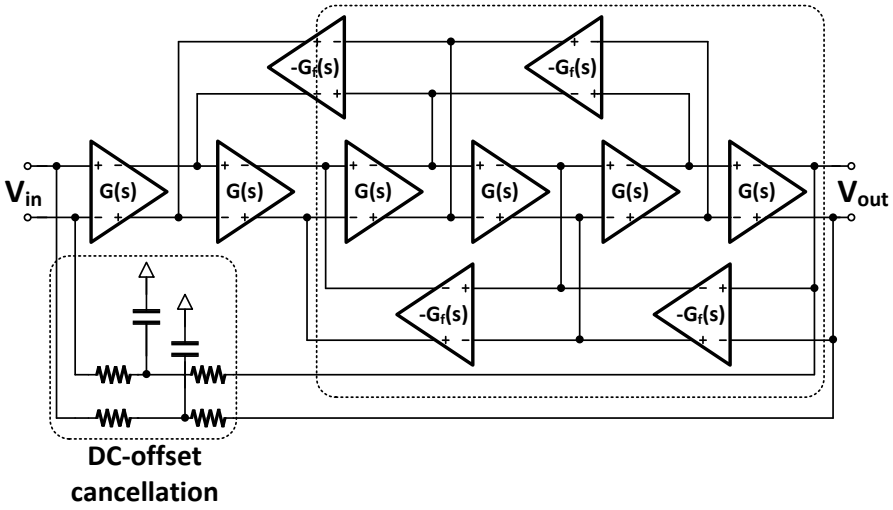


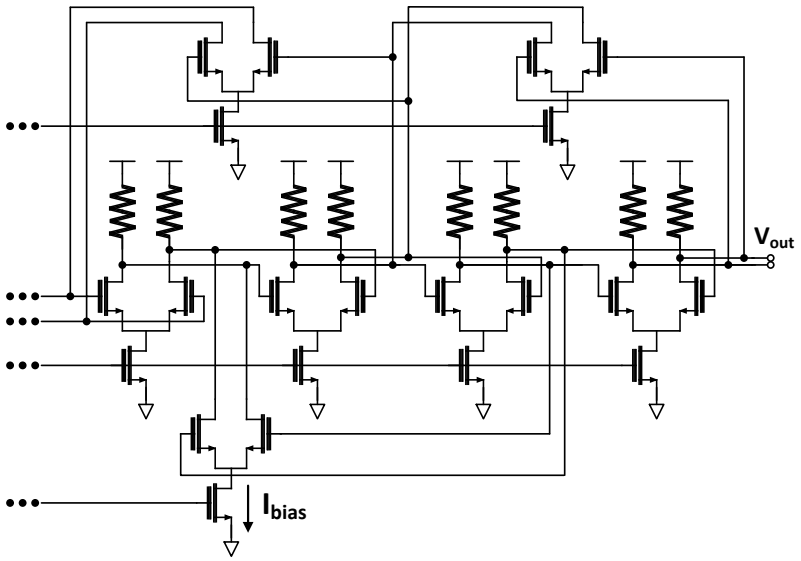
Fig. 3-3. Normalized transimpedance response of the TIA.

3.3.2 Post Amplifier

The PA provides additional gain to drive the following stage, which can be output buffer in this design or a clock and data recovery circuit in an optical receiver with additional blocks integrated. Fig. 3-4(a) shows the simplified block diagram of the PA composed of six gain stages with interleaved active feedback [36]. DC offset cancellation is also included to help DC balancing. The PA provides 20-dB voltage gain and 20-GHz of 3-dB bandwidth. Fig. 3-4(b) shows the schematic diagram for the part inside the box in Fig. 3-4(a).



(a)



(b)

Fig. 3-4. (a) Block diagram and (b) schematic diagram of the designed post amplifier.

3.4 Measurement Results

Fig. 3-5 shows the chip photograph of the optical receiver fabricated with standard 65-nm CMOS technology. The realized receiver circuit occupies 0.44 mm × 0.5 mm of chip area, and consumes 84 mW with 1.2-V supply excluding output buffer.

Fig. 3-6 shows the measurement setup. The photodetector equivalent circuit with the same 65-nm CMOS technology and the optical receiver circuit are connected with bonding wires on a FR4 test board. The measurements are done with on-wafer probing. The PD equivalent circuit includes a 50-Ω matching resistor, a 5-kΩ resistor that converts applied voltages into currents, and two 177-fF MIM capacitors emulating PDs. Fig. 3-7 shows measured and simulated transimpedance frequency responses. The measured transimpedance gain and 3-dB bandwidth is 86 dBΩ and 12 GHz, respectively. Fig. 3-8(a) shows the measured bit-error rate (BER) performance as a function of input current swing. 20-Gb/s $2^{31}-1$ PRBS data detection is successfully achieved with BER less than 10^{-12}. Fig. 3-8(b) also shows the measured 20-Gb/s eye diagram with input current swing of 50 μA_{pp}. Fig. 3-9 shows measured and simulated output noise voltage density without the PD equivalent circuit. The measurement result is well

matched with the simulation result. The extracted input-referred noise current density ($i_{n,in}$) with C_1 = 227 fF and L_{BW} = 0.8 nH is also shown in Fig. 3-9. The input referred rms noise current can be calculated as [43]

$$I_{n,Rx}[A_{rms}] = \sqrt{\frac{f_{BW,N}}{f_{BW,S}} \int_{100MHz}^{f_{BW,S}} \overline{i_{n,in}^2} df} = 2.55\mu A_{rms}, \quad (2.4)$$

where $f_{BW,S}$ and $f_{BW,N}$ is the signal and equivalent noise bandwidth of the receiver circuit, respectively. The extracted average input-referred noise current density is

$$I_{n,in,avg} = \frac{I_{n,Rx}}{\sqrt{f_{BW,S}}} = 23.3 pA/\sqrt{Hz}. \quad (2.5)$$

The sensitivity of the fabricated optical receiver circuit for BER less than 10^{-12} can be estimated using the following equation [41]

$$\text{Sensitivity} \approx 10\log\left[\frac{14.1 I_{n,Rx}(r_e+1)}{2\rho(r_e-1)} 1000\right]. \quad (2.6)$$

Where ρ is the PD responsivity and r_e is the extinction ratio of the modulator. With ρ = 0.5 A/W and r_e = 5 dB, above equation gives sensitivity of −12.7 dBm for $I_{n,Rx}$ of 2.55 μA_{rms}.

Table 3-1 shows performance comparison with previously reported 20- and 25-Gb/s receivers fabricated in CMOS technology. The following figure of merit (FOM) given in [44] is used.

$$\text{FOM}=\frac{(\frac{\text{tech.}}{0.065})^2}{\text{Area}}\frac{\text{Transimpedance Gain? Bandwidth}}{\text{Power Dissipation}}[\text{GHz}\Omega/\text{mm}^2\cdot\text{mW}]. \quad (2.7)$$

The FOM includes gain-bandwidth product, power dissipation and area normalized to 65-nm technology [45]. The fabricated receiver has the highest FOM of 12955 GHzΩ/mm^2·mW because additional inductors between PD and TIA for 20-Gb/s high-speed are not used by design optimization and high gain and large bandwidth with small area can be achieved with using less inductors.

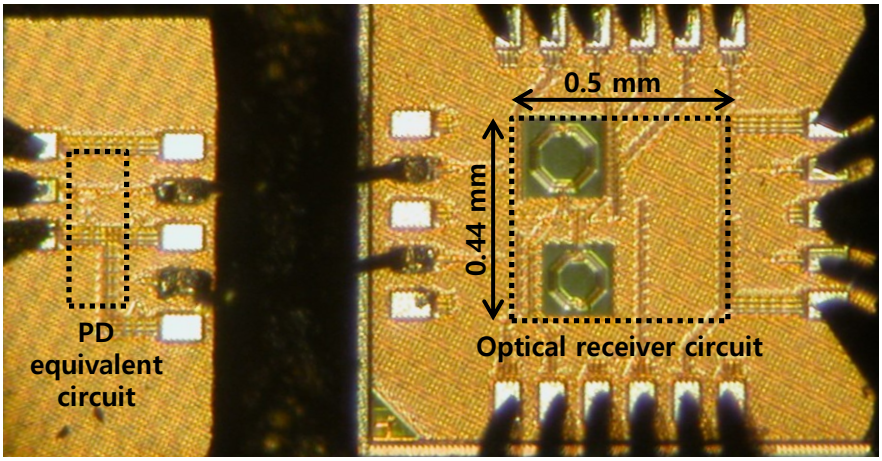


Fig. 3-5. Microphotograph of the fabricated optical receiver.

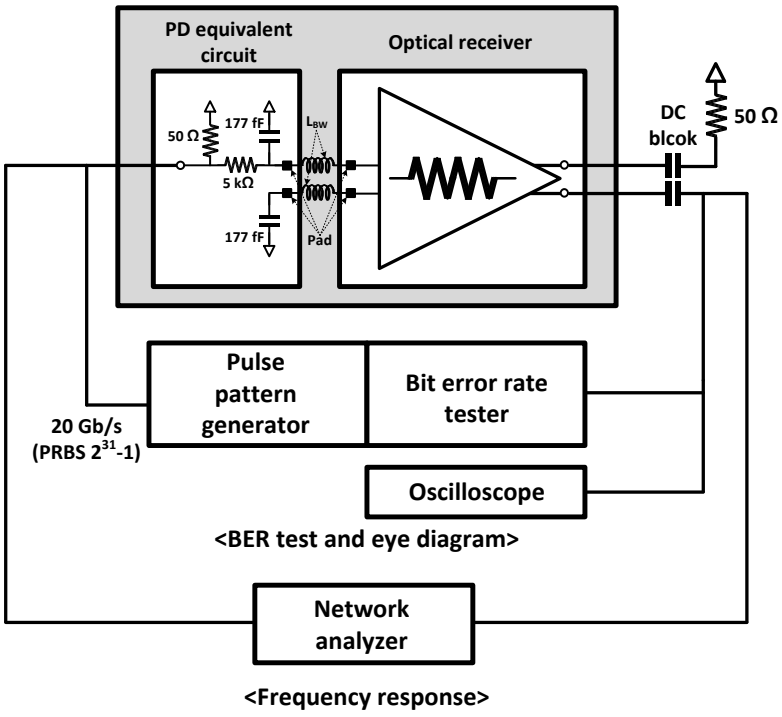


Fig. 3-6. Measurement setup.

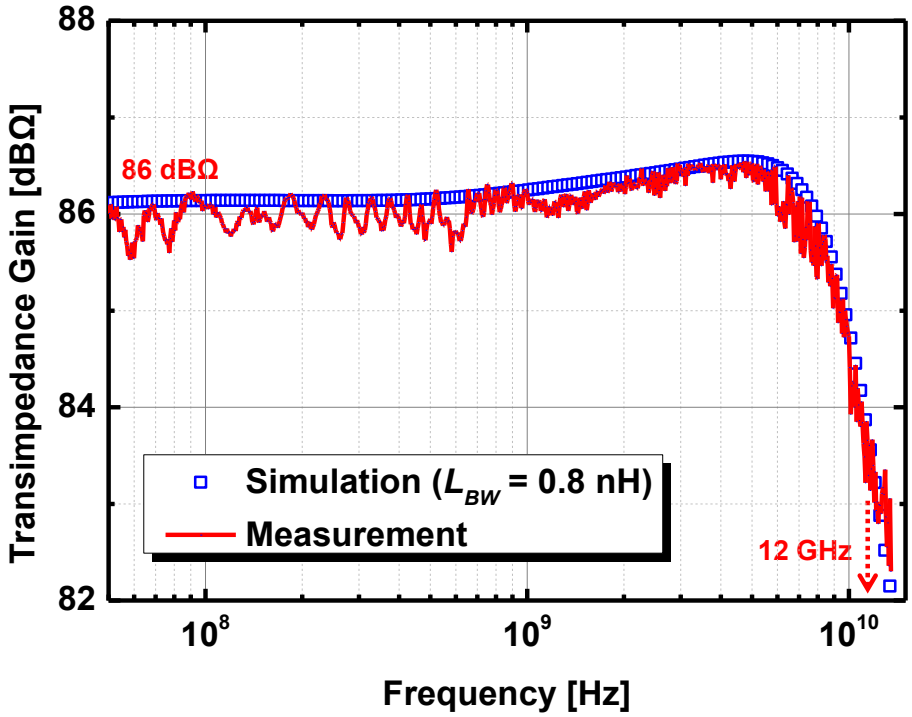
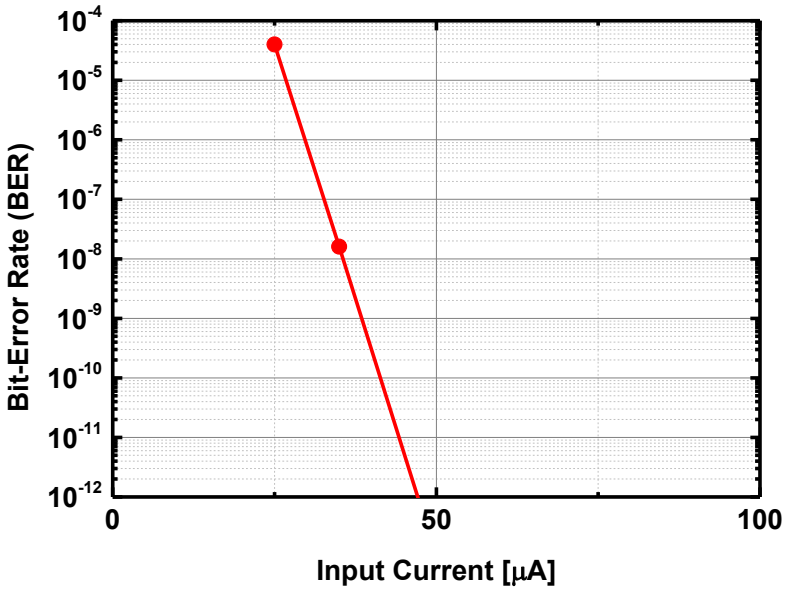
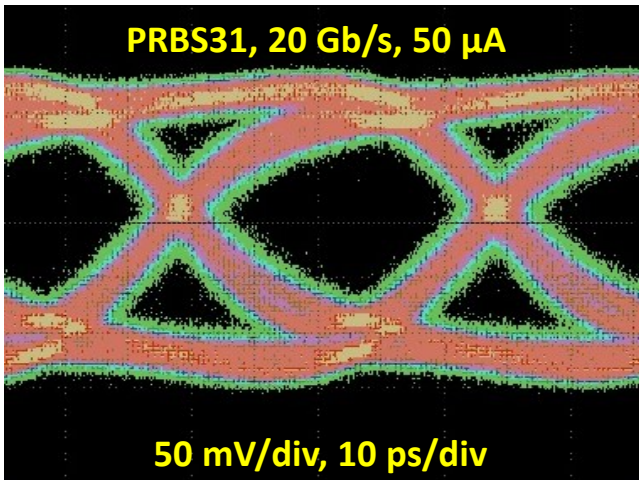


Fig. 3-7. Measured and simulated magnitude response.



(a)



(b)

Fig. 3-8. (a) Measured BER versus input current and (b) measured 20-Gb/s single-ended eye diagram.

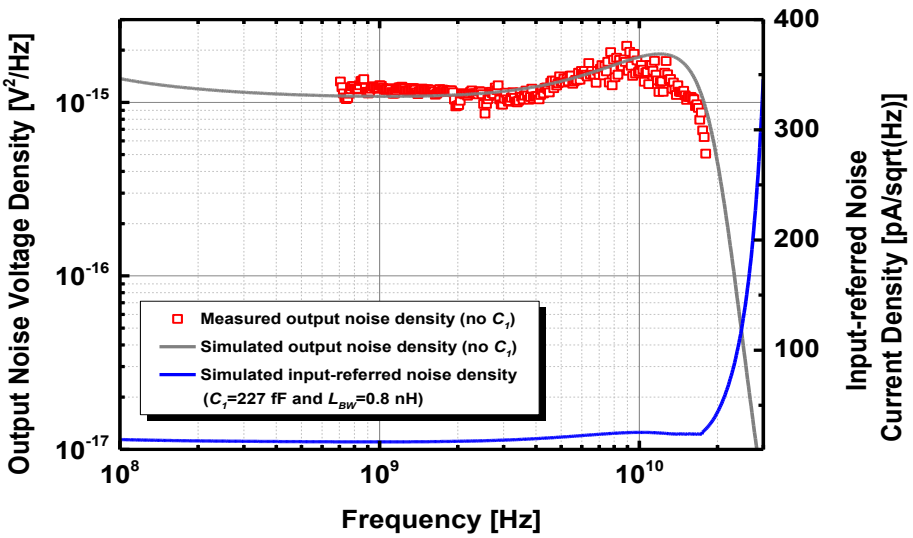


Fig. 3-9. Measured and simulated output noise voltage density and extracted input-referred noise current density.

Table 3-1

Performance comparison of the optical receivers.

	[36] 10' TCASII	[44] 10' JLT	[46] 13' ISSCC	This work
Technology [nm]	130-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS
Data rate [Gb/s]	20	25	25	20
Bandwidth [GHz]	12.6	22.8	21.4	12
Supply [V]	1.2	1.8 (TIA)/ 1.0 (PA)	3.3 (TIA)/ 1.0 (PA)	1.2
Power dissipation [mW]	38.3	74	90.9	84
Transimpedance [dBΩ]	60	69.8	76.8	86
$I_{n,in,avg}$ [pA/$\sqrt{Hz}$]	42.2	23.2	17.8	23.3
Chip area [mm^2]	0.22	0.4	0.32	0.22
FOM [GHzΩ/$mm^2 \cdot mW$]	5980	2380	5090	12955

3.5 Summary

A 20-Gb/s optical receiver circuit is realized in 65-nm CMOS technology. Bonding-wire inductance and pad capacitances are considered in this design so that the optimum receiver circuit can be achieved. The receiver circuit can successfully detect 20-Gb/s $2^{31}-1$ PRBS data with BER less than 10^{-12} measured with a PD equivalent circuit and the optimization method of hybrid-integrated optical receiver in section 2.1 is successfully verified.

4. High-Speed CMOS Optical Receiver with Low-Speed CMOS APD

4.1. CMOS Integrated Optical Receivers

For CMOS integrated optical receivers, PDs in standard CMOS process use for detecting 850-nm wavelength light. However, the 850-nm CMOS PDs suffer the bandwidth limitation from slow diffusive photocurrents. Although several high-speed monolithically integrated optical receivers realized in CMOS technology have been reported, as described in section 2.2, PD structure modifications and electronic equalizers have disadvantages such as low responsivity and additional power and chip area.

In this section, realized monolithically integrated optical receiver with CMOS APD will be shown and better performance with the under-damped TIA described in section 2.2 will be verified with measurement results.

4.2. Overall Structure

Fig. 4-1 shows the simplified block diagram of the proposed CMOS integrated optical receiver. It is composed of a CMOS APD with a dummy PD, an under-damped TIA, a DC-balancing buffer and an output buffer with 50-Ω load. The CMOS APD has P+/N-well junction and optical window of 10 μm × 10μm. The dummy PD provides symmetric capacitance to the differential TIA input. The TIA is designed in shunt-shunt feedback configuration and has under-damped response for compensating the limit of CMOS APD. DC-balancing buffer having f_T-doubler structure is added for fully differential signal. The receiver does not contain a LA, because typical CDR circuits after optical receiver require input sensitivity of tens of mV. A LA is not needed if CDR circuit can be directly integrated with the TIA. In the next chapters, circuit model of the CMOS APD, design procedure of receiver circuits such as TIA and DC balancing buffer, and measurement results will be presented.

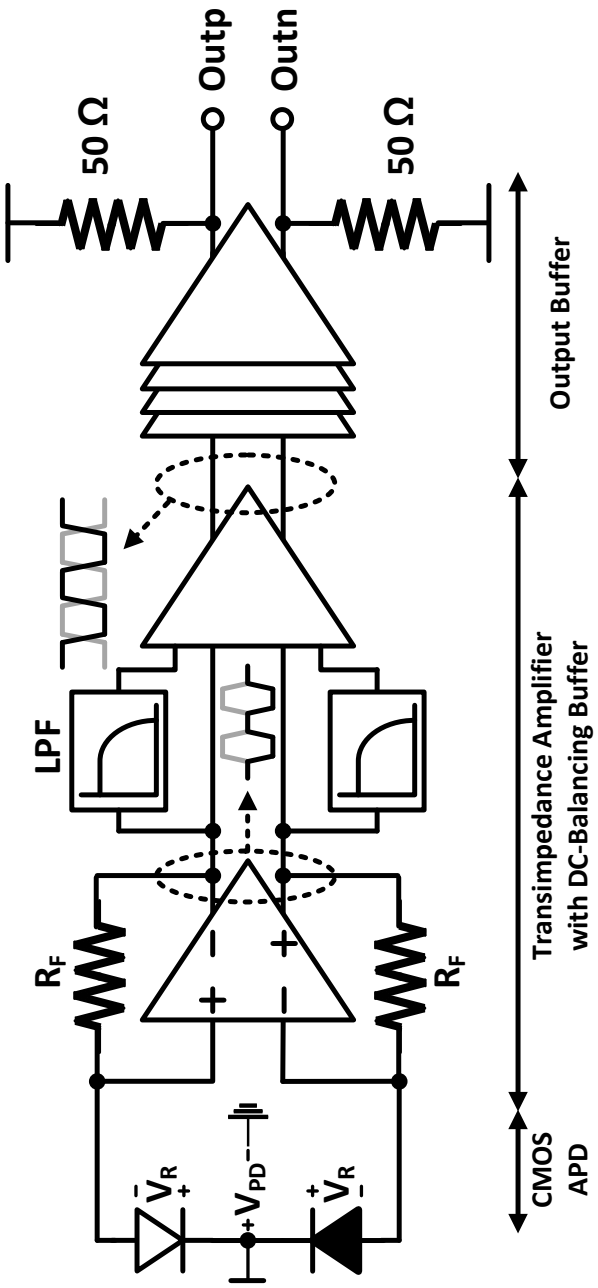


Fig. 4-1. Block diagram of the fabricated optical receiver.

4.3 Circuit Model of the CMOS APD

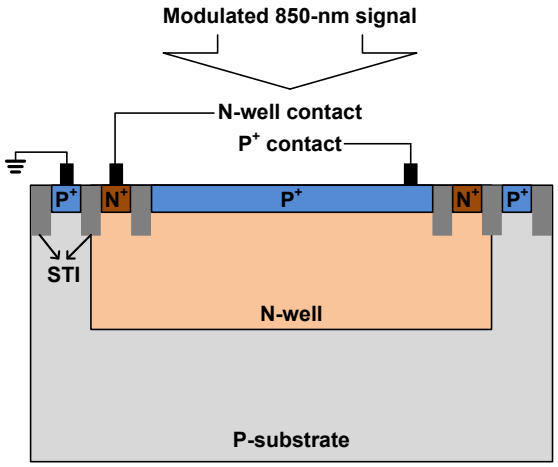
Fig. 4-2(a) and (b) show the cross section and the top view of the CMOS APD integrated in fabricated optical receiver. The CMOS APD is realized with P^+ source/drain and N-well junction in standard CMOS technology without any design-rule violation. Shallow trench isolation (STI) surrounding the vertical P-N junction provides large and uniform electric fields that are desired for avalanche gain. Photo-generate currents are taken from P^+ contact to TIA since currents from N well include diffusive components due to light absorbed in P substrate. The CMOS APD has 10 μm × 10 μm of optical window for optimal photo-detection bandwidth [27].

For TIA design optimization, an accurate circuit model of CMOS APD is essential. The 3-dB bandwidth of the CMOS APD, f_{PD}, can be determined as

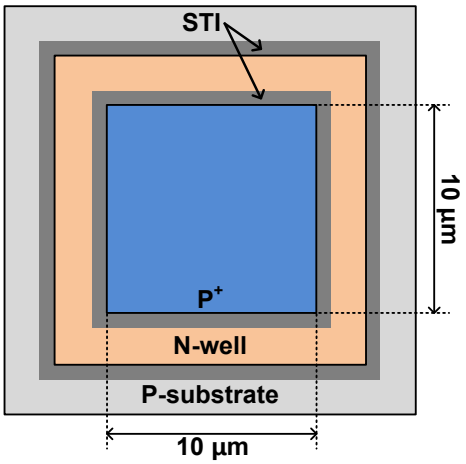
$$f_{PD} = \frac{1}{\sqrt{\left(\frac{1}{f_{tr}}\right)^2 + \left(\frac{1}{f_{RC}}\right)^2}}. \tag{4.1}$$

where f_{tr} and f_{RC} represent the 3-dB bandwidth of the photo-generated hole transit time and the CMOS-APD RC time, respectively. Fig. 4-3(a) shows the measured DC characteristic of the CMOS APD with 0-dBm input optical power. Fig. 4-3(b) shows measured photo-detection

frequency response of the CMOS APD. Fig. 4-4 shows the equivalent circuit model of the CMOS APD. C_j and R_s represent the depletion region capacitance and N-well series resistance, respectively. R_{tr} and C_{tr} are used to model the influence of hole transit time in the APD. The numerical values of these parameters are determined by fitting equivalent circuit simulation results to measured s parameter and frequency responses of CMOS APD. The extracted model parameters and values are listed in Table 4-1. As can be seen in Fig. 4-3(b), the APD has limited 3-dB bandwidth of about 4.7 GHz and the hole transit time dominantly limits 3-dB bandwidth of the CMOS APD.

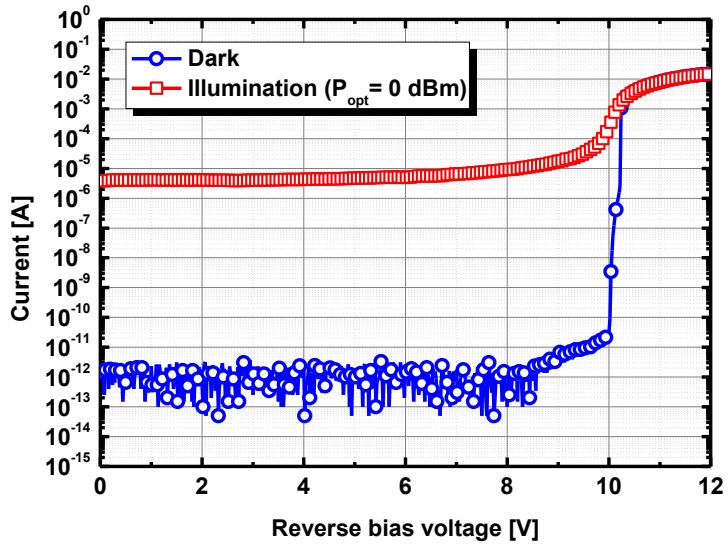


(a)

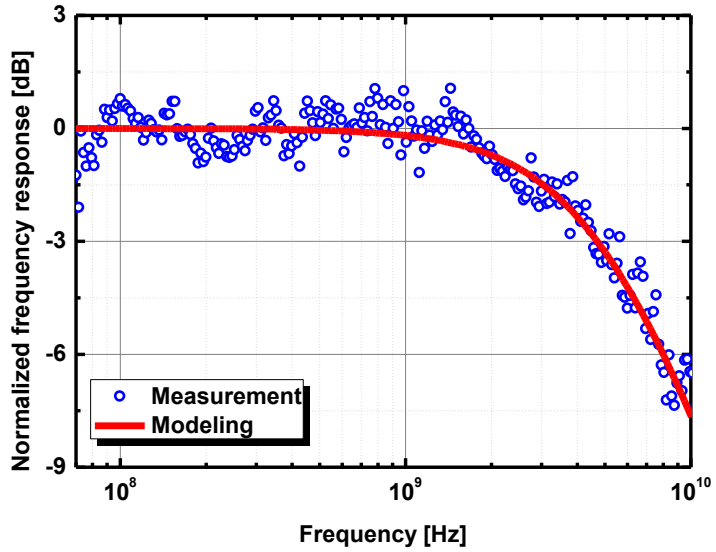


(b)

Fig. 4-2. (a) Cross section and (b) top view of the fabricated CMOS APD.



(a)



(b)

Fig. 4-3. (a) DC characteristic, (b) measured and simulated frequency response of CMOS APD.

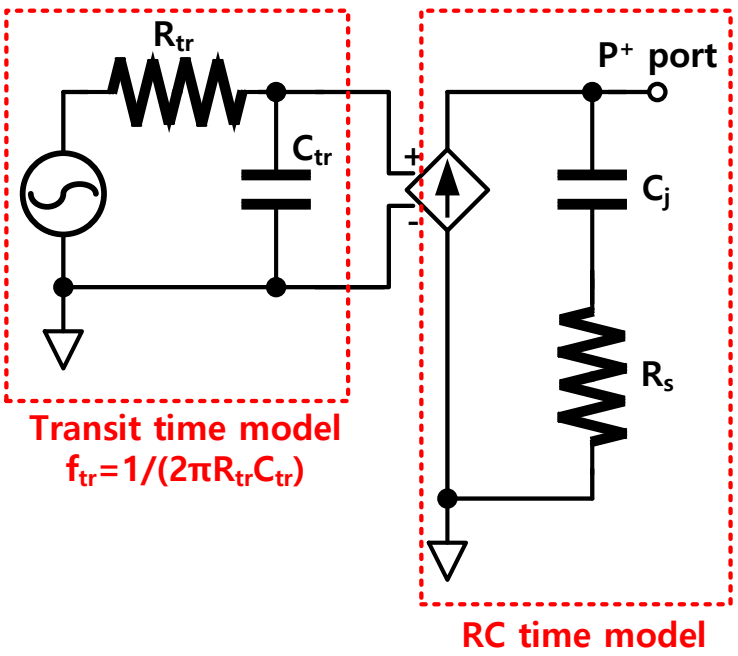


Fig. 4-4. Equivalent circuit model of CMOS APD.

Table 4-1

Extracted model parameters of CMOS APD

Model parameter	Value
Junction capacitance (C_j)	45 fF
Series resistance (R_s)	90 Ω
Transit time bandwidth (f_{tr})	5 GHz

4.4 CMOS Optical Receiver Circuit

4.4.1 Under-Damped TIA

The limited bandwidth of CMOS APD can be compensated by an under-damped TIA, which gives peaked frequency response and, consequently, enhanced optical receiver bandwidth.

Fig. 4-5(a) shows the block diagram of the under-damped TIA. The shunt-shunt feedback configuration is used, which provides low noise characteristics and high gain-bandwidth product. Since the transfer function of the core voltage amplifier can be approximated as [25]

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_0}}, \tag{4.2}$$

the closed loop transfer function of the TIA is given a

$$\frac{V_{out}}{I_{PD}} = -\frac{A_0\omega_0}{C_{PD}} \frac{1}{s^2 + \frac{R_F C_{PD} + 1/\omega_0}{R_F C_{PD}/\omega_0} s + \frac{(A_0+1)\omega_0}{R_F C_{PD}}}, \tag{4.3}$$

which results in low-frequency transimpedance gain of $A_0R_F/(A_0+1)$. The denominator of Eq. (4.3) can be expressed as the standard second-order system function as $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ζ is the damping factor and ω_n is the natural frequency with [25]

$$\zeta = \frac{1}{2} \frac{R_F C_{PD}\omega_0 + 1}{\sqrt{(A_0+1)\omega_0 R_F C_{PD}}} \quad \text{and,} \tag{4.4}$$

$$\omega_n = \sqrt{\frac{(A_0+1)\omega_0}{R_F C_{PD}}} \,. \tag{4.5}$$

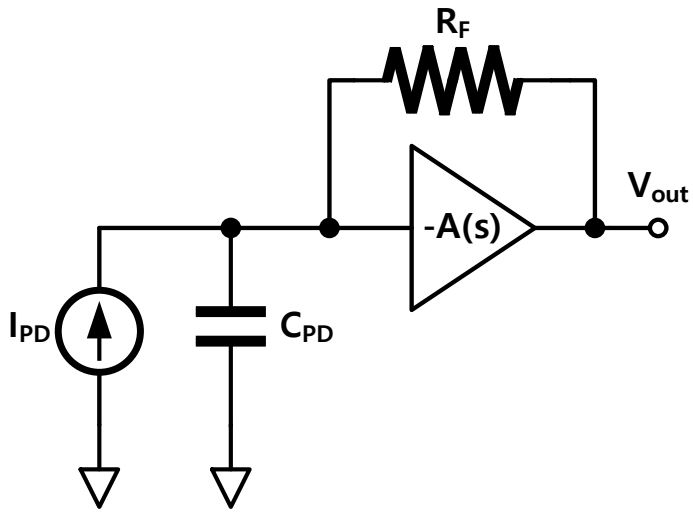
The limited bandwidth of CMOS APD can be compensated by the peaked response of the under-damped TIA. For the under-damped response, we need $\zeta < \sqrt{2}/2$ and the peaking magnitude, M_P, and the peaking frequency, ω_p, are given as [40]

$$M_p = \frac{1}{2\zeta\sqrt{1-\zeta^2}} \quad \text{and} \tag{4.6}$$

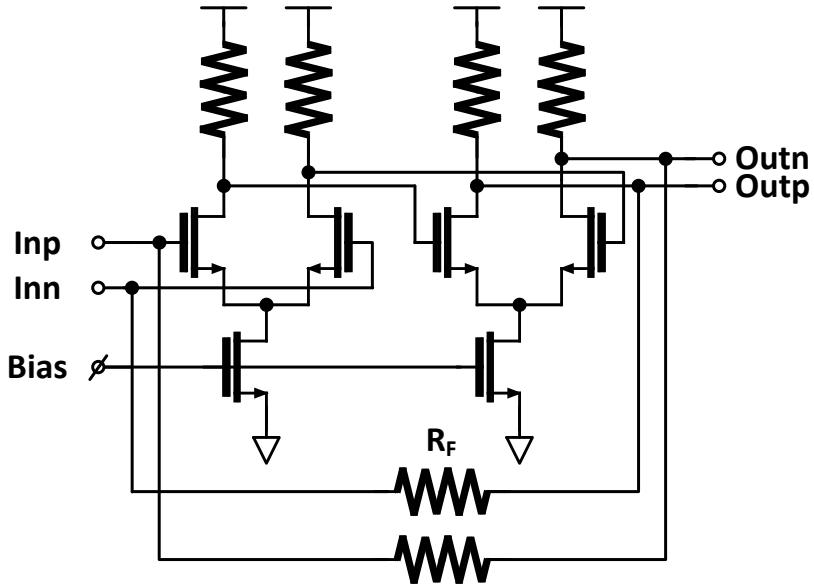
$$\omega_p = \omega_n \sqrt{1-2\zeta^2} \quad , \tag{4.7}$$

M_p and ω_p should be carefully determined so that the limited bandwidth of CMOS APD can be effectively compensated. Fig. 4-5(b) presents the schematic diagram of the TIA and Fig. 4-6(a) shows simulated frequency response of CMOS APD, under-damped TIA and the integrated optical receiver. The under-damped TIA has 2-kΩ feedback resistor and core amplifier of TIA provides 20-dB gain and 4.5-GHz bandwidth. The under-damped TIA results in 3.5 dB of M_p and 25 GHz of ω_p, which gives optimal frequency compensation performance. As shown in Fig. 4-6(b), the under-damped TIA achieves 3-dB bandwidth of 6 GHz with CMOS APD having 4.7-GHz bandwidth. Fig. 4-6(b) shows the eye diagrams of the transient simulation results for CMOS APD and TIA output with 12.5-Gb/s PRBS31 data. As can be seen the

eye diagram of under-damped TIA output is well opened by bandwidth enhancement. This enhancement can be achieved without any additional active circuits consuming additional power or SM PD decreasing responsivity only with circuit-model understanding of CMOS APD and TIA design modification.

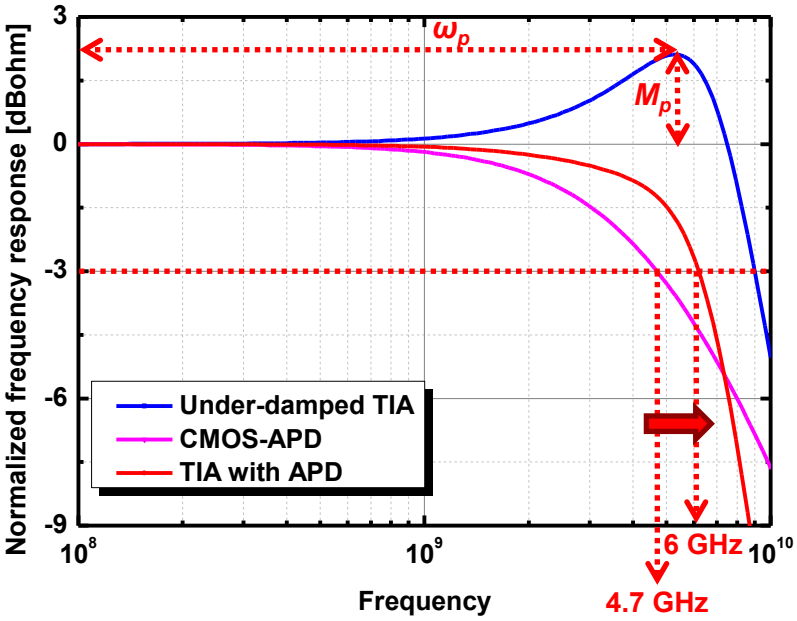


(a)

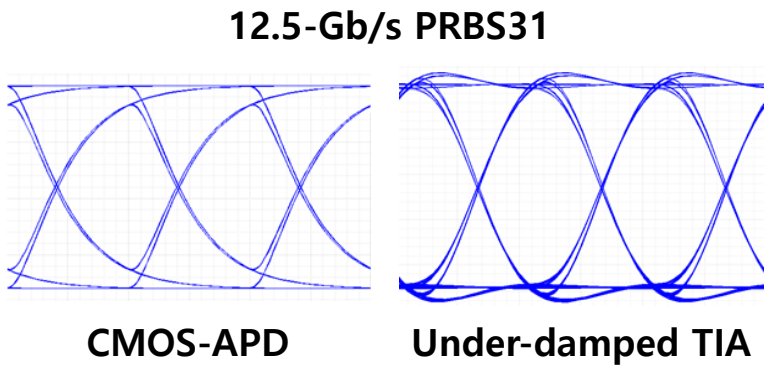


(b)

Fig. 4-5. (a) Block diagram and (b) schematic diagram of the shunt-feedback TIA.



(a)



(b)

Fig. 4-6. (a) Simulated frequency response of the under-damped TIA and (b) transient simulation results of output for CMOS-APD and under-damped TIA.

4.4.2 DC Balancing Buffer and Output Buffer

Delivering photo-generated currents to only one port of two differential TIA input ports induces a DC offset in TIA differential output, which can result bit errors with the decision threshold problem. To solve this problem, a DC-balancing buffer is added. Fig. 4-7 shows the schematic diagram of the designed DC-balancing buffer. Two on-chip low-pass filters and f_T-doubler are used, and to avoid any DC-wander effect, the low cut-off frequency is set to 1 MHz. Output buffers are designed so that they can deliver 200-mVpeak-peak swing to the 50-Ω load of the measurement equipment.

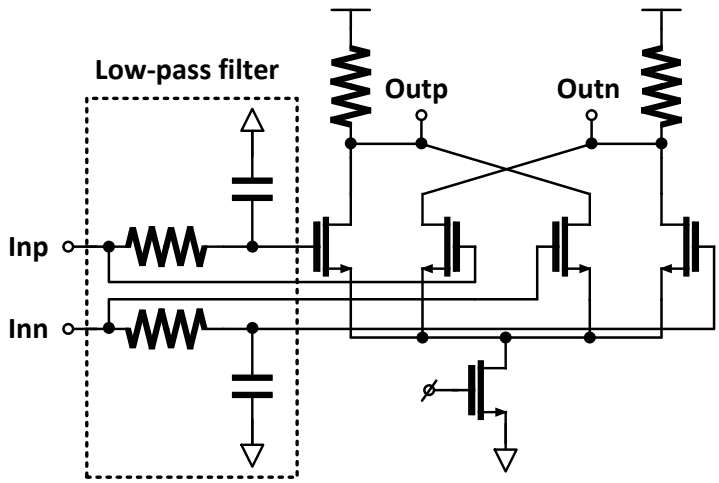


Fig. 4-7. Schematic diagram of the DC-balancing buffer.

4.5 Measurement Results

Fig. 4-8 shows the microphotograph and layout of the fabricated optical receiver. The core size is 0.24 × 0.1 mm^2, and the power consumption of the receiver excluding the output buffer is 13.7 mW with 1.2-V supply voltage.

Fig. 4-9 shows the measurement setup for photo-detection frequency response and optical data detection. All experiments are done on wafer. The 850-nm modulated optical signals are generated by an 850-nm laser diode and a 20-GHz external electro-optic modulator. The modulated optical signals are injected into the optical receiver with lensed fiber. For Measurement, V_{PD} of 10.7 V is used, which provides the optimal reverse bias voltage of 9.7 V to the CMOS APD. For the fabricated optical receiver, the reverse bias voltage of 9.7 V to the APD provides the best BER performance as determined by measurement. For BER evaluation, a 12.5-Gb/s commercial limiting amplifier is used in order to satisfy the input sensitivity requirement of the measurement equipment.

Fig. 4-10 shows the measured and simulated photo-detection frequency responses. The transimpedance gain and 3-dB bandwidth is about 60 dBΩ and 6 GHz, and measured response is well matched with

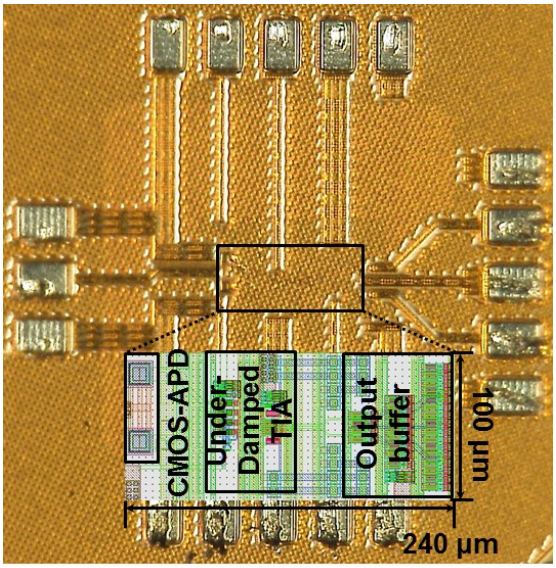


Fig. 4-8. Microphotograph and layout of the fabricated optical receiver with CMOS APD.

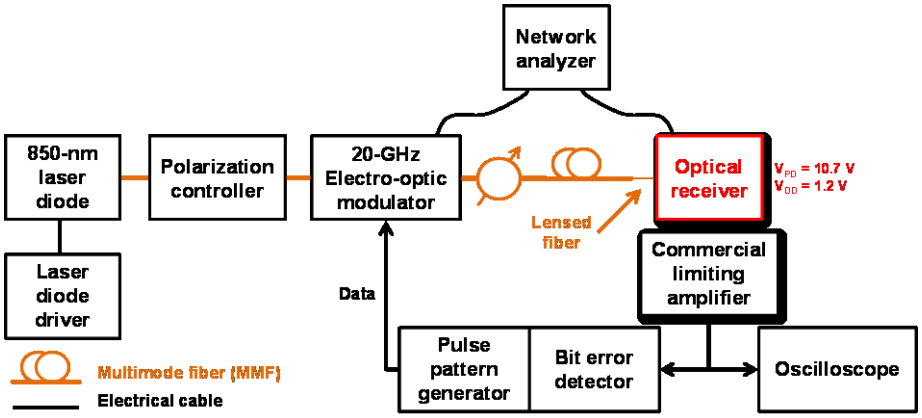


Fig. 4-9. Measurement setup.

simulated response.

Fig. 4-11 shows the measured BER performance for 10- and 12.5-Gb/s input data. For 10 Gb/s, BER of 10^{-12} is achieved with −6-dBm incident optical power for $2^{31}-1$ PRBS input data and −6.5 dBm for $2^{7}-1$ PRBS data. For 12.5 Gb/s, BER of 10^{-12} and 10^{-11} are achieved with −2-dBm incident optical power for $2^{7}-1$ and $2^{31}-1$ PRBS input data, respectively. Fig. 4-12 shows the measured eye diagrams for 10- and 12.5-Gb/s data transmission with −6- and −2-dBm input power.

Fig. 4-13 shows the measured BER performance for various V_{PD}. As shown in the figure, the best BER performance can be achieved at 10.7 V of optimum V_{PD} which provides 9.7 V of V_R. The reason of the worse BER performance is decreased signal amplitude with decreasing V_R and increased avalanche noise with increasing V_R, respectively. Fig. 4-14 shows the measured eye diagrams for 10, 10.7 and 11.1 V of V_{PD}.

Table 4-2 shows the performance comparison of the fabricated optical receiver with previously reported CMOS integrated optical receivers. The table also contains a column, which includes the power consumption and chip area of a LA having 0.076-mm^2 chip area, 12.5-GHz bandwidth [18] so that the fabricated receiver performance can be fairly compared with others. Two different types of figure of merit (FoM) are used in the table. For FoM of gain-bandwidth product per

power, our integrated receiver without the LA shows inferior performance. This is due to the fact the LA provides most of the gain. This is needed when the output signals are delivered outside the circuit, but if the optical receiver is fully integrated including CDR circuits, then LA providing high gain is not necessary. For such an application, FoM for power efficiency defined as mW per Gb/s becomes more relevant. Chip area is another important factor for integrated solutions. For this FoM, our receiver achieves the lowest value of 1.10. The power efficiency FoM becomes 4.17 if we include above-mentioned LA.

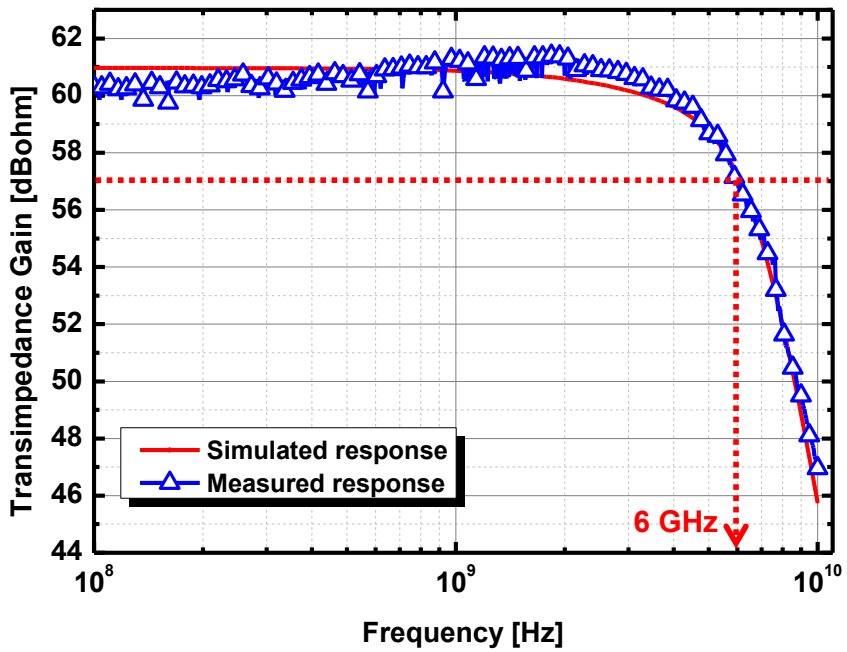


Fig. 4-10. Measured and simulated frequency response.

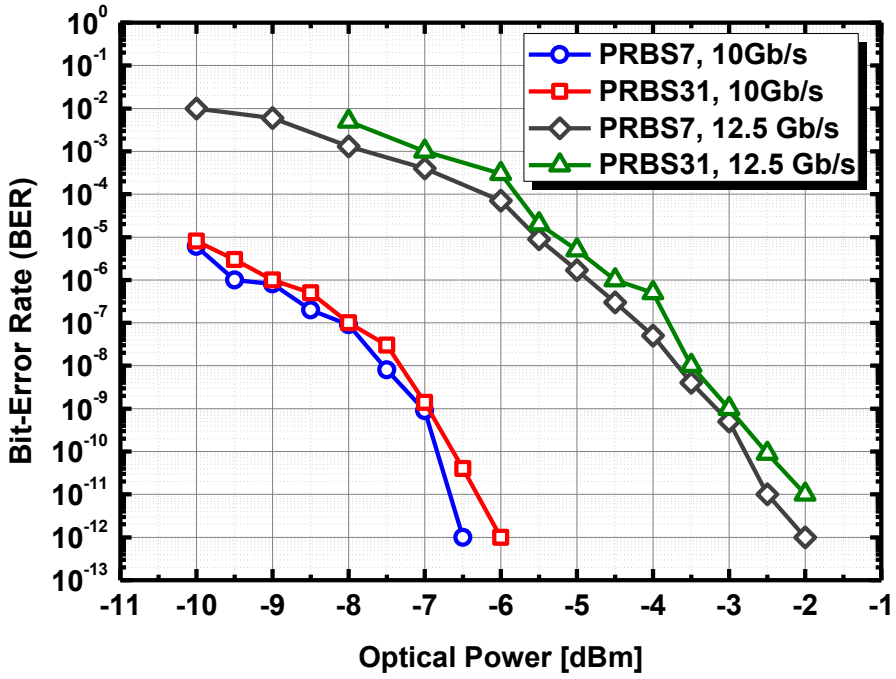


Fig. 4-11. Measured BER performances with various incident optical power for 10- and 12.5-Gb/s data.

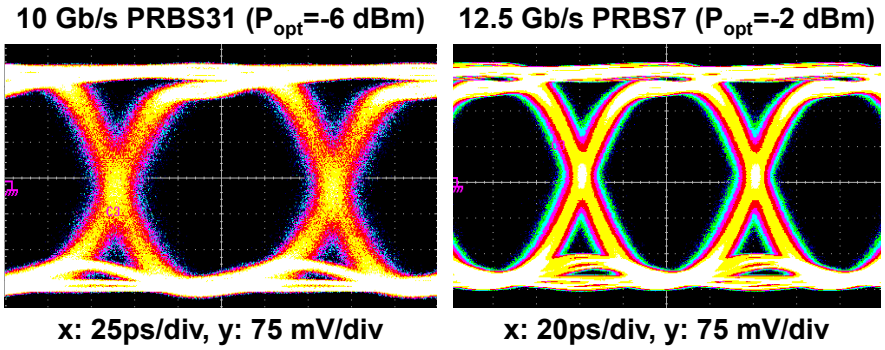


Fig. 4-12. Measured eye diagrams for 10- and 12.5-Gb/s data transmission with −6- and −2-dBm input power.

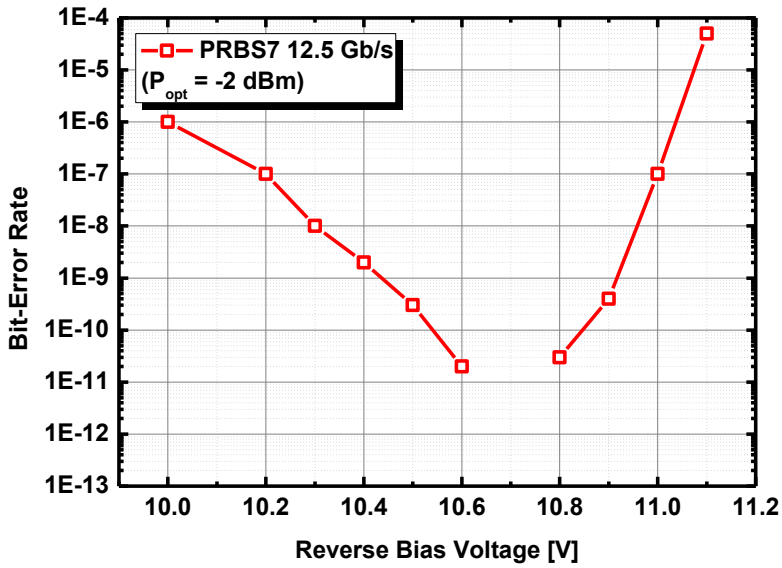


Fig. 4-13. Measured BER performances with various V_{PD}.

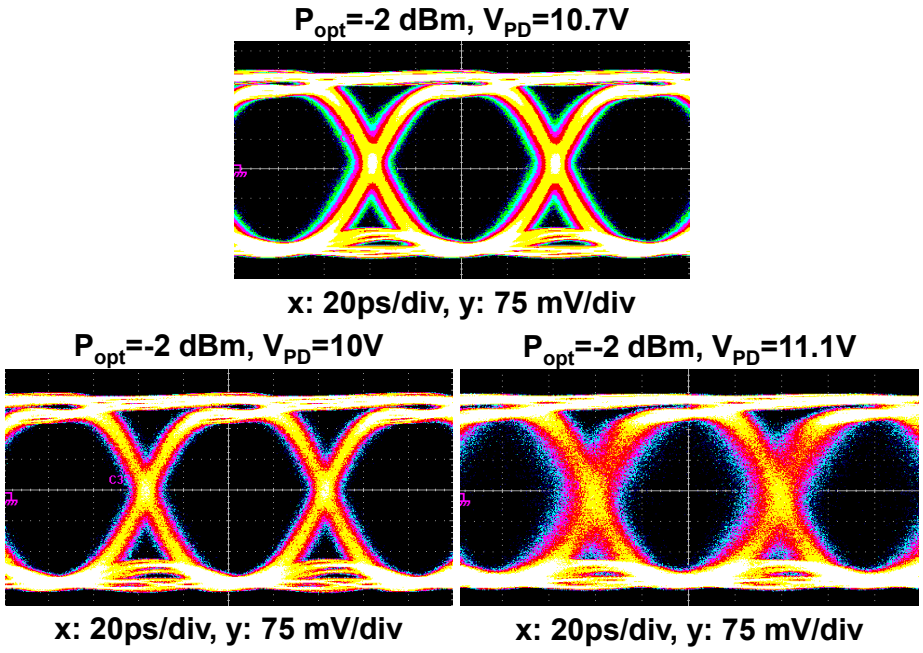


Fig. 4-14. Measured eye diagrams with different V_{PD}.

Table 4-2

Performance comparison of the reported CMOS optical receivers.

	[38] 11' JSSC	[18] 12' JQE	[39] 14' OE	This work		Estimated work
Technology	180-nm CMOS	130-nm CMOS	130-nm CMOS	65-nm CMOS		Photonic BiCMOS
Structure	*SM PD + TIA + LA (Inductors)	APD + TIA + **EQ + LA	*SM APD + TIA + **EQ + LA	APD + TIA (No LA)		APD + TIA + LA (LA is assumed)
Gain [dBΩ]	88	100	104	60		100
Bandwidth [GHz]	5.8	6	8	6		6
Data rate [Gb/s]	10	10	12.5	12.5	10	12.5
BER (PRBS)	10^{-11} (2^7-1)	10^{-12} (2^7-1)	10^{-12} (2^7-1)	10^{-12} (2^7-1)	10^{-12} (2^{31}-1)	N/A
Sensitivity	-6 dBm	-4 dBm	0 dBm	-2 dBm	-6 dBm	N/A
Supply voltage	1.8 V (Circuit) 14.2 V (PD)	1.2 V (Circuit) 10.5 V (PD)	1.3 V (Circuit) 10.5 V (PD)	1.2 V (Circuit) 10.7 V (PD)		1.2 V (Circuit) 10.7 V (PD)
Power	118 mW	66.8 mW	72.4 mW	13.7 mW		52.1 mW
Chip area	0.76 mm^2	0.26 mm^2	0.26 mm^2	0.024 mm^2		0.1 mm^2
***GB/P [Ω/mW]	1235	8982	17512	438		11516
Power efficiency [mW/Gb/s]	11.8	6.68	5.79	1.10	1.37	4.17

*SM PD: spatially-modulated photodetector, **EQ: equalizer, ***GB/P = gain×bandwidth/power dissipation

4.6 Summary

A high-speed CMOS integrated optical receiver in which an under-damped TIA compensates the CMOS-APD bandwidth limitation is realized in 65-nm CMOS technology. With precise circuit model of the CMOS APD and careful design of the under-damped TIA, the bandwidth enhancement can be achieved without any additional equalizing circuits or SM PDs. Also, optical data up to 12.5 Gb/s are successfully detected by fabricated optical receiver. The design strategy employed in fabricated receiver should be valuable for various high-performance electronic-photonic integrated circuit applications, in which careful design of both electronic circuits and photonic devices in an integrated manner can provide better performances with less power consumption and smaller system sizes.

5. A 25-Gb/s Monolithic Optical Receiver with Ge PD

5.1. EPIC Optical Receivers

Optical interconnect solutions based on Si photonics are promising solution as they can fully utilize such advantages as cost-effectiveness and easier integration with electronics, which the mature Si fabrication technology readily provides. In particular monolithic integration of photonic devices with electronic circuits on Si platform can be very powerful solution without parasitic pad capacitance and wire-bonding inductance in hybrid integration. There are already reported impressive monolithic integrated optical receivers [47]-[51], with accurate circuit model of PD, better sensitivity and energy efficiency can be achieved with design optimization.

In this section, accurate Ge-PD circuit model will be utilized, which allows design optimization of sensitivity and energy efficiency. Furthermore the measured optical receiver performances will be demonstrated that they agree very well with simulation results, which the required step for realizing high-performance and cost-effective photonic-electronic integrated circuits with high degree of integration.

5.2. Overall Structure

Fig. 5-1 shows the block diagram of the realized 25-Gb/s integrated optical receiver. It includes on a single platform the first generation Ge PD developed at IHP [52, 53], a transimpedance amplifier (TIA), a single-to-differential converter (SDC), a post amplifier (PA) and an output buffer (OB) based on IHP's 0.25-µm SiGe BiCMOS technology which provides photonic device integration and electronic circuit having f_T and f_{max} of 190 GHz [52]. The TIA has regulated cascode configuration and SDC including low-pass filter is included. PA is also added to amplify the output signal for measurement equipment sensitivity.

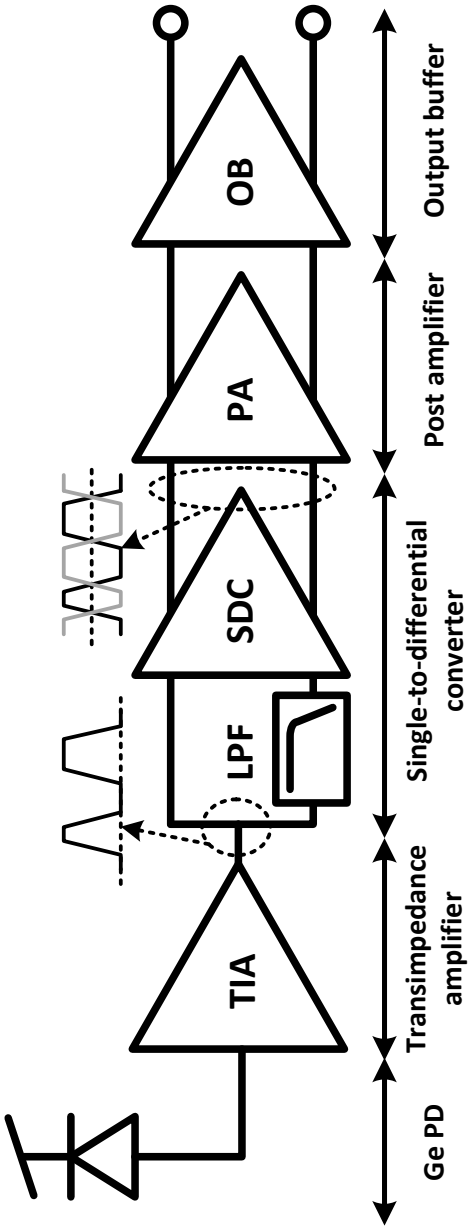


Fig. 5-1. Block diagram of the realized monolithic optical receiver.

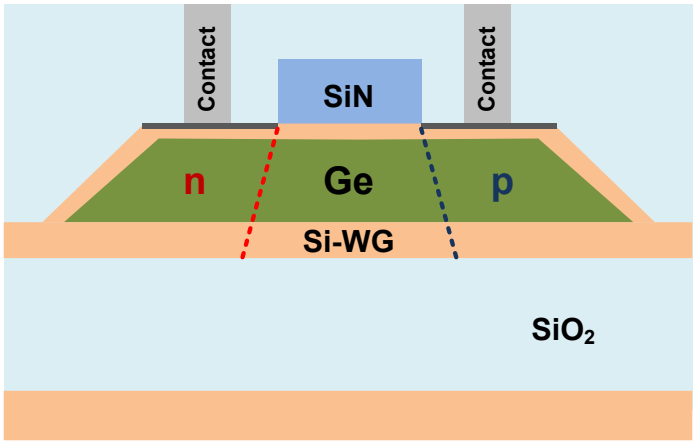
5.3. Ge-Photodetector Equivalent Circuit Model

Fig. 5-2(a) shows the cross section of the waveguide Ge PD integrated in realized optical receiver. It is based on a lateral PIN structure having 3-μm width and 20-μm length. Fig. 5-2(b) shows the measured dark current and photo current with −3-dBm incident optical power. The responsivity of Ge PD is 0.6 A/W and the photodetection 3-dB bandwidth with 50-Ω load is 25 GHz.

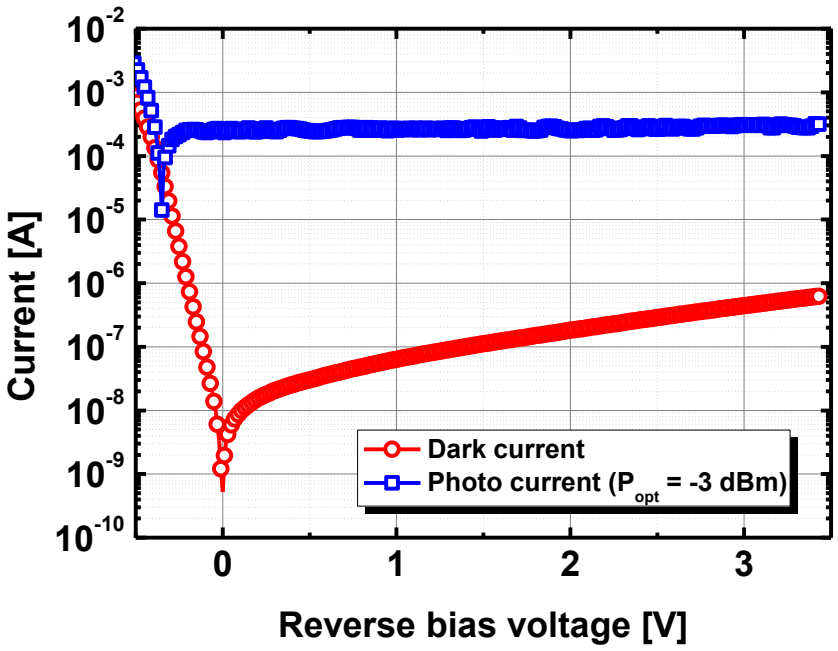
Fig. 5-3(a) shows its equivalent circuit model containing two current sources, which provides better agreement with measurement results [26]. Fig. 5-3(b) graphically shows the frequency response of I_{drift} and I_{diff}, which respectively represent photo-generated carriers undergoing drift and diffusion with corresponding 3-dB frequency f_{3dB_drift} and f_{3dB_diff}. A_{drift} and A_{diff} respectively represent the percentage of photogenerated carriers that undergo drift and diffusion. The model also contains passive elements representing junction (C_J), junction resistance (R_J), series resistance (R_S) and parasitic capacitance (C_{para}). The passive elements of the circuit model can be determined by fitting the measured S22 data and photo-generated carrier can be characterized by fitting photo-detection frequency response.

The extracted numerical values at reverse bias voltage (V_R) of 1 V

and 2 V are given in Table 5-1. Fig. 5-4(a) and (b) show the measured electrical refection coefficients, S22, and photodetection frequency responses, respectively as well as simulated results with realized Ge-PD circuit model for V_R of 1 V. Also, Fig. 5-5(a) and (b) also show the well-fitted simulation and measurement results for V_R of 2 V.

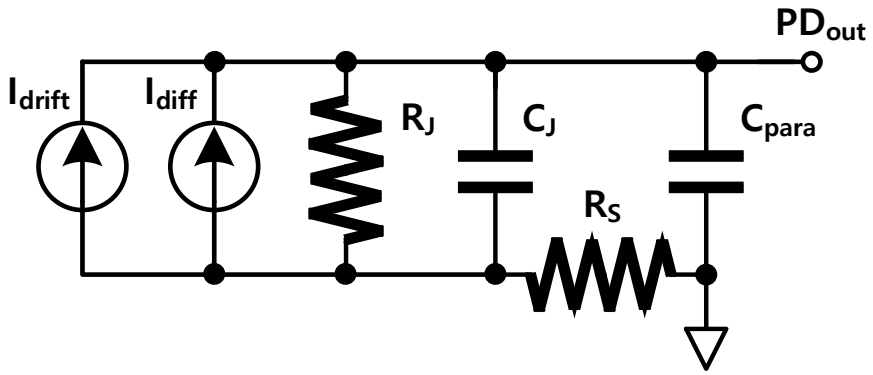


(a)

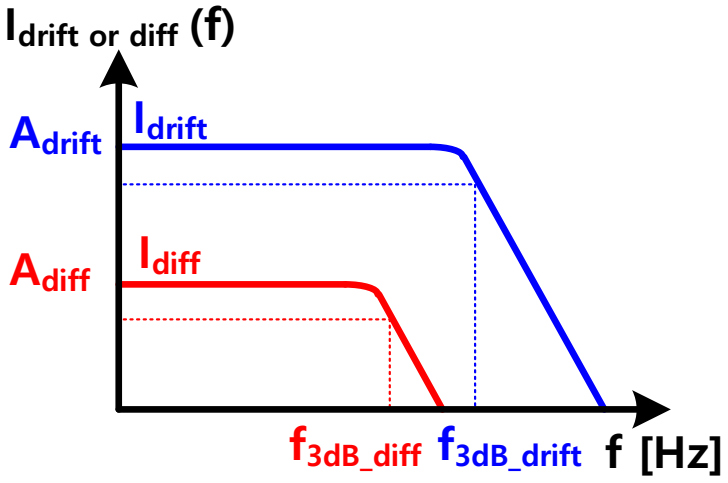


(b)

Fig. 5-2. (a) Structure and (b) measured current characteristics of the integrated Ge PD.



(a)



(b)

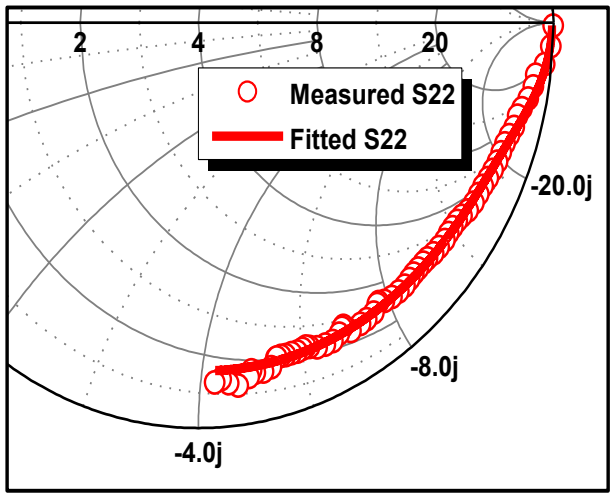
Fig. 5-3. (a) Equivalent circuit model of the Ge PD and (b) frequency response of photogenerated current.

Table 5-1

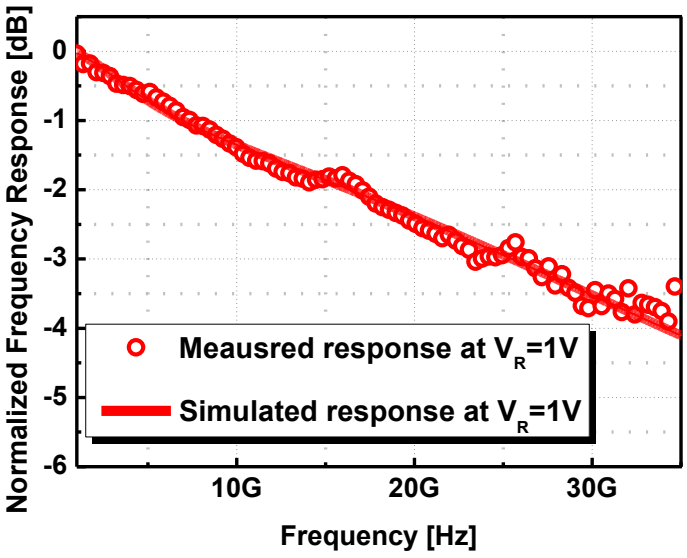
Extracted model parameters of Ge photodetector

Reverse bias voltage = 1 V			
Passive elements		I_{drift} & I_{diff}	
C_J	7 fF	f_{3dB_drift}	34 GHz
R_S	90 Ω	A_{drift}	85.6 %
R_J	100 kΩ	f_{3dB_diff}	4.7 GHz
C_{para}	2.3 fF	A_{diff}	14.4 %

Reverse bias voltage = 2 V			
Passive elements		I_{drift} & I_{diff}	
C_J	5 fF	f_{3dB_drift}	34 GHz
R_S	90 Ω	A_{drift}	89.2 %
R_J	100 kΩ	f_{3dB_diff}	4.7 GHz
C_{para}	2.3 fF	A_{diff}	10.8 %

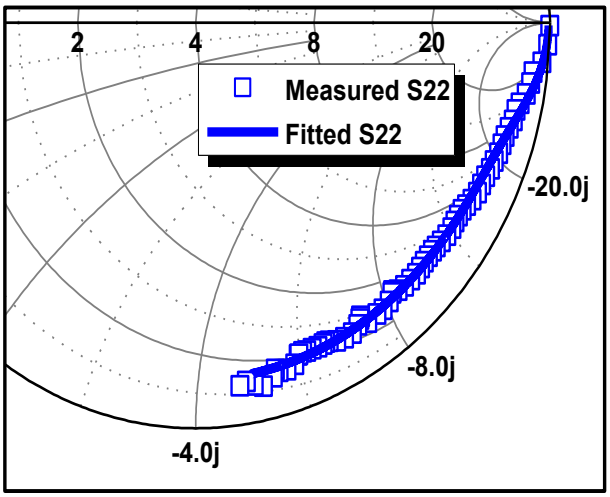


(a)

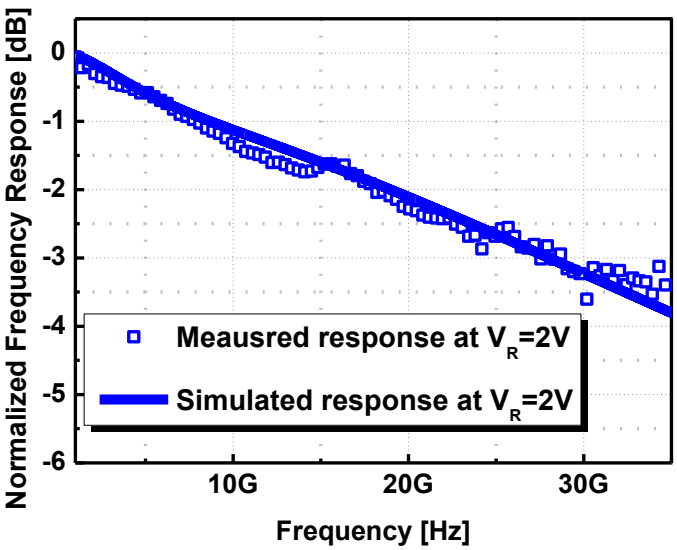


(b)

Fig. 5-4. Measured and simulated (a) S22 and (b) photo-detection frequency response at V_R of 1 V.



(a)



(b)

Fig. 5-5. Measured and simulated (a) S22 and (b) photo-detection frequency response at V_R of 2 V.

5.4. Optical Receiver Circuit

5.4.1 Transimpedance Amplifier (TIA)

One of the TIA configurations for high speed, the regulated cascode configuration (RGC) is used for the fabricated TIA, which has advantages of low input impedance and high gain-bandwidth product. Fig. 5-6 shows the schematic diagram of the designed RGC TIA. The input impedance (Z_{in}) of RGC TIA can be expressed as

$$Z_{in} = \frac{1}{g_{m1}(1+g_{m2}R_B)}, \tag{5.1}$$

where g_{m1} and g_{m2} are transconductance of SiGe HBTs Q1 and Q2. The transfer function of RGC TIA is given as

$$Z_T(s) = \frac{R_L}{\left[1+s\frac{C_{PD}+C_{in}}{g_{m1}(1+g_{m2}R_B)}\right]\left[1+sR_L(C_L+C_{out})\right]}, \tag{5.2}$$

where C_{PD} is the capacitance of photodetector and C_{in} and C_{out} are input and output capacitance of RGC TIA. C_L is the load capacitance due to the subsequent stage. According to Eq. (5.2), there are mainly two poles affecting bandwidth from input and output of RGC TIA. Also, the low frequency transimpedance gain is R_L.

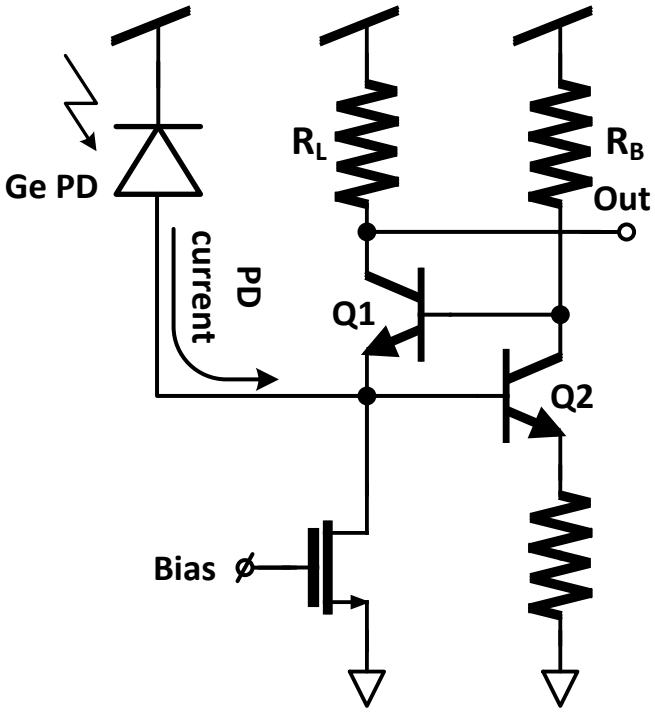


Fig. 5-6. Schematic diagram of the designed RGC TIA.

5.4.2 Single-to-Differential Converter (SDC)

The single-to-differential converter is included in fabricated optical receiver to convert single ended output of the TIA into differential signal. Fig. 5-7 shows the schematic diagram of the designed SDC. Emitter degeneration is used for gain-bandwidth enhancement. Also, it contains on-chip low-pass filter and the DC delivering circuit in order to eliminate DC offset in the TIA. The low cut-off frequency is set to 2 MHz to avoid any DC-wander problem for 25-Gb/s PRBS $2^{31}-1$ data transmission.

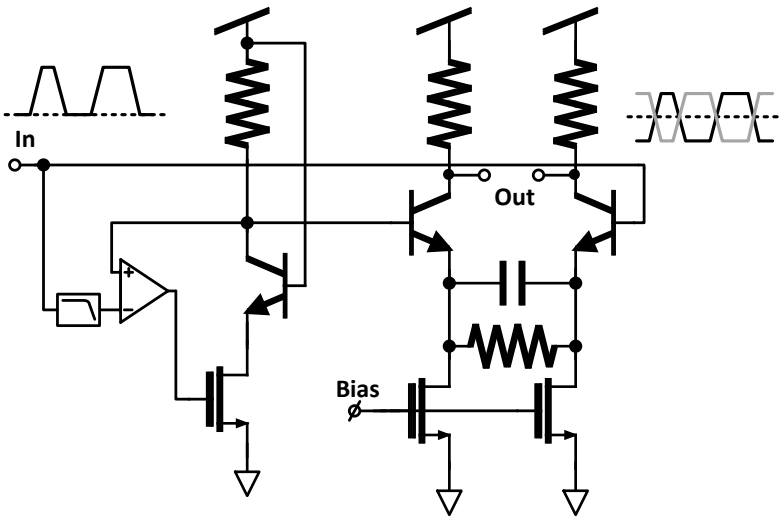


Fig. 5-7. Schematic diagram of the designed SDC.

5.4.3 Post Amplifier (PA) and Output Buffer

The post amplifier is designed to amplify SDC output signals for achieving 200 mV peak-to-peak with −10-dBm input optical power. Fig. 5-8 shows the schematic diagram of the designed PA. The PA has 2-stage amplifier with active feedback for large gain-bandwidth product, and emitter followers are included for loading following stage. The output buffer is used for driving 50-Ω load for measurement equipment.

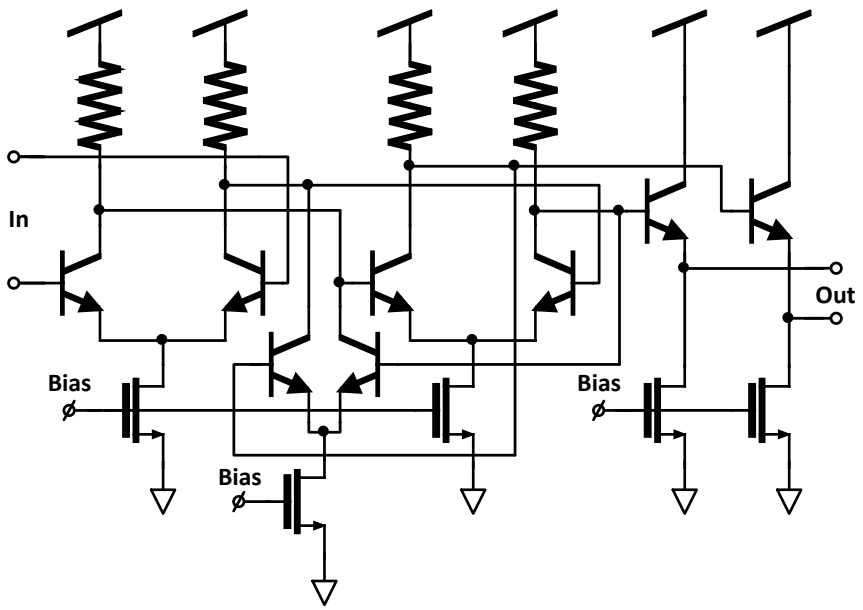
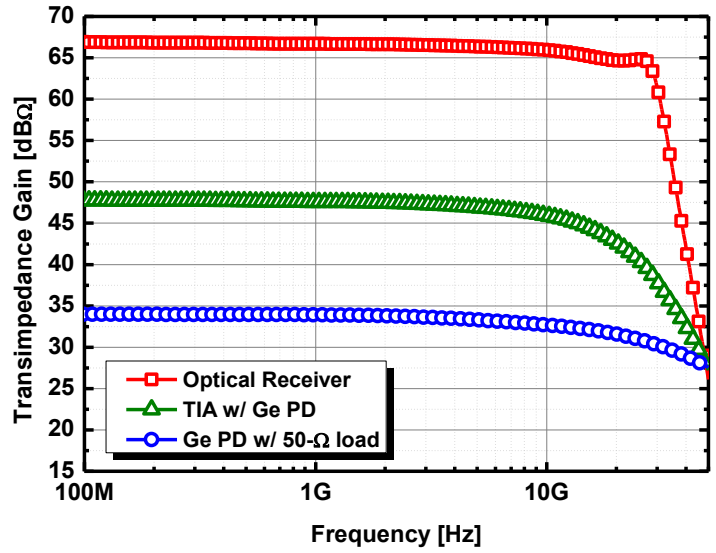


Fig. 5-8. Schematic diagram of the designed PA.

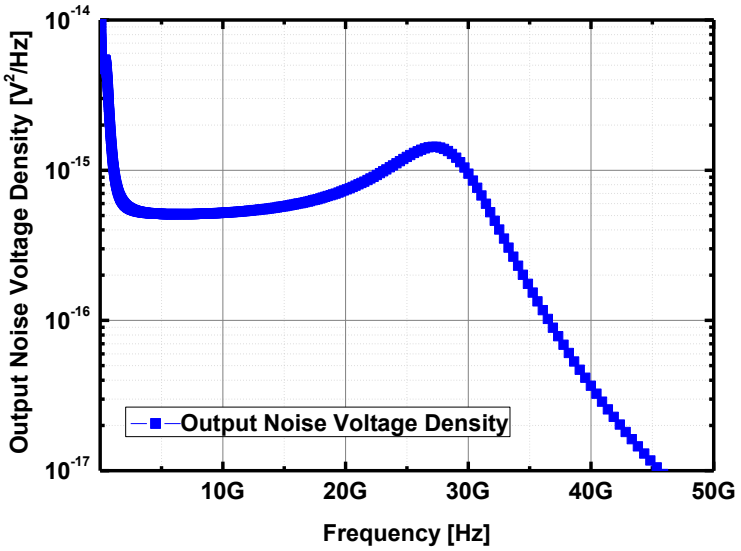
5.4.4 Simulation Results

Fig. 5-9(a) shows the simulated frequency response for Ge PD circuit model with 50-Ω load, TIA with Ge-PD circuit model and the entire optical receiver. As shows in the figure, TIA provides transimpedance gain of 48 dBΩ and 3-dB bandwidth of 20 GHz including the Ge-PD circuit model. The entire optical receiver has transimpedance gain of 67 dBΩ and 3-dB bandwidth of 17 GHz resulting in SDC and PA after TIA

Fig. 5-9(b) shows the simulated output noise voltage density. The integrated output noise voltage from 10 MHz to 50 GHz is 29.3 μV_{rms}^2, which corresponds to input referred noise current of 4.91 μA_{rms}.



(a)



(b)

Fig. 5-9. Simulated (a) photo-detection frequency response and (b) output noise voltage density of the optical receiver with Ge PD model.

5.5. Measurement Results

Fig. 5-10 shows the microphotograph of the fabricated optical receiver. Its core size is 0.38 × 0.2 mm^2, and the power consumption of the optical receiver is 37 mW with 2.5-V supply voltage including the output buffer.

Fig. 5-11 shows the measurement setup for optical data detection. All experiments are done on wafer. The 1550-nm modulated optical signals are generated by a 1550-nm tunable laser source and a 40-GHz external mach-zehnder modulator. The modulated optical signals are injected into the optical receiver through grating coupler. For measurement, V_{PD}s of 2.5- and 3.5-V are used, which provides the V_R of 1- and 2-V to the Ge PD, respectively.

Fig. 5-12(a) shows the simulated and the measured bit-error rate (BER) at V_R of 1 V with 20- and 25-Gb/s $2^{31}-1$ PRBS data. The simulated results are fitted with the BER estimation given as [35]

$$\mathrm{BER}=\frac{1}{2}\,erfc\left(\frac{\alpha\cdot\mathrm{SNR}}{2\sqrt{2}}\right), \tag{5.3}$$

where SNR is the signal-to-noise ratio and α represents penalties due to non-idealities caused by the transmitter and electrical cables in the measurement and bandwidth penalty [54]. In this simulation SNR is calculated with photo current for signal and circuit simulation results

for noise. For the noise value, only the circuit noise determined from circuit simulation is considered since the Ge-PD noise is much smaller. As a result of fitting by Eq. (5.3) to the measured data, α is estimated as 0.94 for 20 Gb/s and 0.75 for 25 Gb/s. For 20-Gb/s operation, BER of 10^{-13} is achieved for $2^{31}-1$ PRBS input with incident power of −11.5 dBm and, for 25-Gb/s operation, BER of 10^{-12} is achieved with incident optical power of −10 dBm. Fig. 5-12(b) shows 20- and 25-Gb/s simulated and measured eye diagrams at selected BER values. As shown in the figure, simulated and measured results for BER performances and eye diagrams are well matched.

Fig. 5-13(a) and (b) also show simulated and measured BER performance and eye diagrams at V_R of 2 V with 20- and 25-Gb/s $2^{31}-1$ PRBS data. In this case, α is estimated as 0.95 for 20 Gb/s and 0.76 for 25 Gb/s. For 20-Gb/s operation, BER of 10^{-14} is achieved for $2^{31}-1$ PRBS input with incident power of −11.5 dBm and, for 25-Gb/s operation, BER of 10^{-12} is achieved with incident optical power of −10 dBm. As shown in Fig. 5-13(a) and (b), BER performances and eye diagrams for V_R of 2 V are also well matched.

Table 5-2 shows the performance comparison of fabricated optical receiver with previously reported 25-Gb/s monolithically integrated optical receivers with Ge PD. As shown in the Table, the fabricated

optical receiver achieves higher sensitivity and better energy efficiency. Furthermore small foot print of 0.38×0.2 mm^2 can be achieved without using on-chip inductors.

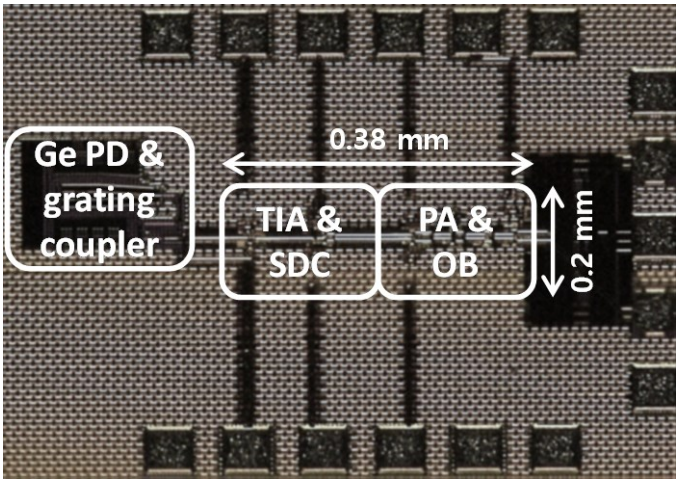


Fig. 5-10. Microphotograph of the fabricated monolithic optical receiver with Ge PD.

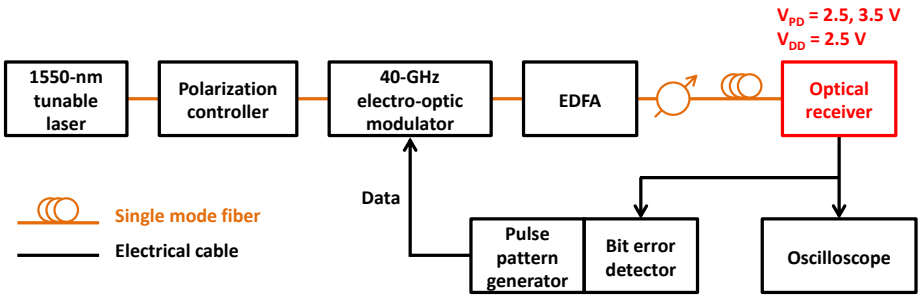
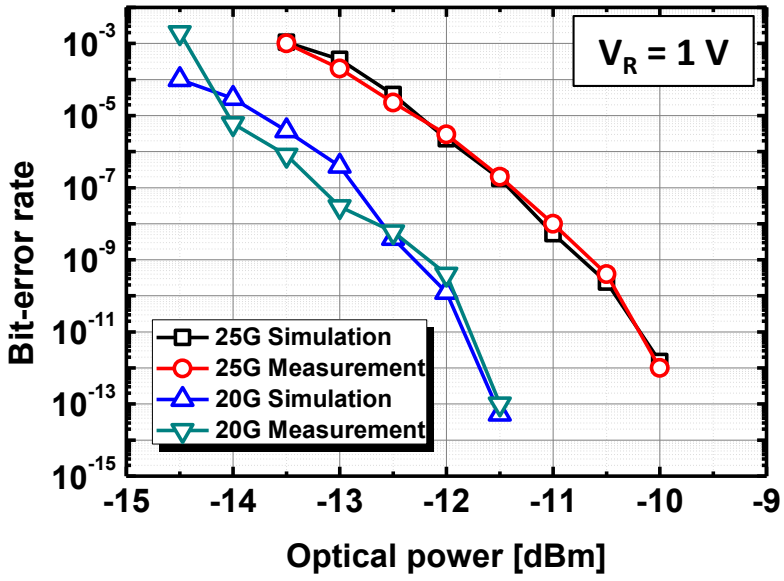
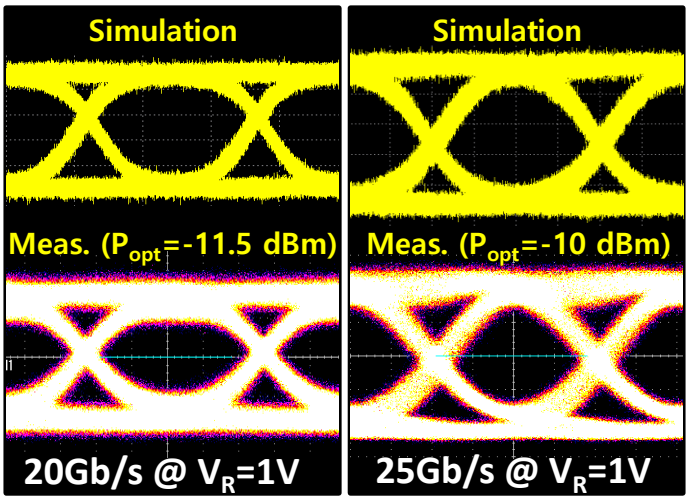


Fig. 5-11. Measurement setup.

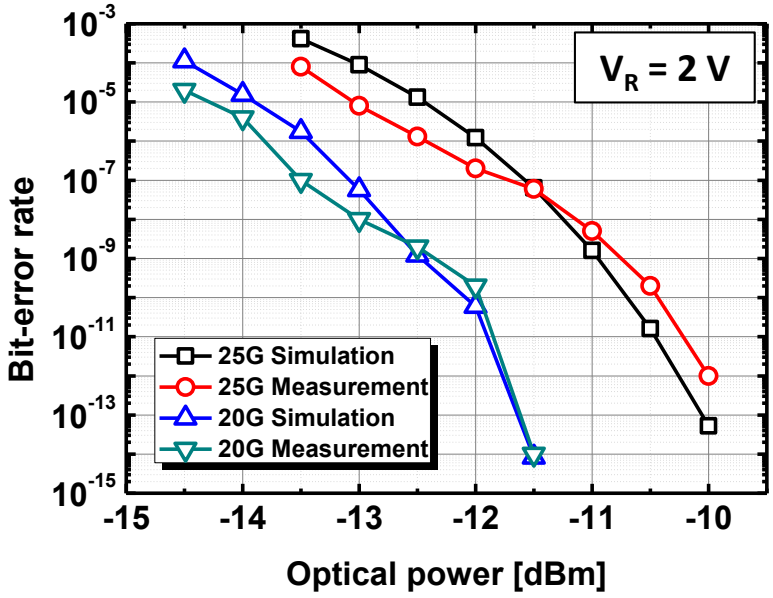


(a)

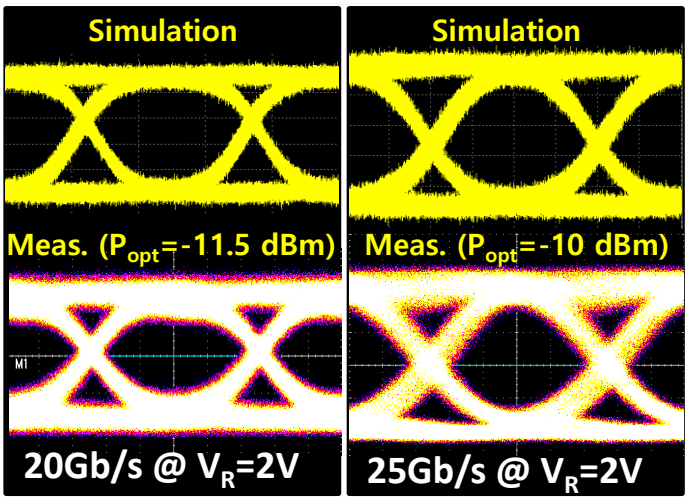


(b)

Fig. 5-12. Simulated and measured (a) BER performances and (b) eye diagrams at selected BER points for V_R of 1 V.



(a)



(b)

Fig. 5-13. Simulated and measured (a) BER performances and (b) eye diagrams at selected BER points for V_R of 2 V.

Table 5-2

Performance comparison of the reported 25-Gb/s optical receiver monolithically integrated with Ge PD

	[47] 14' OFC	[48] 12' JSSC	[50] 13' OFC	This work
Technology	Photonic BiCMOS	130 nm SOI CMOS	90 nm CMOS	Photonic BiCMOS
Gain [dBΩ]	71	67	-	67
Data rate [Gb/s]	25	25	25	25
BER	10^{-3}	10^{-12}	10^{-12}	10^{-12}
Sensitivity [dBm]	-15	-6	-6	-10
Output swing [mV]	200	200	-	200
Power [mW]	57	48	-	37
Efficiency [pJ/bit]	2.28	1.92	-	1.5

5.6. Summary

A 25-Gb/s monolithic optical receiver containing a Ge PD is realized with IHP's photonic BiCMOS technology. With an accurate Ge-PD equivalent circuit model and careful design, the fabricated optical receiver achieves much improved performances with sensitivity of −10 dBm for 25-Gb/s $2^{31}-1$ PRBS data detection and energy efficiency of 1.5 pJ/bit. In addition, simulated BER performances and eye diagrams are demonstrated that they are well matched to the measurement results.

6. Conclusion

In this dissertation, high-speed Si optical receivers are realized with Ge PD and CMOS APD for 1550-nm and 850-nm optical interconnect applications. The realized optical receivers contain photodetector, transimpedance amplifier, post amplifier and output buffer.

For these optical receivers, design optimizations are achieved considering characteristics and connection of the PDs. For monolithic integration, DC characteristics and frequency responses of the CMOS APD and Ge PD are investigated and accurate circuit models of the PDs are developed. For hybrid integration, wire-bonding inductance is characterized and modeled. With circuit models above, performances of the optical receivers can be optimized as well as enhanced with precisely simulated results for photonic-electronic integrated circuit. In addition, simulation results with circuit models of the photodetectors are verified with measurement results of eye diagram and bit-error rate.

As can be seen in chapter 3, 4 and 5, the fabricated optical receivers can achieve impressive performances with data rate, power efficiency and chip area. Also, it is expected that the used design method using equivalent circuit model and connection of the PDs can be expanded to other integrated optical receivers with other PDs.

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Abstract (In Korean)

실리콘 집적 광 수신기의 대역폭 및 SNR 최적화

본 논문은 고속 실리콘 기반 모놀리식과 혼성 집적 광 수신기들을 디자인 최적화하는 연구를 하였고 제작하였다. 제작된 광 수신기들은 정확한 광 검출기와 혼성 집적에 쓰이는 본딩 와이어의 인덕턴스의 등가회로 모델을 이용한 설계 최적화가 되었다. 본 설계 최적화는 더 나은 성능을 보일 뿐 아니라 속도 제약을 가진 광 검출기의 속도 보상을 가능하게 하였다. 정확한 광 검출기의 등가회로 모델을 개발하기 위해 광 검출기의 DC 및 주파수 응답 특성이 측정 및 분석되어 적용 되었다. 또한, 본딩 와이어의 언덕턴스가 시뮬레이션과 측정결과를 통해 검증 되었다.

디자인 최적화된 혼성 집적 광 수신기 회로가 제작 되었다. 이 수신기는 혼성 집적으로 인한 본딩 와이어와 패드의 기생 캡과 인덕턴스를 고려하여 설계 되었다. 이 수신기 회로에는 오프셋 제거 회로를 포함한 전치 증폭기와 후치 증폭기, 출력 버퍼를 포함하고 있다. 제작된 광 수신기 회로는 광 검출기 등가 회로를 이용하여 검증 되었다. 측정된 이득과 대역폭은 각각 84 dBΩ과 12 GHz이다. 제작된 광 수신기를 이용하여 20-Gb/s PRBS31 광 신호를 성공적으로

전송하였다 (BER < 10^{-12}). 칩 면적은 0.5 mm × 0.44 mm 이며, 전력 소모는 1.2 V 전원에서 약 84 mW이다.

표준 65-nm CMOS 공정을 이용하여 모놀리식 집적 광 수신기를 제작하였다. 이 수신기에는 CMOS 아발란치 광 검출기와 under-damped 전치 증폭기가 집적 되어 있다. Under-damped 전치 증폭기는 CMOS 아발란치 광 검출기의 제한된 속도를 보상하고 기존에 발표된 광 수신기들과 비교 하였을 때 적은 파워와 나은 광 민감도를 가능하게 한다. 제작된 광 수신기를 이용하여 10-Gb/s PRBS31과 12.5-Gb/s PRBS7 광 신호를 성공적으로 전송 하였고 (BER < 10^{-12}), 측정된 광 민감도는 각각 -6 dBm과 -2 dBm이다. 칩 면적은 0.24 mm × 0.1 mm 이며, 전력 소모는 1.2 V 전원에서 약 84 mW이다.

Photonic BiCMOS 공정을 이용하여 고성능 모놀리식 집적 광 수신기를 제작하였다. 이 수신기에는 도파관 형태의 Ge 광 검출기, 전치 증폭기, 단일-차동 변환 회로, 후치 증폭기 및 출력 버퍼가 한 칩에 집적되어 있다. 제작된 광 수신기를 이용하여 25-Gb/s PRBS31 광 신호를 성공적으로 전송 하였으며 (BER < 10^{-12}), 측정된 광 민감도는 -10 dBm이다. 제작된 광 수신기의 전력 효율은 1.5 pJ/bit이다. 또한, Ge 광 검출기의 등가 회로 모델을 이용한 광 수신기의 아이다이어그램과 BER 시뮬레이션으로 측정결과를 예측하였다.

본 논문에서 제작된 모놀리식 및 혼성 집적 광 수신기들은 광

검출기들과 그들의 연결을 이해 및 정확한 등가 회로 모델을 구현하였고, 이를 이용하여 디자인 최적화하였다. 이 설계 방법들은 디자인 최적화된 광 수신기의 구현 방법으로 사용 가능할 것으로 예상된다.

핵심 단어: 아발란치 광 검출기, 비트 에러율, 등가 회로 모델, 혼성 집적, 리미팅 증폭기, 모놀리식 집적, 광 연결, 광 수신기, 광전자 회로, 광 검출기, 주파수 특성, 후치 증폭기, 전력 효율, 실리콘 포토닉스, 신호 대 잡음비, 전치 증폭기, 본딩 와이어 인덕턴스.

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[1] **Hyun-Yong Jung**, Jeong-Min Lee, Stefan Lischke, Dieter Knoll, Lars Zimmermann, and Woo-Young Choi, "A 25-Gb/s Monolithic Optical Receiver with Improved Sensitivity and Energy Efficiency," *submitted to IEEE Photonics Technology Letters*

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