Temperature Stabilization Circuits for Optical Modulators

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Temperature Stabilization Circuits for Optical Modulators

by

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Table of Contents

List of Tables

List of Figures

Abstract

Temperature Stabilization Circuits for Optical Modulators

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As the demand for commercial data centers and mobile devices are rapidly increasing, the application of high-bandwidth optical interconnects are gradually expanding from medium-and-long distance communications to short reach interconnects. There is a great interest in Si optical modulators for short-reach interconnect applications due to they have great advantage of being easily compatible with Si circuitry. However, the Si optical modulators have a serious drawback in that its

characteristics are easily influenced by the temperature. For a solution, this dissertation focuses on demonstrations of indispensable control circuits for practical use of optical modulators.

A new integrated Mach-Zehnder modulator (MZM) bias control circuit realized in 0.25-μm BiCMOS technology is demonstrated for 3-Gb/s data modulation of a commercial 850-nm MZM. This control circuit monitors the optical modulation amplitude (OMA) of the MZM output optical power and automatically searches the optimum MZM bias voltage having maximum OMA and maintains it there.

A new improved integrated MZM bias control circuit realized in 28nm CMOS technology is demonstrated for 25-Gb/s data modulation of a 1550-nm MZM. This control circuit monitors the OMA and average power of the MZM output optical power and automatically searches and maintains it with two-step approach, which provides improved power consumption and initial acquisition time.

A new Si micro-ring modulator (Si MRM) wavelength (λ) stabilization IC realized in 0.25-μm BiCMOS technology is demonstrated for 25-Gb/s data modulation of a 1550-nm Si MRM. This circuit monitors the OMA of the Si MRM output optical power and automatically searches the optimum heater voltage having maximum OMA and maintains it there with low-power strategy.

These demonstrated ICs will be expected to have great potential of monolithic integration with Si optical transmitter based on Si MZM or Si MRM.

Keywords**:** Mach-Zehnder modulator (MZM), Si micro-ring modulator (Si MRM), bias controller, wavelength (λ) stabilization circuit, optical modulation amplitude (OMA), photodetector, trans-impedance amplifier (TIA), integrated circuit (IC), monolithic integration, optical interconnect, Si photonics, control circuit, digital control.

1. Introduction

1.1. Optical Interconnect and Silicon (Si) Photonics

Interconnects between system to system have improved through many studies over the last several decades. From short distance of the chip-to-chip and the board-to-board interconnects to long distance of the trans-ocean telecommunications, several application data has been transmitted through electrical and optical media [1]. For the long-distance transmission, optical media have been widely used due to their wide bandwidth and low attenuation while for the short distances copper media have been widely used because they are easily compatible with Si circuits [2, 3].

Nowadays, the exploding data traffic from the various smart devices cause huge demand for high-speed interconnects of many systems including data centers or communication routers like figure 1-1. Although photonic devices had not been easy to integrate with Si circuitry, the optical interconnect has been actively researched in recent years to alternative of many electrical interconnect with the development of Si photonics [4, 5].

In Si photonics technology, optical waveguides can be easily

integrated in Si wafer in few hundred nm width based on the difference of refractive index between Si and Si oxide. Not only waveguides but also many photonic devices such as modulators, filters, and couplers can be integrated on Si wafer in compact size and moreover with widespread Si circuits like figure 1-2. This integration circuit between photonic and electronic device is called by Si electronic-photonic integrated circuit (EPIC). It has huge advantages of saving area and simplifying interface between electrical-optical devices, consequently, it is very cost-effective way and researched actively [6].

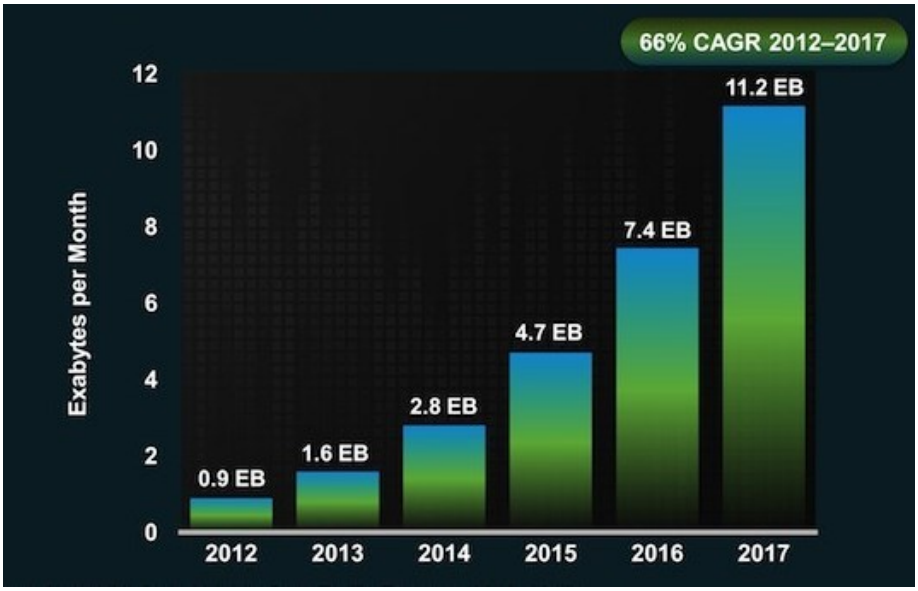


Figure 1-1. Global mobile data traffic growth [10]

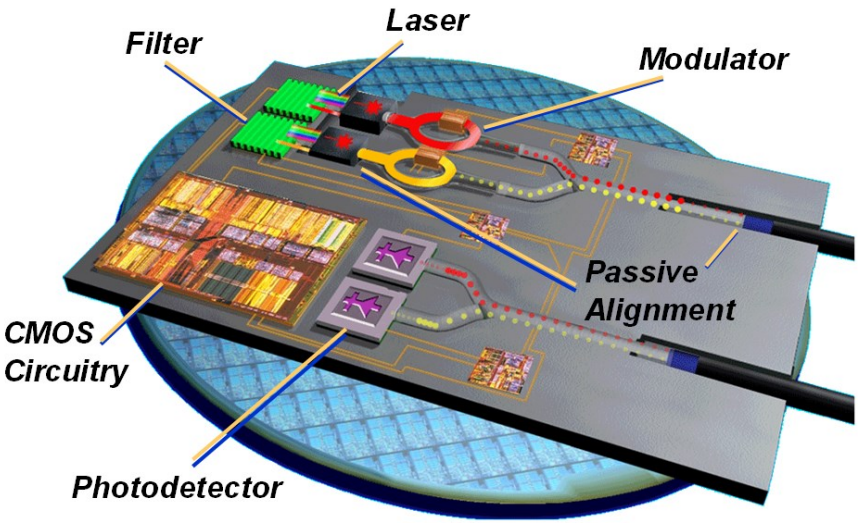


Figure 1-2. Conceptual structure of Si photonics [11]

1.2. Instability of Optical Modulator in Transmitter

As described in previous chapter, Si photonics technology has a potential of integration between photonic devices and electrical circuits into a single chip. Moreover, in addition to this monolithic integration, the Si photonics has a great advantage that the electrical circuit can help optical devices as calibrating their several intrinsic problems. In this dissertation, using the smart electrical circuit, we propose and demonstrate a new algorithm to calibrate and control the environmental dependent problem of optical modulator. Prior to the text, we will explain temperature issue of optical modulator in Si photonics with optical transmitter system.

Figure 1-3 shows simple block diagram of general high-speed optical transmitter system. The optical modulator converts high-speed electrical signal to optical signal using the light source from the laser. The modulator driver applies the electrical signals to load of optical modulator with clean eye. Even though there is a way of direct modulation of the laser without modulator, the Si photonics does not provide intrinsic laser sources yet. In Si photonics technology, consequently, the optical modulator with externally provided laser source is essential to the optical transmitter system.

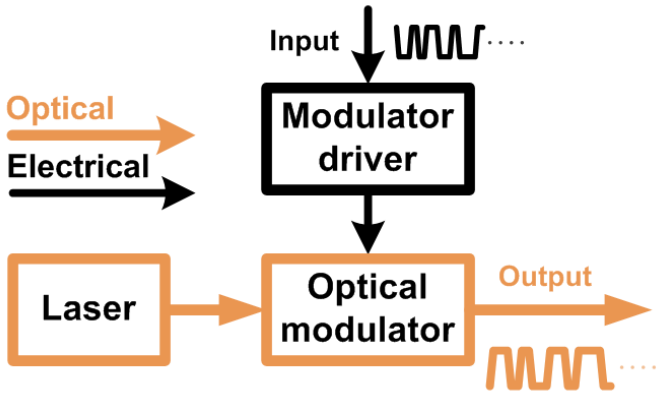


Figure 1-3. Conceptual block diagram of optical transmitter

When we design this optical transmitter, design environments of the electrical circuit and the optical modulator are quite a different. In case of electrical circuit designs, environment variables including process and temperature can be considered based on fine-modeled process-design-kit and even their intrinsic problems can be calibrated by their sub-circuits. The electrical load of the optical modulator can be also precisely modeled and used for design optimization as well. However, in case of the optical device designs, since it is intrinsically a passive element unlike the electric circuits, it is not easy to predict problems and calibrate them to optimize operating point. This would be a critical problem in practical use of optical modulator. There are two optical modulators of Mach-Zehnder modulator (MZM) and micro-ring modulator (MRM) which are typically researched for optical

transmitter system. Now, we introduce how the problems affect their characteristics and operating points.

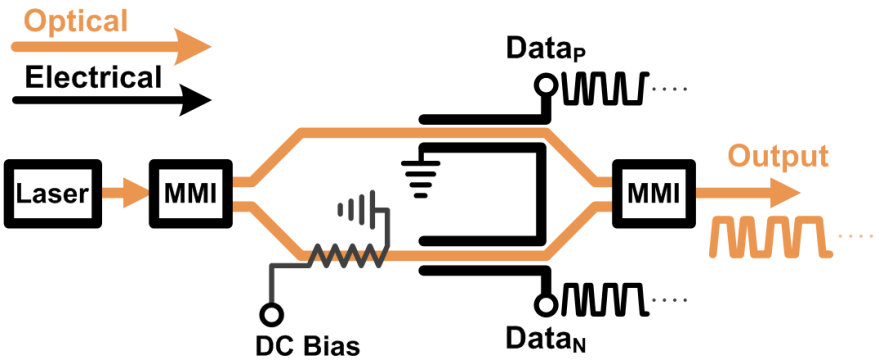


Figure 1-4. Basic structure of Mach-Zehnder modulator (MZM)

Figure 1-4 shows a conceptual structure of MZM. As a traditional optical modulator, MZM has been widely used and studied in optical systems. As shown in the figure, MZM has a structure of two power-split optical waveguides, which are power-combined as one output waveguide. When electric fields are applied to each split waveguide, the refractive index of each waveguide is changed based on Pockels and Kerr effect, the phases of each optical signal are changed, and the power-combined optical intensity can be expressed by below equation. P_0 and ϕ are laser power and phase change at modulate arms, respectively [7].

$$E_{\text{output}} = \frac{E_0 \cdot (e^{-j(\omega t+\phi)} + e^{-j(\omega t-\phi)})}{2}$$
$$P_{\text{output}} = P_0 \cdot (1+\cos\phi) \cdot e^{-j\omega t} \quad (1.1)$$

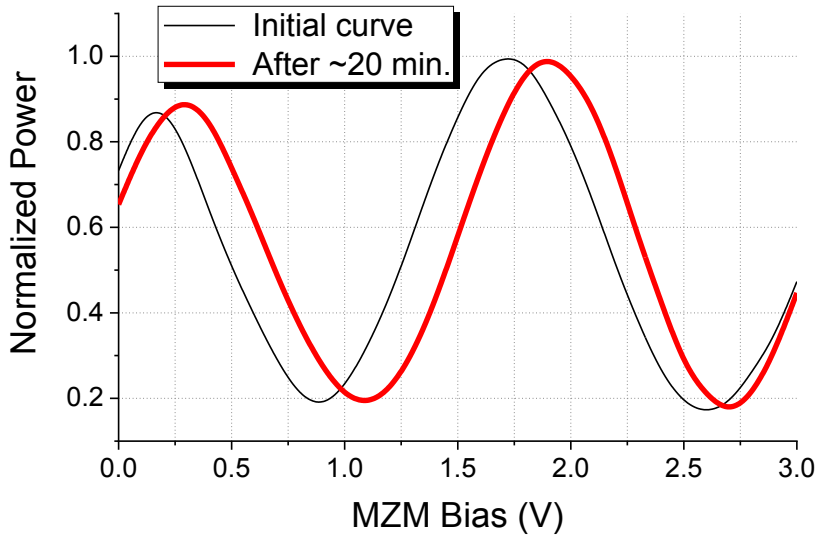


Figure 1-5. Normalized optical power transfer curve of LiNbO3 MZM

However, when the environment factors are changed extrinsically or intrinsically, operating condition drifts due to their temperature, humidity, asymmetric arms, and high power of optical source. Figure 1-5 shows thermal drift phenomenon of the DC transfer curves of commercial $LiNbO_3$ MZM with time. In order to calibrate this unpredicted DC drift, the control circuit for MZM DC bias, called by a bias controller, has been studied for practical use and it will be discussed in next chapter [8].

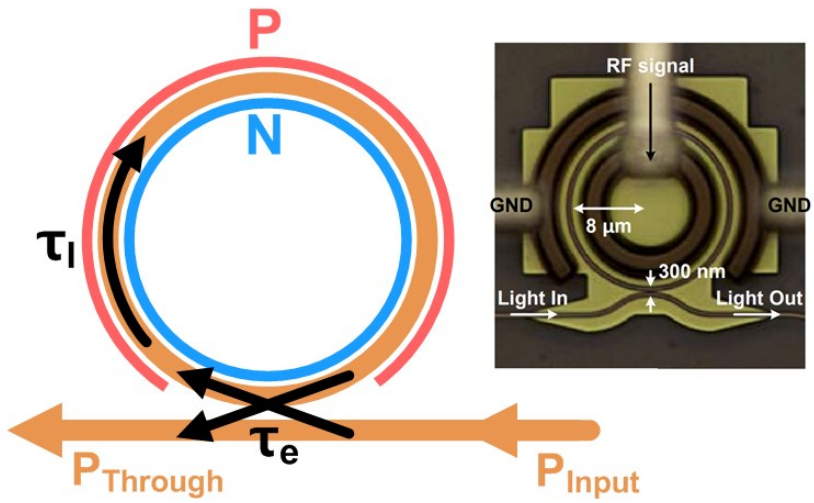


Figure 1-6. Basic structure of Si micro-ring modulator

The figure 1-6 shows a basic Si MRM structure [9]. When we use Si waveguide design process, a compact ring resonator with a radius of few μm can be designed. Due to the advantages of its small size and consequent light electrical load, the MRM has been studied extensively as optical modulator. This resonator has a transmission spectrum having a resonance wavelength as below equation (1.2) which is based on a coupled-mode theory [10], where τ_e, τ_l represent decays due to coupling and propagation loss, respectively, and ω_{res} represents angular frequency of resonance. In equation (1.4), c, m, L, η_{res}, and λ_{res} represent velocity of light in vacuum, resonance mode number, ring circumference, refractive index at resonance, and its wavelength, respectively.

$$\frac{P_{Through}}{P_{in}}(\lambda)=\frac{(\omega-\omega_{res})^2+(\tau_l^{-1})^2}{(\omega-\omega_{res})^2+(\tau_e^{-1}+\tau_l^{-1})^2} \tag{1.2}$$

$$\omega=\frac{2\pi}{\lambda} \tag{1.3}$$

$$\omega_{res}=\frac{2\pi}{\lambda_{res}}=\frac{2\pi mc}{\eta_{res}L} \tag{1.4}$$

Figure 1-7 shows conceptual modulation diagram with MRM spectra near resonance wavelength. If voltage is applied to the waveguide of ring resonator, its refractive index (η_{res}) is changed based on Pockels and Kerr effects, where the resonance wavelength (λ_{res}) red-shifts. Consequently, this phenomenon can be used for optical modulation at the specific wavelength (λ_{mod}).

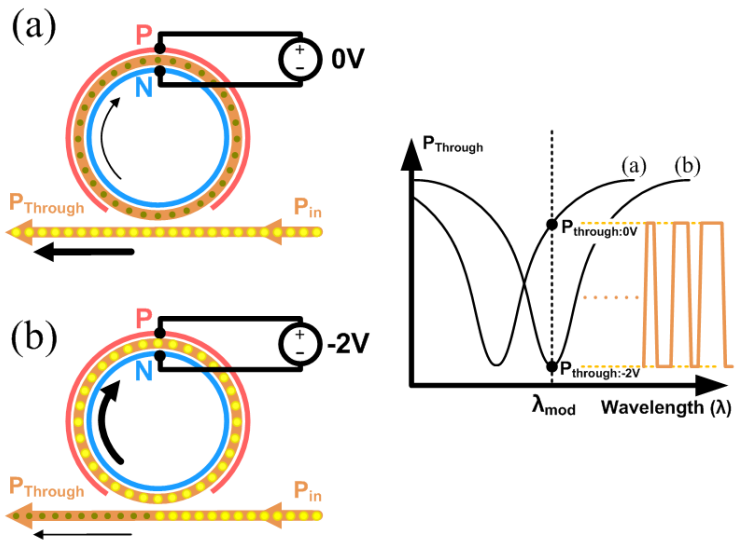


Figure 1-7. Conceptual optical modulation diagram with MRM transmission spectra

However, his instability of operating condition is also present in MRM, which is very sensitive to temperature and input optical power. Figure 1-8 and 1-9 show spectra near resonance of Si MRM with temperature and input optical power. External temperature variation changes its refractive index (η_{res}) and causes a large variance of the MRM resonance wavelength and then, consequently, makes optical modulation unstable. Moreover, when the input optical power near resonance wavelength increases, it causes temperature increasing inside the ring, called a self-heating, and also makes similar problem for data modulation. Therefore, for the practical use as modulator, ring structure is essential to calibrate the resonance wavelength drift from several temperature instabilities. For the calibration for external variations, various studies have been progressed under the name of wavelength stabilization circuit (λ-stabilizer) and it will be also discussed in next chapter [11].

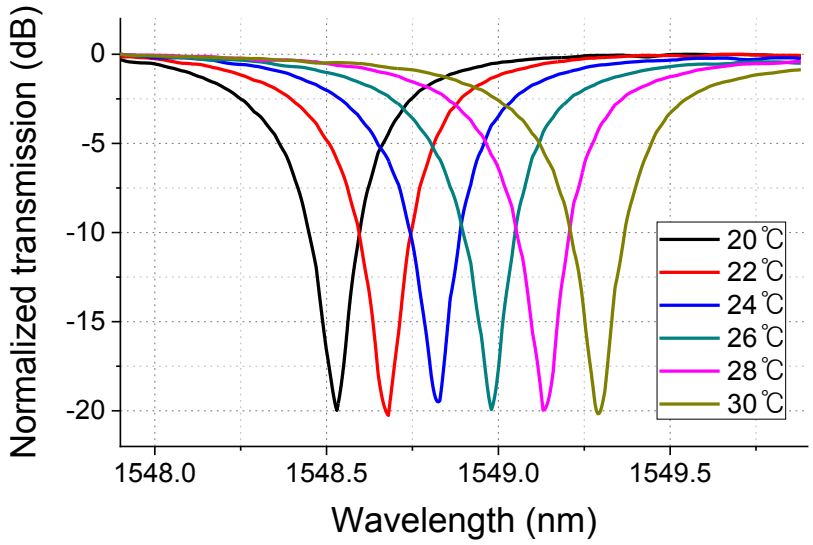


Figure 1-8. Si MRM transmission spectra according to six different external temperatures

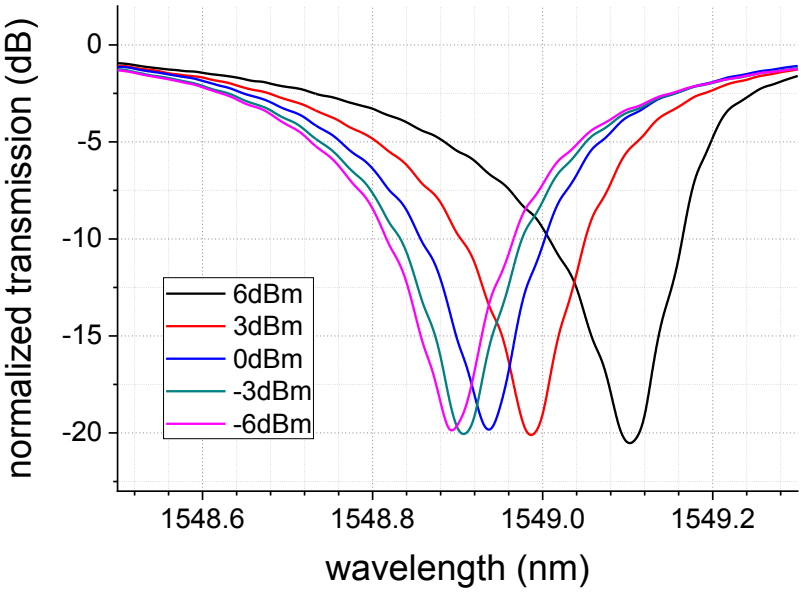


Figure 1-9. Si MRM transmission spectra according to five different input optical powers

1.3. Stabilization Algorithms for Optical Modulators

1.3.1. MZM Bias Controller

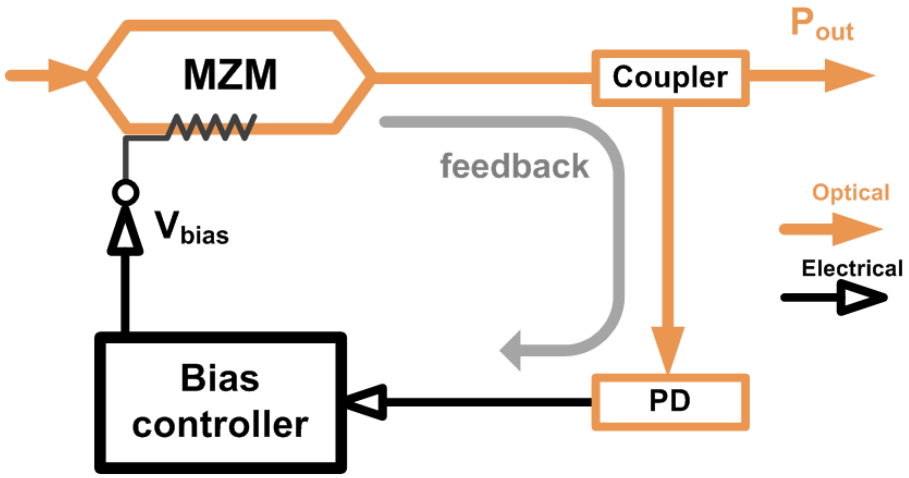


Figure 1-10. Conceptual block diagram of the MZM bias controller

Figure 1-10 shows a block diagram of the conceptual MZM bias controller. In fact, this MZM bias controller is used not only to overcome thermal drift problems descripted in previous chapter but also to adapt to various modulation techniques that require different optimal bias. For example, the optimal bias for the intensity modulation such as on-off keying (OOK) modulation or pulse-amplitude modulation (PAM) should be the quadrature bias which has the

maximum optical modulation amplitude (OMA), but in case of phase modulation such as binary or quadrature phase shift keying (BPSK or QPSK), the peak or null bias is the optimal because these biases can generate phase shift of π with same OMA assuming with modulation amplitude of V_π [12].

There are various published researches for the MZM bias control. A low-frequency dithering signal (or a pilot tone) has long been used for this control algorithm. The dithering signals of amplitude α and phase ϕ added on DC bias from equation (1.1) can generate relevant monitoring output signals. Equation (1.5) and (1.6) represent the 1st- and 2nd- order harmonics from input optical power (P_0) after dithering signal of equation (1.7) addition on DC bias. The 1st- order harmonic component is minimized on null or peak bias and maximized on quadrature bias and the 2nd- order harmonic component is opposite. Based on this bias dithering and harmonics monitoring, the bias controllers using logarithmic ratio between harmonics [13] and detecting the coherent lights by 3×3 coupler [14] were demonstrated and published.

$$P_{1st-order}=P_0 \cdot \sin\phi \cdot (\frac{\alpha^3}{8}-\alpha) \tag{1.5}$$

$$P_{2nd-order}=P_0 \cdot \cos\phi \cdot (\frac{\alpha^2}{4}-\frac{\alpha^4}{48}) \tag{1.6}$$

$$V_{Pilot}(t)=\alpha \cdot \sin(\omega t+\phi) \tag{1.7}$$

Since these bias controllers have potential to be integrated with Si MZM, so the possibility as IC chips is very important with the development of Si photonics. However, all these mentioned researches are not reported with integrated circuit (IC) chip and only demonstrated with discrete components or system level, so it is hard to be estimated the area and power directly. Basically, the frequency of bias dithering, as most commonly used method, is few kilohertz, the low-pass filters or band-pass filters are essential. As indirect estimation, even except the power budget, the area of these filters is expected to have considerable area under um technology. Therefore, an alternative solution or algorithm for IC chip is needed for the Si MZM bias control.

1.3.2. MRM Wavelength (λ) Stabilization Circuit

In case of MRM, the situation is little more serious. Intrinsically, it did not have any DC bias port (like MZM) for calibrating wavelength drifts (λ-drifts). Fortunately, the MRMs including a p-type doped resistor on the waveguide as a heater have been developed and researched for controlling resonance wavelength [15-16]. Additionally, as shown in figure 1-11, it can be used to monitor from direct coupling of a portion of modulated optical output power, but it can be also used for monitoring by additional drop-port to the Si MRM [17].

As similar with MZM, the dithering monitoring method could be also applied to MRM [18]. However, since a time constant from heater to drop port is generally few ten μs, the dithering frequency should be under few ten kHz [19]. Similar with MZM, this dithering method needs Si filters of huge area, so this could be a barrier to integrate the control circuits as mentioned in MZM chapter.

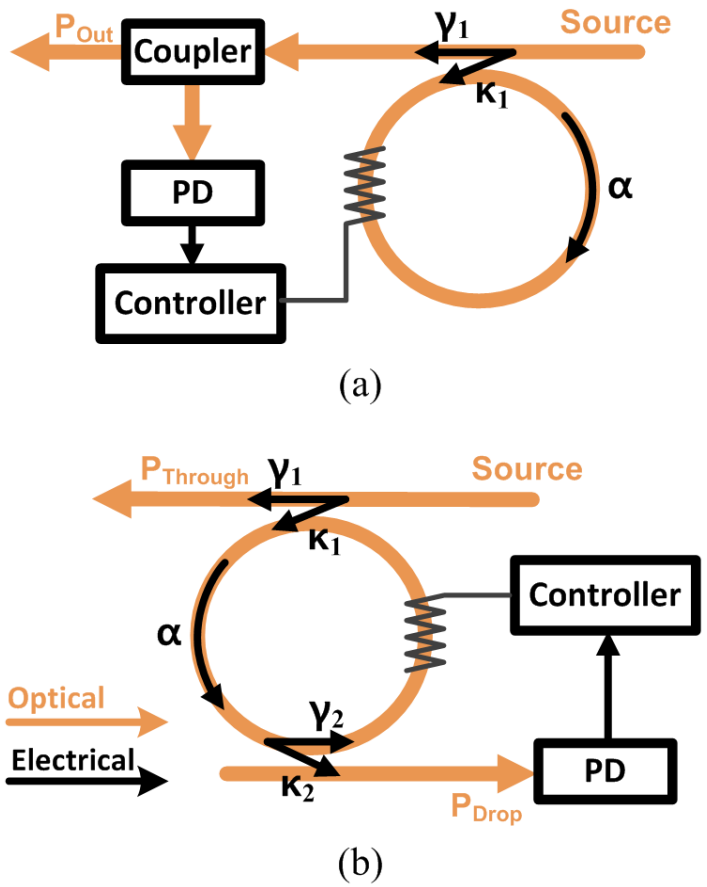


Figure 1-11. Conceptual block diagram of the Si MRM wavelength (λ) stabilization circuit (a) without or (b) with a drop port

Unlike MZM bias control, there are researches about λ-stabilizers demonstrated with IC chips. Some use monitoring an average power at drop port and minimize it [20]. Through this control algorithm, the stabilizer controls the resonance wavelength to a maximum point of an extinction ratio (ER). However, others approaches are conducted from

OMA perspective rather than ER [21]. These stabilizers find and maintain the maximum of OMA by continuous monitoring the optical power at 0 and 1 referred to the transmitted data. However, these stabilizers may not be inappropriate in power budget due to continuous use of high-speed circuits for data-dependent OMA monitoring and its demonstration speed is only 5-Gb/s. There is other approach using a slope quantization [22] but it is not fully-integrated yet and its demonstration speed is only 2-Gb/s. In this dissertation, we propose and demonstrate a new solution or algorithm with monolithically integrated chip which finds maximum OMA and calibrates it using the temperature monitoring circuit.

1.4. Outline of Dissertation

This dissertation focuses on control algorithms of bias and temperature stabilization for optical modulators (MZM and MRM). All of stabilization circuits are fabricated and demonstrated by single IC chip, and the area and the power budget are improved gradually. The rest of this dissertation is organized as follows.

Chapter 2 shows the MZM bias control algorithm based on OMA monitoring. In this chapter, we propose a new bias control method using OMA monitoring and demonstrate it for the first time as a single IC chip. Chapter 3 shows the improved MZM bias control algorithm based on average power and OMA monitoring. In this chapter, we propose and demonstrate a two-step approach with additional average power monitoring, in which the controller could be dramatically improved in power budget. Chapter 4 shows new application of the two-step approach for MRM λ-stabilization. In this chapter, we propose and demonstrate a new low-power solution to MRM temperature stabilization, in which the algorithm can calibrate not only external temperature but also input laser power variation. Finally, all the algorithms and demonstrations will be summarized in chapter 5.

2. Control Algorithm Based on Optical Modulation Amplitude (OMA) Monitoring

The control algorithm based on the OMA monitoring described in this chapter is proposed and demonstrated through the MZM for 850-nm application. As described in chapter 1.3.1, methods with pilot-tone have critical disadvantage of integration difficulty for IC chip. In this section, we propose a new algorithm that directly monitors and continuously maximizes OMA, in which a control circuit can be easily integrated into a small area.

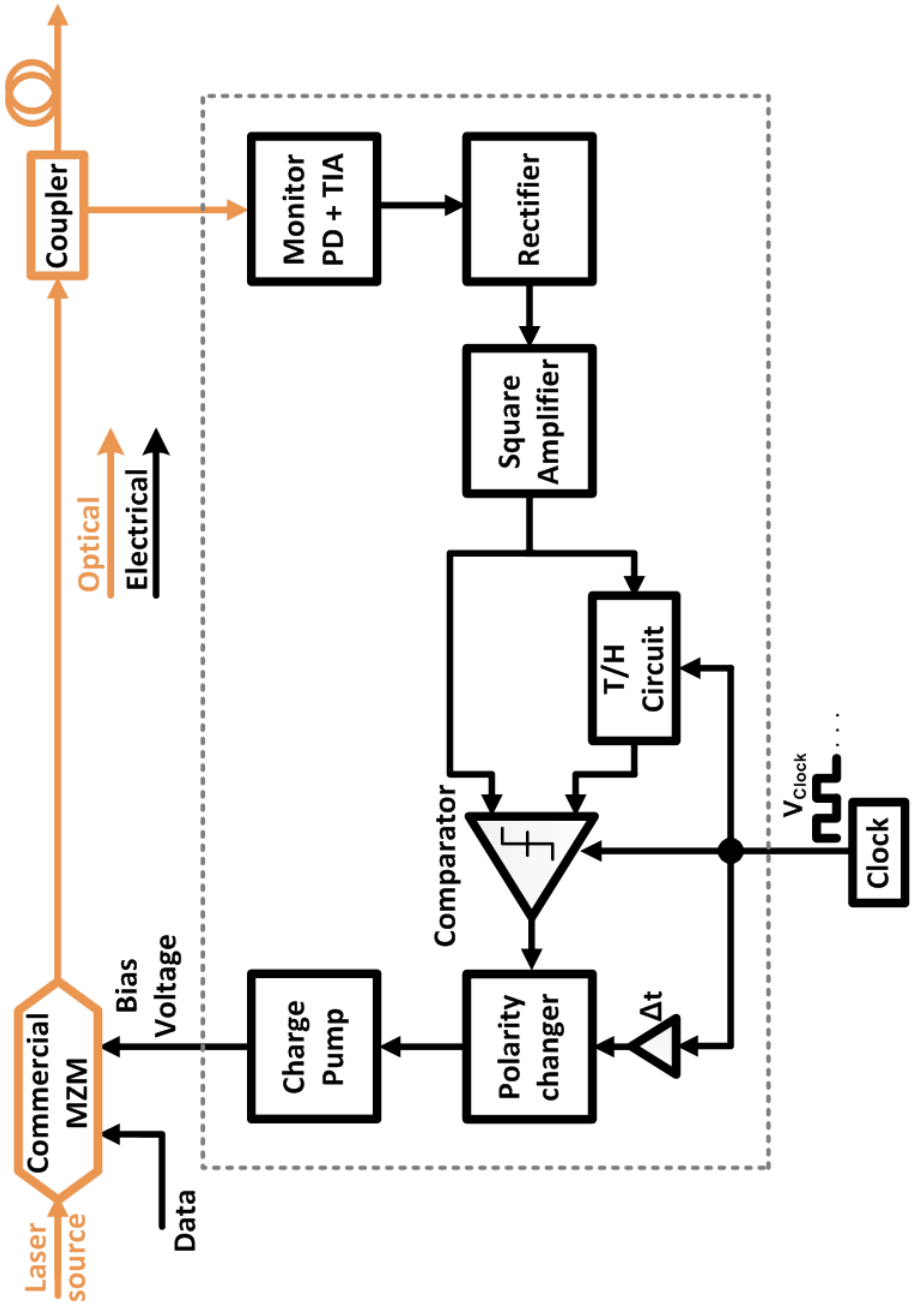


Figure 2-1. Block diagram of MZM bias controller based on OMA monitoring

2.1. Control Strategy

The box in figure 2-1 shows the block diagram of our MZM bias controller. It consists of monitor photodetector (PD), trans-impedance amplifier (TIA), rectifier, track-and-hold (T/H) circuit, comparator, polarity changer, and charge-pump (CP), all of which are monolithically integrated. A portion of MZM output light is coupled into the monitor PD and converted into voltage signals with the TIA. The rectifier produces DC signals (V_{Rec}) representing the OMA at a given MZM bias point. In order to provide large sensitivity of OMA near the optimum bias, a square amplifier (V_{Sqr}) is installed after the rectifier. Figure 2-2(a) shows the MZM DC transfer curve according to several bias conditions. The best modulation efficiency is achieved when the MZM is biased at the quadrature point ($V_{Quad+/-}$), in which point the linearity and the slope is the best due to the DC curve follows sine wave. Figure 2-2(b) shows the output curves of rectifier and the square amplifier with improved sensitivity near the optimum bias.

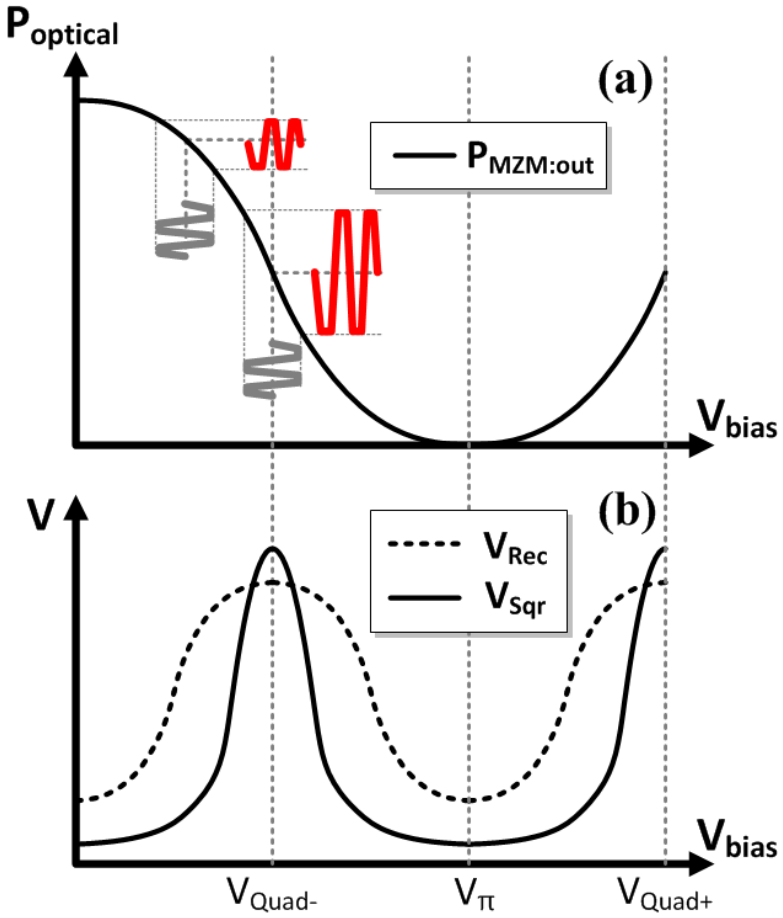


Figure 2-2. (a) MZM DC bias transfer curve with (b) rectifier output (VRec) and square amplifier output (VSqr)

Based on the obtained OMA information, the followed remaining circuits are used to maintain the optimal MZM bias. All subsequent operations are triggered with the clock signal (V_{Clock}) provided externally. The square amplifier's output is connected to the T/H circuit ($V_{T/H}$) and held the information for a half period. The comparator

compares the present OMA information (V_{SQR}) with the previous stored one ($V_{T/H}$). At the same time, the MZM bias moves voltage up or down by the charge-pump, which direction is decided by the comparator's output. When the V_{SQR} is higher than the $V_{T/H}$, the CP maintains its pumping polarity but when it is not, the polarity is reversed, all of these direction changes are operated by the polarity changer. In this way, the optimal bias can be automatically approached and maintained.

Figure 2-3 shows timing diagram of the control flow described in the preceding paragraph. After the bias controller reset at t_0, the MZM bias moves up with initial polarity of "UP". While reaching the optimum, the V_{BIAS} continues to increase, accordingly V_{RECT} and V_{SQR} increase together, and the polarity of charge-pump slew does not change according to the decision of the comparator. As V_{BIAS} increases, when it passes the optimum bias point, V_{SQR} decreases. After just moment, stored $V_{T/H}$ becomes larger than V_{SQR} for a half period, the comparator judges it, and the polarity changer changes the current slew direction like as t_1 and t_3 moment by star sign (★). By repeating this process, the bias voltage maintains the optimum with the voltage dithering, which amplitude is decided from the charge-pump slew-rate (I_{CP}/C_{BIAS}) and control clock speed.

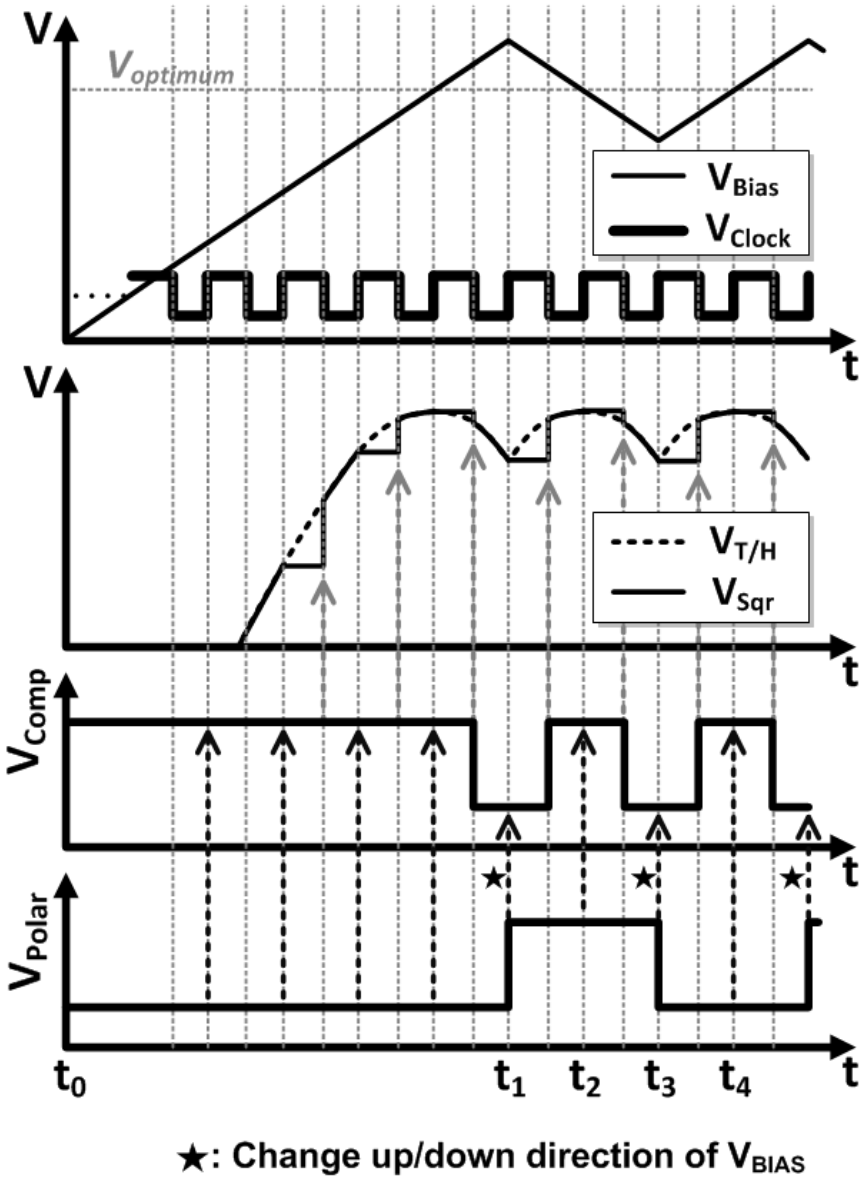


Figure 2-3. Timing diagram of bias control process

2.2. Implementation

This section describes detailed design of the sub-blocks used in the bias controller. Firstly, as monitoring photodetector, we use an 850-nm CMOS photodiode which can be easily integrated in standard CMOS processes [23-24], which has 3-GHz bandwidth and 0.0125-A/W responsivity. It receives vertically coupled optical power at an area of about 100-μm^2. The converted photocurrent is converted again into a voltage signal by the TIA, which configuration is a shunt-shunt feedback structure with an on-chip low-pass filter and a DC-balancing buffer as shown in figure 2-4 [25]. It has 60-dBΩ total gain with enough bandwidth to transmit 3-Gb/s data.

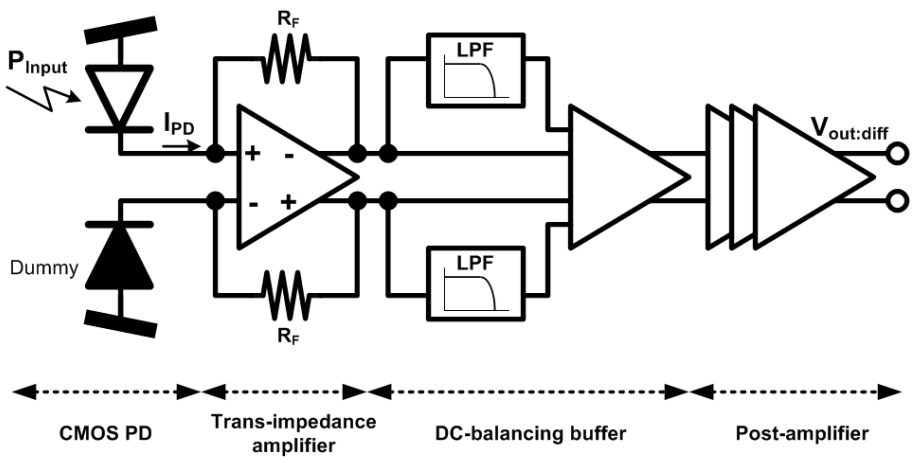


Figure 2-4. Schematic of shunt-shunt feedback TIA

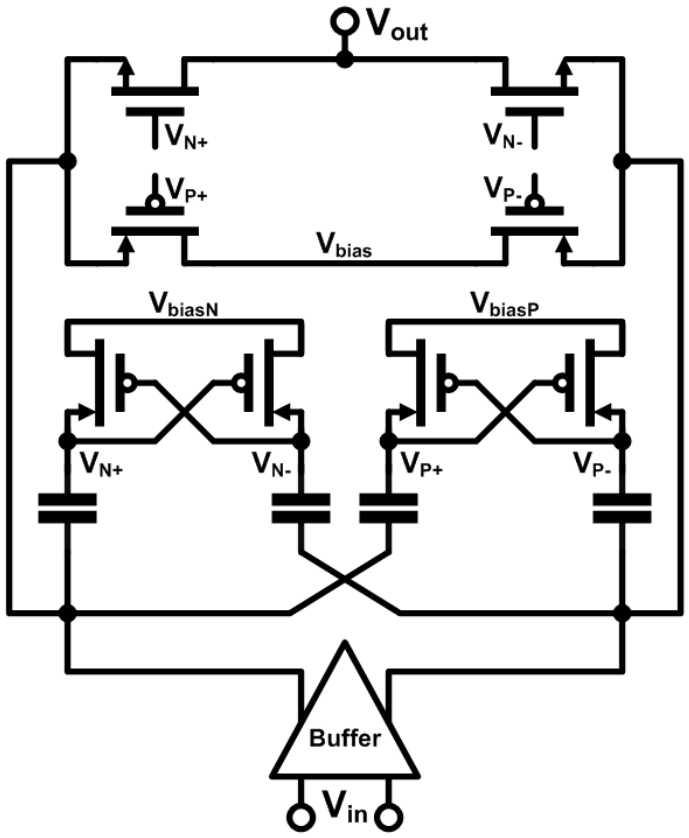


Figure 2-5. Schematic of driven-gate CMOS high-speed rectifier

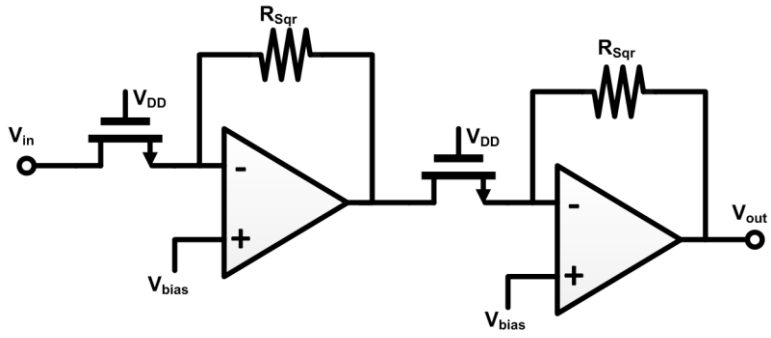


Figure 2-6. Schematic of CMOS square amplifier

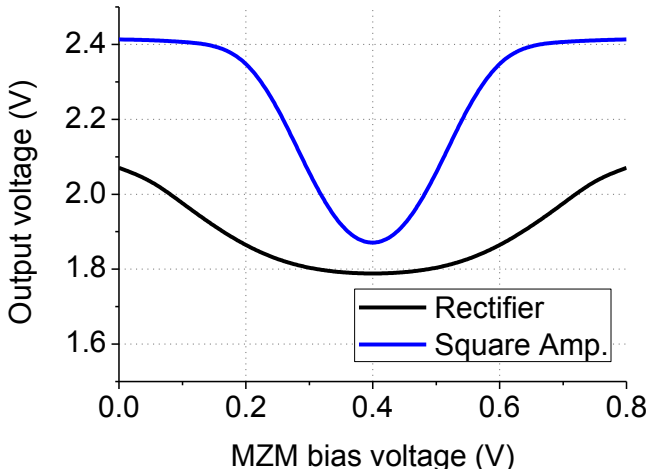


Figure 2-7. Simulation results of rectifier and square amplifier outputs according to MZM DC bias

A conventional CMOS rectifier has a poor linearity since it has conversion difficulty when the signal lower than the threshold voltage (V_{th}) is coming. Therefore, we used a driven-gate rectifier configuration as shown in figure 2-5, which improves sensitivity near the V_{th} through clock bootstrapping [26]. Despite the improved linearity of the rectifier, the OMA sharpness near optimum bias is not high enough, so that the dithering might be worse. Fortunately, a square amplifier as shown in figure 2-6 can improve its sharpness and the figure 2-7 shows simulation results of rectifier and square amplifier outputs according to MZM DC bias curve. In practical implementation, the rectifier output is designed to have lower value as the OMA becomes larger, so that the

comparator's input sensitivity operates at about 60% of the supply voltage which is the best. As shown in the figure, we can clearly see that the OMA sensitivity is improved near the optimum [27].

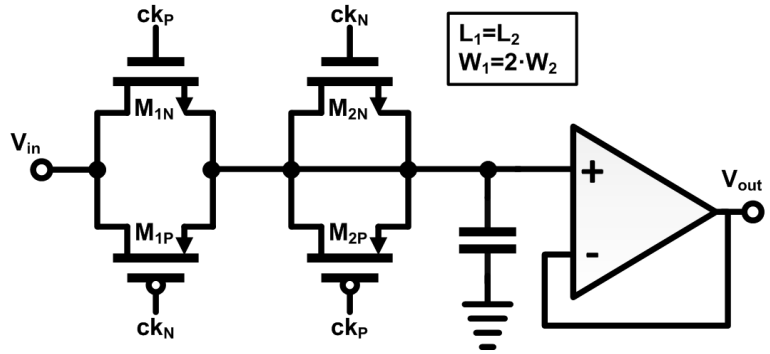


Figure 2-8. Schematic of CMOS T/H circuit with charge-offset cancellation

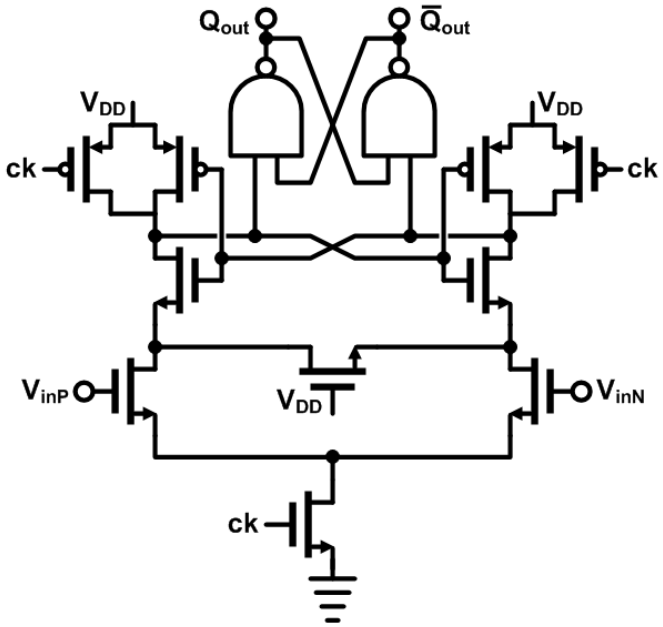


Figure 2-9. Schematic of sense-amplifier-based D flip-flop

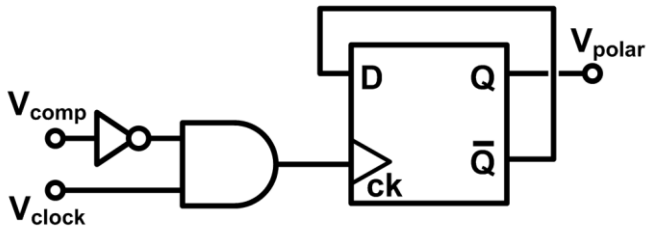


Figure 2-10. Schematic of polarity changer

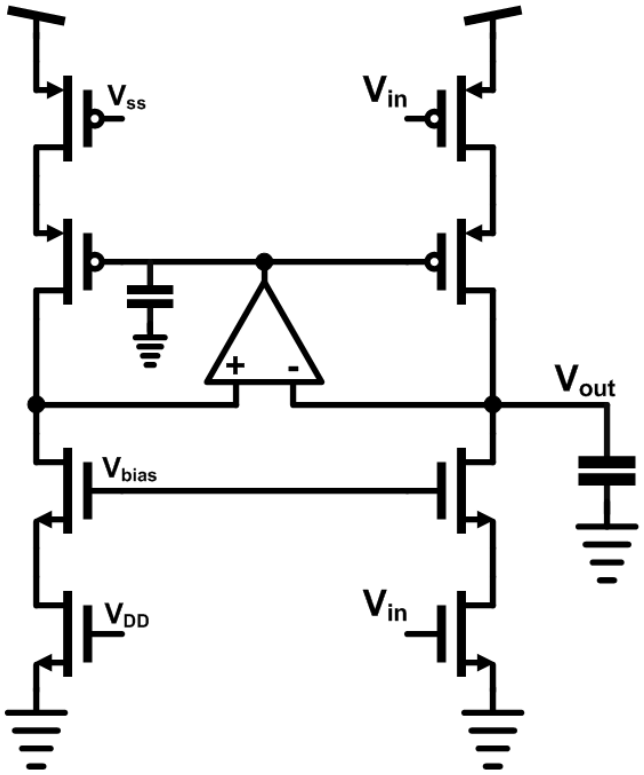


Figure 2-11. Schematic of charge-pump with p-n current matching

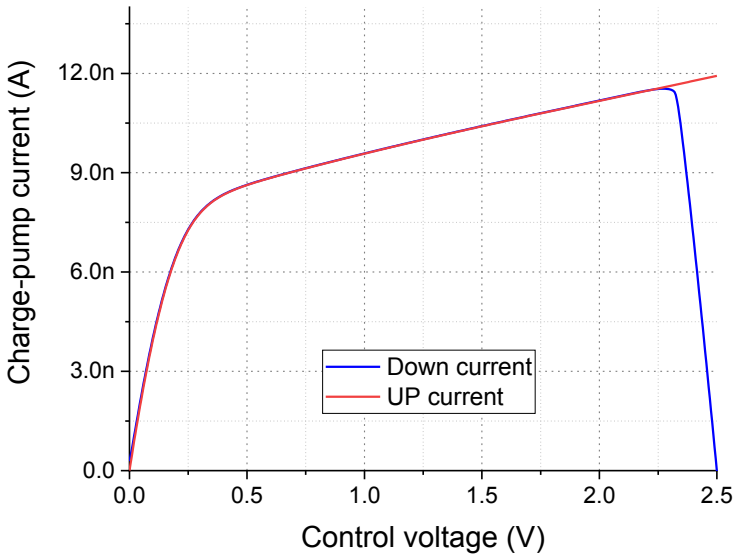


Figure 2-12. Simulation results of charge-pump currents according to output voltage

The T/H circuit uses a structure improved with a charge-offset cancellation function as shown in figure 2-8 [28]. The comparator uses a sense-amplifier based D flip-flop as shown in figure 2-9, which is widely used for high-speed and high-sensitivity applications. As shown in figure 2-10, the polarity changer uses one D flip-flop and one AND gate as a state machine, in which if the input is 1, it maintains the output but if the input is 0, it changes its output like 1 to 0 or 0 to 1. In case of charge-pump as shown in figure 2-11, it is important to have a constant slew rate, that is, it should flow a constant amount of current to the output capacitor (C_{BIAS}) regardless its direction. To the constant

slew, we used a p-n current matching structure, so that a constant current flows over a wide output range [29]. Figure 2-12 shows simulation result of charge pump current according to output voltage at up and down states.

2.3. Measurement Results

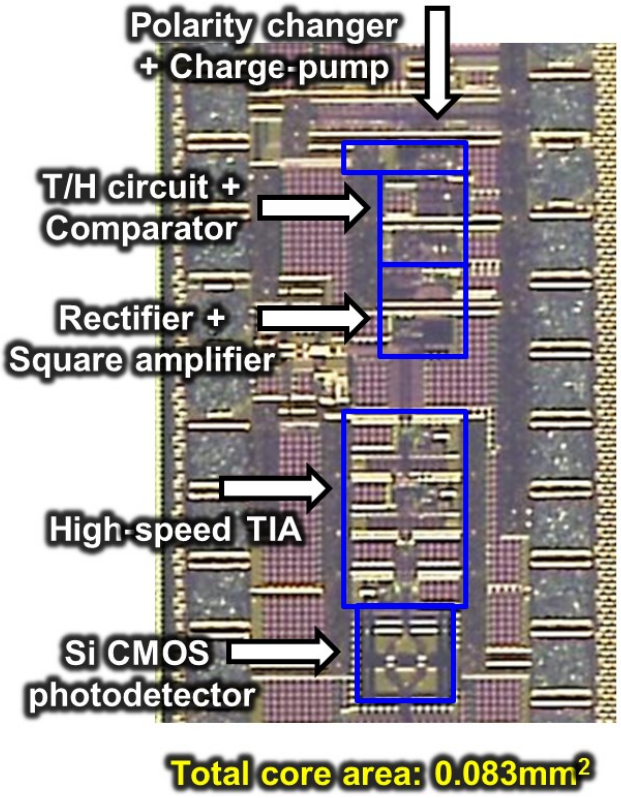


Figure 2-13. Microphotograph of bias controller IC chip

Figure 2-13 shows the chip photograph. It was fabricated with 0.25-μm BiCMOS technology and has about 0.083-mm^2 area. This chip is the first IC chip as the MZM bias controller and it has great potential of single chip integration with Si MZM. Because of the low responsivity of Si CMOS photodetector, a large optical power of 13-dBm by

Erbium-Doped Fiber Amplifier (EDFA) is provided to MZM measurement to stable operation of the bias controller. Fortunately, Si photonics foundry which provides photonic-electronic integration technology can integrate with a Ge photodetector which has tens of GHz bandwidth and about 0.5-A/W responsivity, so this problem can be easily solved. The circuit consumes power of 92.5-mW with the 2.5-V standard supply voltage. Most power consumption is from the rectifier and its input buffer.

Figure 2-14 shows the measurement setup. The target 850-nm MZM has 5GHz bandwidth and 0.8-V V_{π}. The 850-nm laser source with 13-dBm optical power is provided to the MZM with data or pilot tone modulations, while half of its output power is coupled to the Si CMOS photodetector of the bias controller. At this time, we use two oscilloscopes to observe the bias voltage and the output optical eye diagram, respectively. The 50-kHz control clock is provided externally in consideration of the charge-pump's slew rate.

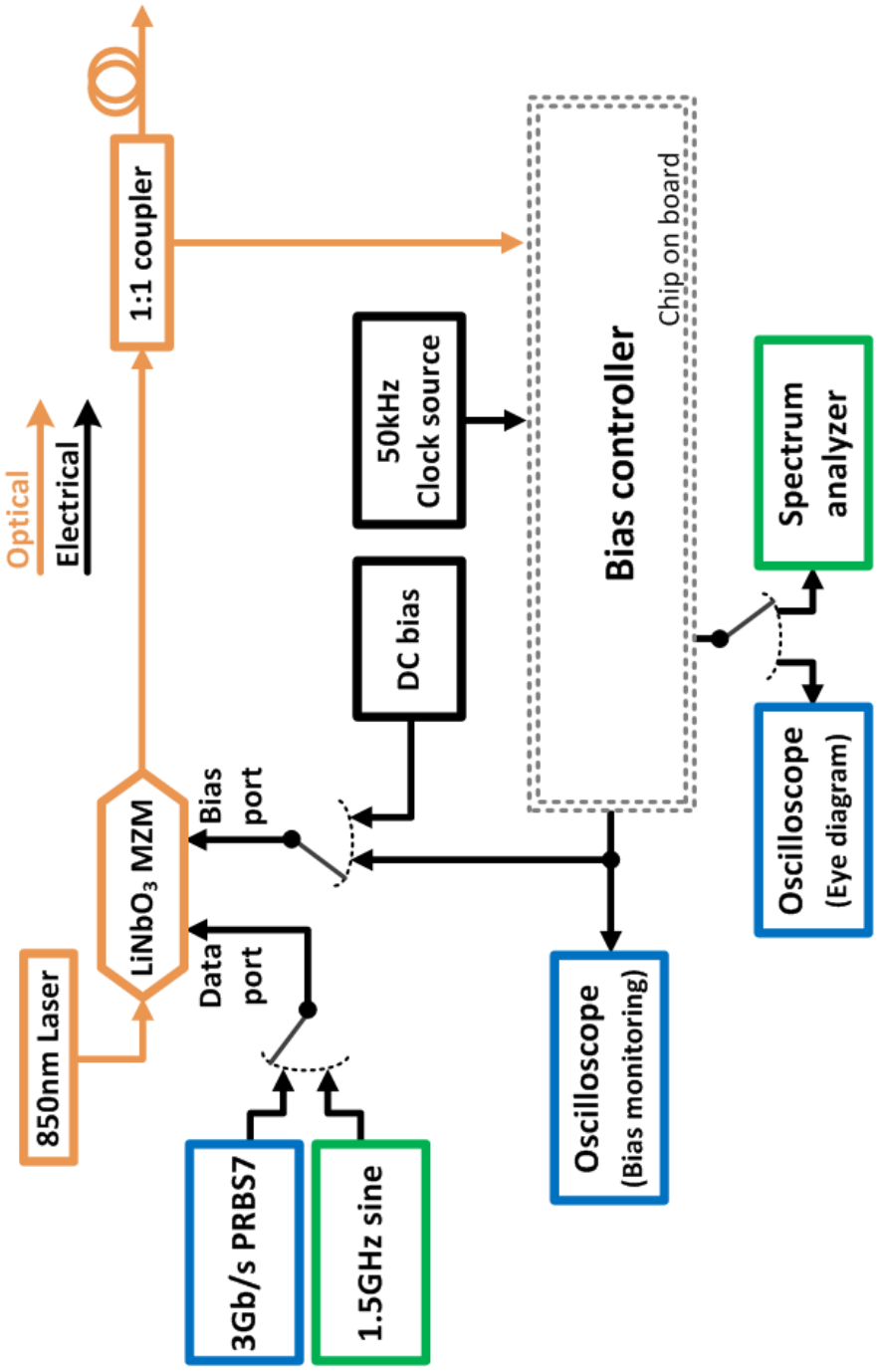


Figure 2-14. Measurement setup for demonstration of MZM bias controller based on OMA monitoring

Firstly, figure 2-15 shows the transient response measurement from the moment the controller is turned-on until the bias voltage reaches the optimal. The bias voltage takes up to about 400-μs until it reaches the optimal, and next it maintains optimum with voltage dithering. The slew rate is about 1-mV/μs and the dithering amplitude is about 40-mV_{P2P}, both of which can be changed depending on the circuit design.

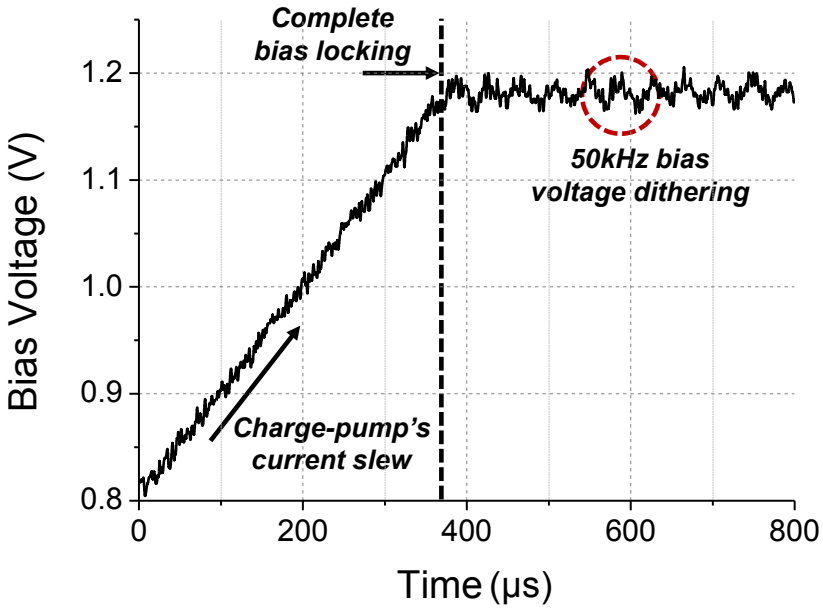


Figure 2-15. Initial transient response of MZM bias voltage

To verify the continuity of the circuit operation, two long

measurements are also achieved. One is to observe whether the controlled bias is really optimal and the other is to observe whether the MZM can maintain clean eye diagram for a long time.

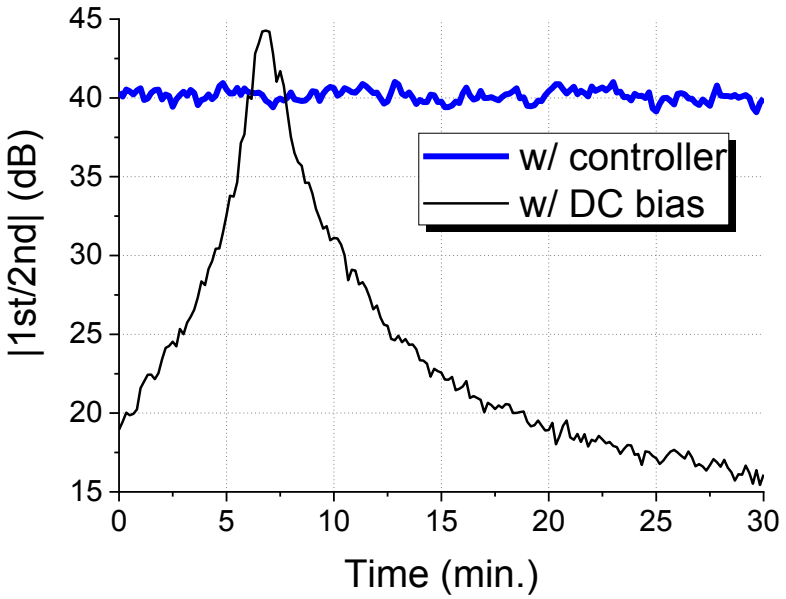


Figure 2-16. Ratio of first and 2nd-harmonic components for 1.5-GHz modulation of MZM with and without bias controller

For the former measurement, harmonics of modulated optical power are observed with a 1.5-GHz pilot-tone modulation. At the optimal bias, the MZM must produce the largest fundamental (1^{st}-order) tone and the smallest second-order harmonic. Figure 2-16 shows the ratio between the fundamental to the second-order during 30

minutes operation with-and-without a bias controller. Without a bias controller, that is with a DC bias, the rate changes dramatically due to internal thermal drift. On the other hand, with the bias controller, the MZM bias controller keeps the ratio close to the optimal. There is slight difference between the controlled ratio and a peak of un-controlled ratio. It is inferred due to periodic bias noise by the voltage dithering.

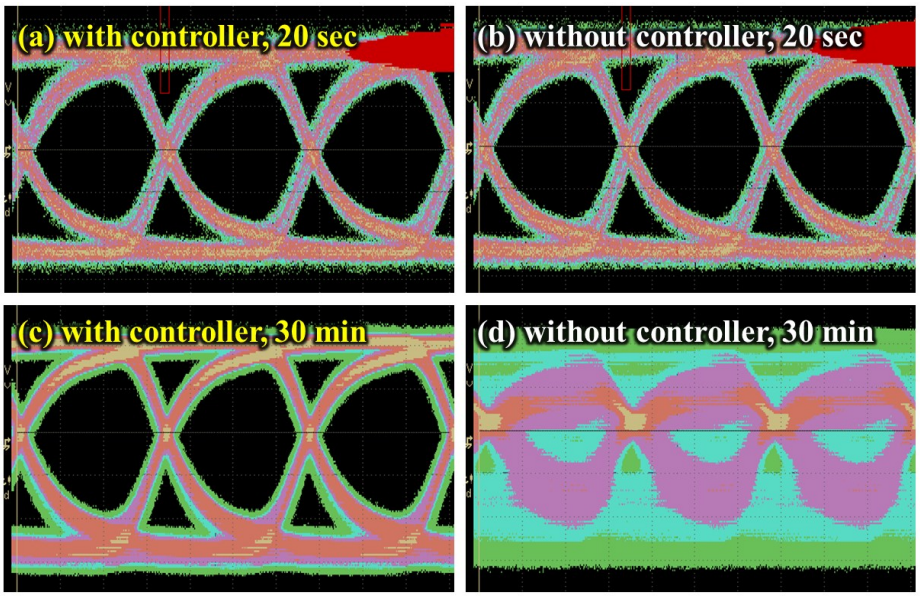


Figure 2-17. Accumulated eye diagram of 3-Gb/s data modulated with LiNbO3 MZM with or without bias controller (a), (b) for initial 20 seconds and (c), (d) for 30 minutes

Finally, for the latter measurement, the accumulated eye diagrams are observed with 3-Gb/s PRBS7 data modulation. This rate is limited

by the bandwidth of the Si CMOS photodetector rather than the sub-circuit of the bias controller. If the integrated photodetector is replaced by a Ge or an avalanche type, a much faster demonstration would be possible. Figure 2-17 shows a 10 seconds and 30 minutes accumulated eye diagrams with the bias controller or ground DC bias. Initial eye diagrams are all clear but the longer accumulated eyes have the great difference, in which the eye quality with bias controller is clearly maintained.

2.4. Summary

A new type of an integrated MZM bias control circuit is demonstrated. Our bias controller monitors the OMA of the MZM output optical power and automatically searches the optimum MZM bias voltage and maintains it there. A prototype IC chip realized in 0.25-μm BiCMOS technology with an integrated Si CMOS PD can provide the successful bias control for 3-Gb/s data modulation of a commercial 850-nm MZM. It has matters to be improved that continuous operation of high-speed circuitry leads to quite power consumption, the bias slew rate limits an initial acquisition time, and bias dithering leads to a slight degradation in optimization. However, out controller has great advantageous of always controlling the bias for maximum OMA without any additional monitoring tools like pilot tone. Also, reversing the direction of the OMA control, that is minimization OMA, is expected to be available for the NULL bias condition used in phase modulation. Furthermore, since the bias controller is based on the Si process fully-compatible with Si electronic-photonic integration, it has a great potential of providing Si MZM with an integrated bias controller.

3. Improved Control Algorithm 1: Based on OMA and Average Power Monitoring

The control algorithm based on the OMA and average power monitoring described in this chapter is proposed and demonstrated by the 1550-nm MZM. As described in Chapter 2, the algorithm based on continuous OMA monitoring has disadvantages of that it consumes too much power from high-speed circuits and it has quite bias voltage dithering depending on control speed and analog slews. In this chapter, we present an improved algorithm of that the bias controller uses OMA monitoring circuit not continuously but only initially. And it has a digital control independent from analog slew minimizes voltage dithering.

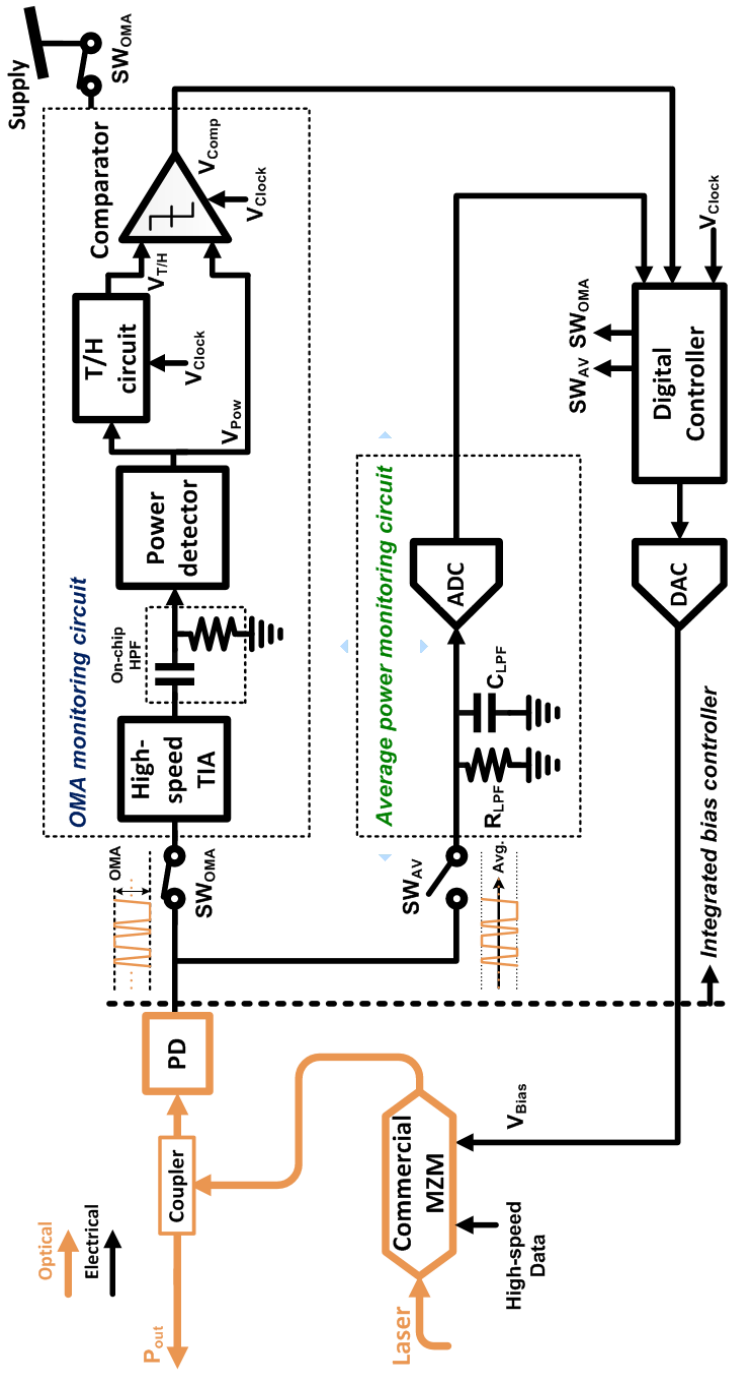


Figure 3-1. Block diagram of MZM bias controller based on OMA and average power monitoring

3.1. Control Strategy

The algorithm in this chapter is basically based on the method of the 'OMA monitoring' used in chapter 2. However, this method has disadvantages with too high power consumption, long initial acquisition time, and complexity of bias dithering. Therefore, we propose improved version of MZM bias control below.

First, we apply a two-step approach (initial scans and continuous-time calibration), which can overcome huge and continuous power consumption and long initial acquisition time. Second, the analog bias dithering is minimized by using a fine-tuned digital control in 1-bit unit. Finally, we replaced the high-speed rectifier with a power detector to improve OMA monitoring efficiency.

The algorithm described in this chapter is set in major two steps. As soon as the circuit is turned on, the first step is achieved to find the MZM bias generating optimal OMA through two bias voltage scans. Then, the second step of continuous-time digital PID control with average power monitoring is immediately followed. The second step with the average power monitoring circuit is used and based on the fact that if the optical average power at a given optimal DC bias remains constant, the optimal OMA also remains.

Figure 3-1 shows the whole block diagram of the bias controller, which can be divided into major three parts. First, OMA monitoring part, it consists of TIA, on-chip high-pass filter (HPF), power detector, T/H circuit and comparator, all of which are used only at the initial first step. Second, the average optical power monitoring circuit, it consists of a resistor as low-speed TIA and analog-to-digital converter (ADC) to be used for continuous-time calibration in second step. Finally, heater control circuit, it consists of synthesized digital circuit and DAC to manage overall algorithm digitally. Detailed circuit descriptions for all sub-circuits are described in Section 3.3.

3.1.1. Initial Bias Scans (First Step)

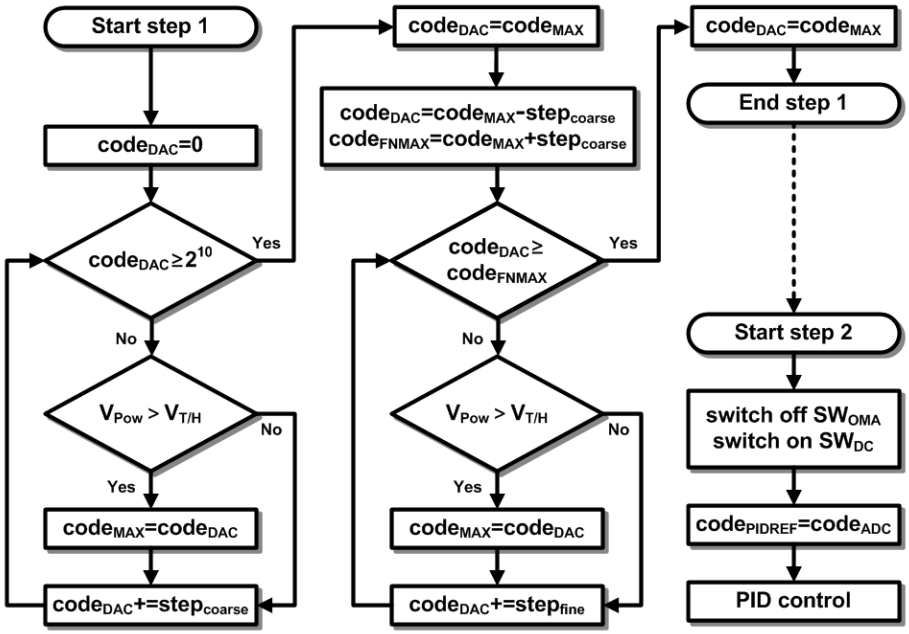


Figure 3-2. Algorithm flowchart of MZM bias control based on OMA and average power monitoring

Figure 3-2 shows a flowchart of our algorithm. When the circuit is turned on, it observes the MZM output while scanning the bias voltage from ground to supply voltage using the DAC. This scan is achieved from two number of step bits, $step_{COARSE}$ and $step_{FINE}$, all of which can be adjusted to reduce scan time depending on the situation. Also, all controls are synchronized by externally provided control clock. During these scans, TIA, power detector, and photodetector convert the optical

modulated signal into a DC voltage corresponding to the OMA. This monitoring photodiode can be easily integrated on a single Si chip such as avalanche Si type or Ge type depending on the optical wavelength in the future. For this demonstration, we use a hybrid-integrated Ge photodiode implemented on Si wafer by Si photonics foundry.

As first scan, in the increasing of $step_{COARSE}$ step-by-step, it can compare the present and the one-step past OMA using T/H circuit and comparator. When the present bias voltage produces a better OMA than the past one, the digital controller registers the present DAC code ($code_{DAC}$) on the maximum OMA code ($code_{MAX}$). Otherwise, this update of $code_{MAX}$ is skipped. After the full-range code scan of the DAC is complete, the coarsely optimized MZM bias is determined and stored in bit form, and then a second scan with $step_{FINE}$ starts. In this scan step, the controller initially sets $code_{DAC}$ to '$code_{MAX}$-$step_{COARSE}$' and define '$code_{MAX}$ + $step_{COARSE}$' as the end point of the fine scan. Except the range set, this fine scan is same as the coarse scan. When it finishes the scans, the $code_{MAX}$ will store initially optimized DAC code which provides the largest OMA.

Figure 3-3 shows a timing diagram of the first step. V_{Bias} is the MZM bias voltage provided by $code_{DAC}$. V_{Pow} is the power detector output, $V_{T/H}$ is the T/H circuit output which holds V_{Pow} only for half

period of the control clock cycle, V_{Comp} is the negative edge-triggered comparator output, and V_{clock} represents the control clock signal. The coarse scan starts from t_1 and the fine scan starts from t_2. The moment of the star-sign (★) indicates that the OMA by the present bias is better than by the past one, so the present $code_{DAC}$ is registered to the $code_{MAX}$. Finally, when the scan is completed, the final $code_{MAX}$ is registered back to the $code_{DAC}$ and the next second step of continuous-time calibration begins.

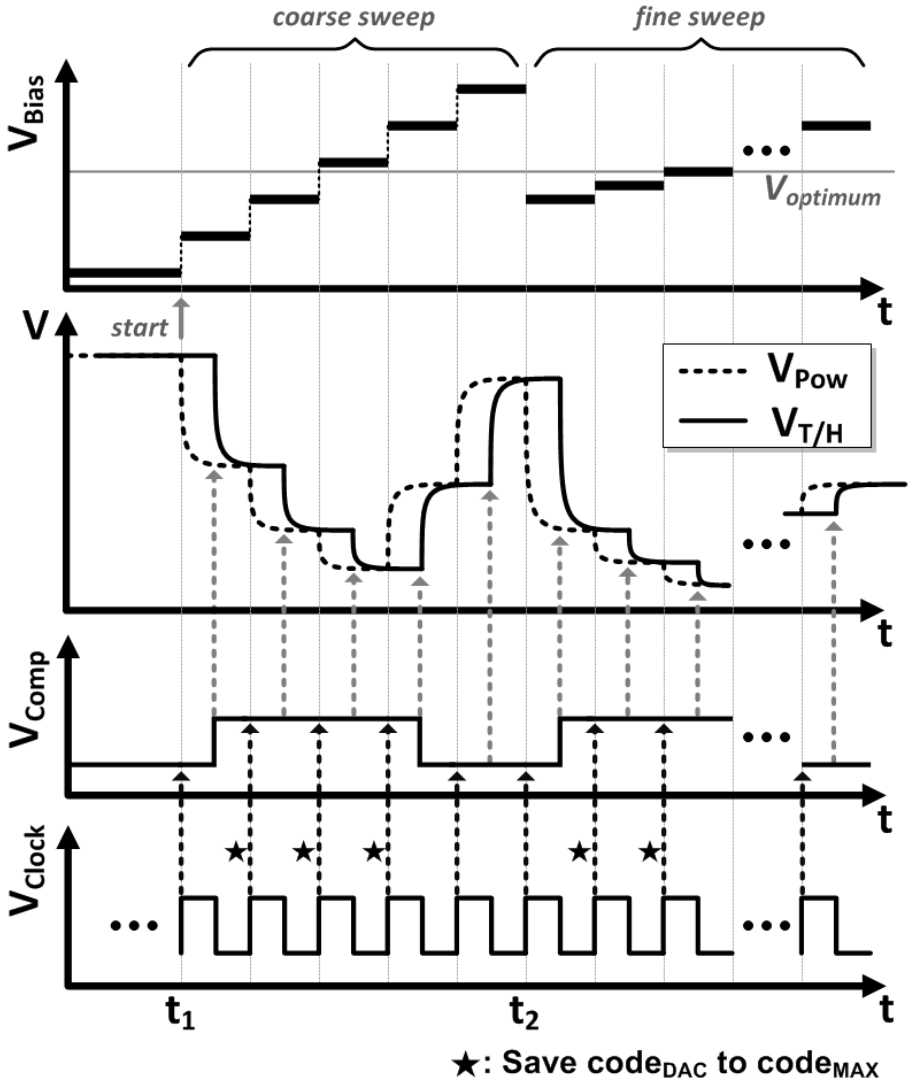


Figure 3-3. Timing diagram of initial bias scan step (First step)

3.1.2. Digital PID Control (Second Step)

When the second step begins, the digital controller disconnects the OMA monitoring circuit (SW_{OMA}) from the photodetector and supply voltage and connects the average power monitoring circuit (SW_{AV}) to the photodetector. This turned-off OMA monitoring circuit contributes to reducing power consumption. Then, the photocurrent corresponding to the average optical power by the photodetector is converted into a DC voltage by R_{LPF} and C_{LPF} and digitized by the ADC. At the end of the first step with the initially optimized MZM bias, the digital controller immediately registers the digitized ADC code in a new register for using as reference indicating optimal OMA. Then, this reference code can be used to maintain the same average optical power continuously by digital PID control.

The average power monitoring circuit consists of low-speed TIA resistor (R_{LPF}) and on-chip capacitor (C_{LPF}) and conventionally used 10-bit second-order Σ-Δ modulator ADC. Each block in the feedback can be linearly-modeled and performed a classic dynamics analysis to determine the PID coefficients of proportional, integral, and derivative, respectively (K_P, K_I, and K_D).

3.2. Implementation

The TIA as shown in figure 3-4 is designed with the inverter-based feedback structure having 60-dBΩ gain and 10-GHz bandwidth in post-layout simulation [30]. For OMA monitoring, the required input amplitude of photocurrents for the TIA is estimated 40-μA peak-to-peak at the optimal bias, which is based on signal-to-noise ratio (SNR) of TIA, comparator's sensitivity, OMA monitoring circuit's noise, and 1-bit resolution of the DAC. The T/H circuit is designed to structure of charge-injection compensation like chapter 2.2. The negative edge-triggered comparator is designed with the sense amplifier D flip-flop.

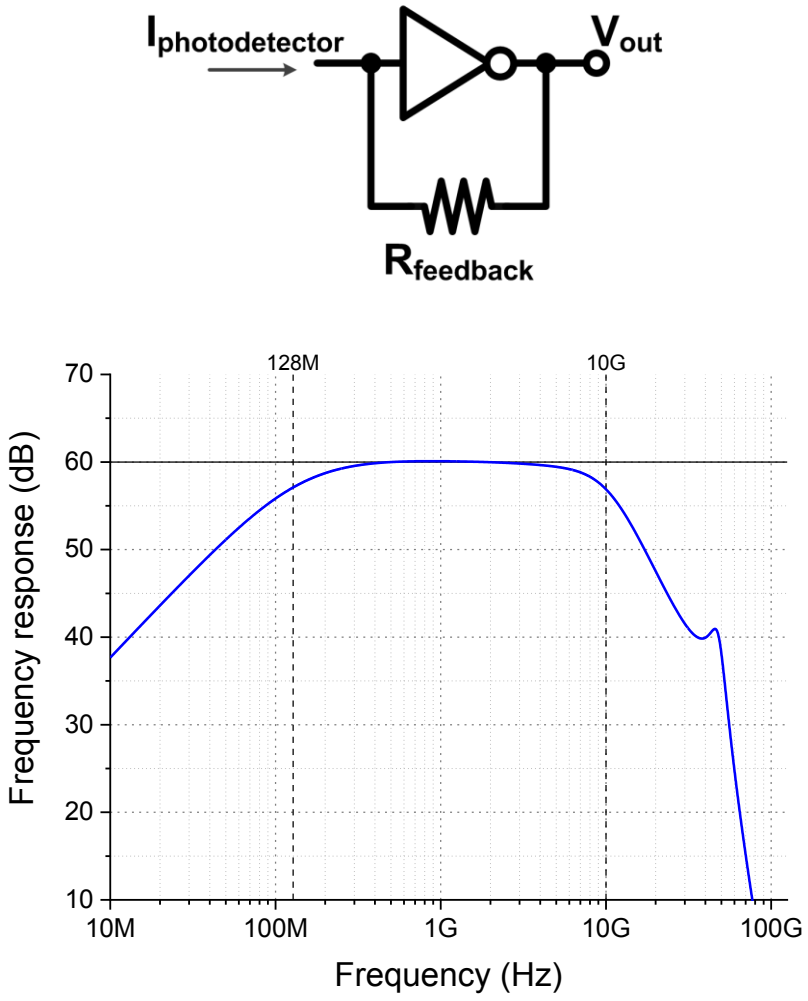


Figure 3-4. Block diagram and post-layout frequency response simulation of inverter-based feedback TIA

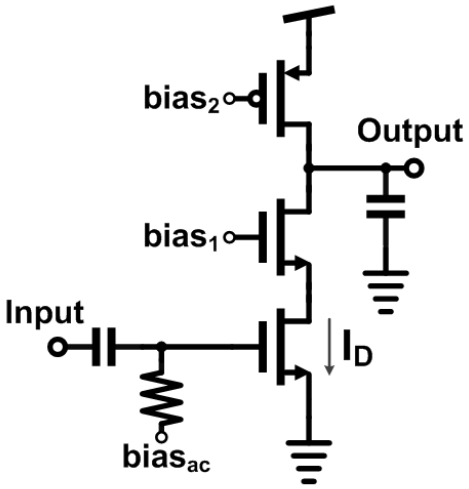


Figure 3-5. Block diagram of CMOS power detector

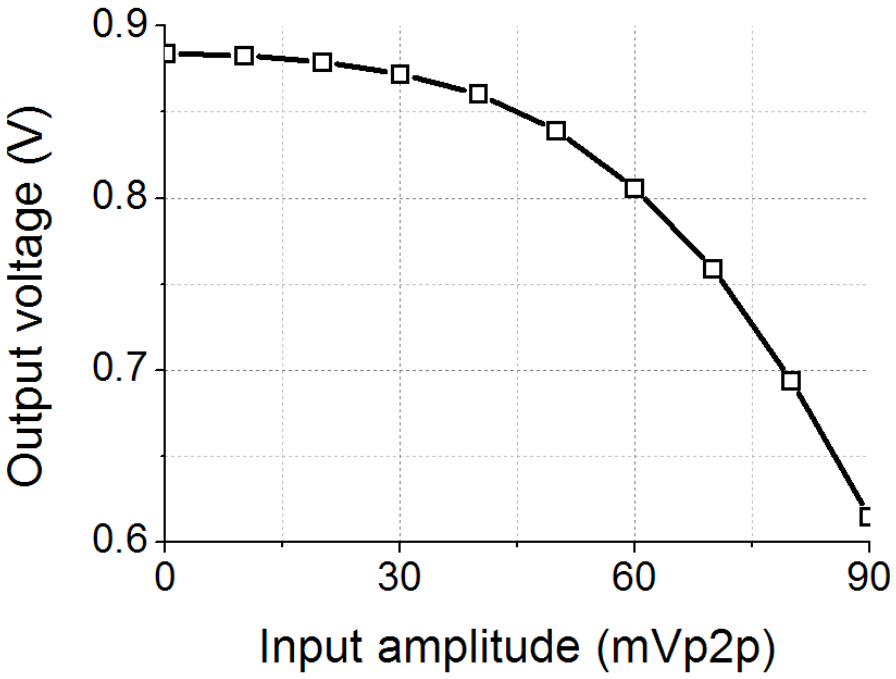


Figure 3-6. Post-layout simulation results of CMOS power detector

Unlike in chapter 2, we used a power detector structure for the OMA monitoring. Figure 3-5 shows the schematic for the power detector [31] and figure 3-6 shows its post-layout simulation results when 25-Gb/s random data having different voltage amplitude are introduced. It consumes only 50-uW power, which is dramatically improved from high-speed rectifier consuming few tens of mW.

The R_{LPF} is designed to be 1-kΩ corresponding to 0-dBm input monitoring optical power. The ADC is designed to conventional 2^{nd}-order Σ-Δ modulator, which is shown in figure 3-7. The two integrators for ADC are designed with switched capacitors which are modulated with same speed of Σ-Δ modulation. As shown in figure 3-8, the DAC providing analog bias voltage is designed based on the R-2R ladder structure and considered an offset due to the output impedance generated in the inverter.

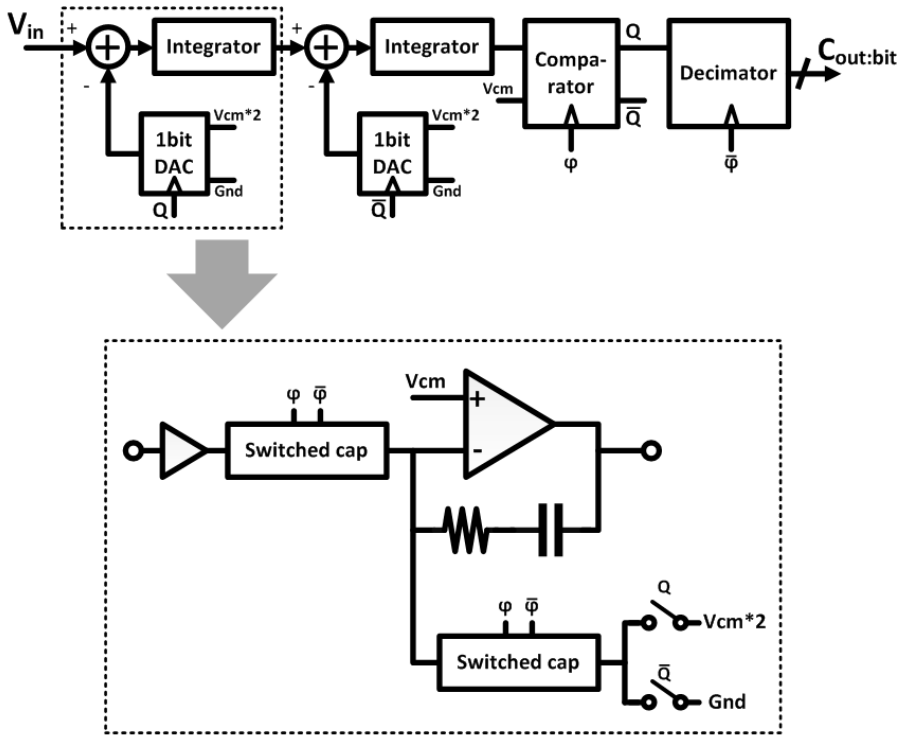


Figure 3-7. Schematic of analog-to-digital converter (ADC) based on second-order delta-sigma (Σ-Δ) modulator

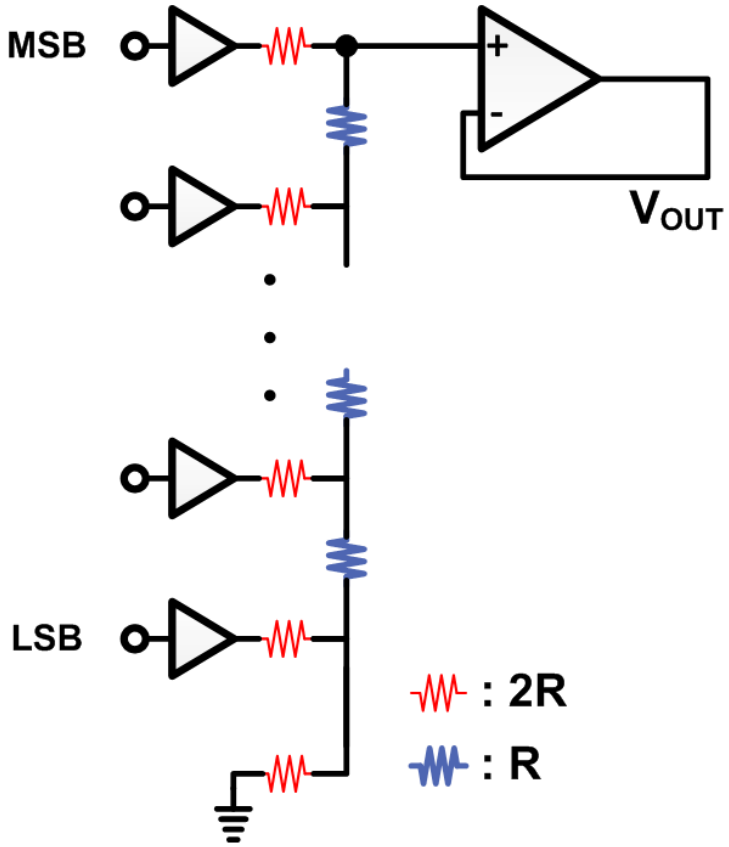


Figure 3-8. Schematic of digital-to-analog converter (DAC) based on R-2R ladder structure

The digital circuit, synthesized, placed, and routed computer-based on a RTL-level verilog-HDL, determines the DAC code while operating the initial scan step and the digital PID control step, subsequently. Figure 3-9 shows the used RTL-level code, which is based on 28-nm CMOS logic gates.

```
// Decimator of ADC
always@(posedge adcclock or negedge adcresetn) begin
        if(!adcresetn) adccount <= 11'b00000_00000_0;
        else begin
                if(adcin==1'b1) adccount <= adccount +1;
        end
end
always@(posedge coreclock[0] or negedge resetn) begin
        if(!resetn) begin
                adccode <= 10'b00000_00000;
        end
        else begin
                adccode <= adccount[9:0];
        end
end

// Digital controller for OMA and average power monitoring algorithm
always@(posedge coreclock[1] or negedge resetn) begin
        if(!resetn) begin
                code <= 10'b0000_000_000;
                maxcode <= 10'b0000_000_000;
                mode <= 2'b00;
                sweepcount <=7'b0000000;
                turnoff<=1'b0;
        end
        else begin
                if(mode==2'b00) begin
                        if(compout==1'b0) maxcode <=code;
                        code <= code + 63; // next 2 code;
                        sweepcount <= sweepcount+1;
                        if(sweepcount==16) begin
                                mode <= mode+1;
```

```
                                code <= maxcode-64;
                                sweepcount <=0;
                            end
                    end
                    else if(mode==2'b01) begin
                            if(compout==1'b0) maxcode <=code;
                          code <= code + 1<<sweepbit; // next 2 code;
                          sweepcount <= sweepcount+1;
                          if(sweepcount==(128>>sweepbit - 1)) begin
                                  mode <= mode+1;
                                  code <= maxcode;
                          end
                    end
                    else if(mode==2'b10) begin
                            refcode <= adccode;
                            mode <= mode+1;
                    end
                    else begin
                            turnoff<=1'b1;
                            code <= code + (ki+kp)*(adcvalue-refcode) -
(kp+2*kd)*feedpost + kd*feedpost2;
                          feedpost2 <= feedpost;
                          feedpost <= adcvalue-refcode;
                    end
            end
end
```

Figure 3-9. Register-transfer level verilog-HDL code (only ‘always@’ blocks) for synthesizing digital circuit based on two-step approach

The Figure 3-10 shows transistor-level room-temperature (25°C) simulation results of the initial bias sweep (First step) and followed continuous-time calibration (Second step). MZM, photodetector, TIA, on-chip HPF, power detector, and ADC are behavior modeled in Verilog-A. TIA, HPF, power detector, and ADC are simulated with the post-layout extracted parasitic components. During the first step, the controller determines the MZM bias voltage which generates the minimum value for the power detector output corresponding to the largest OMA, and then during the second step, it maintains the bias during. For this simulation, coarse- and fine- scan steps, K_P, K_I, and K_D are 64, 5, 1, 1, and 0, respectively.

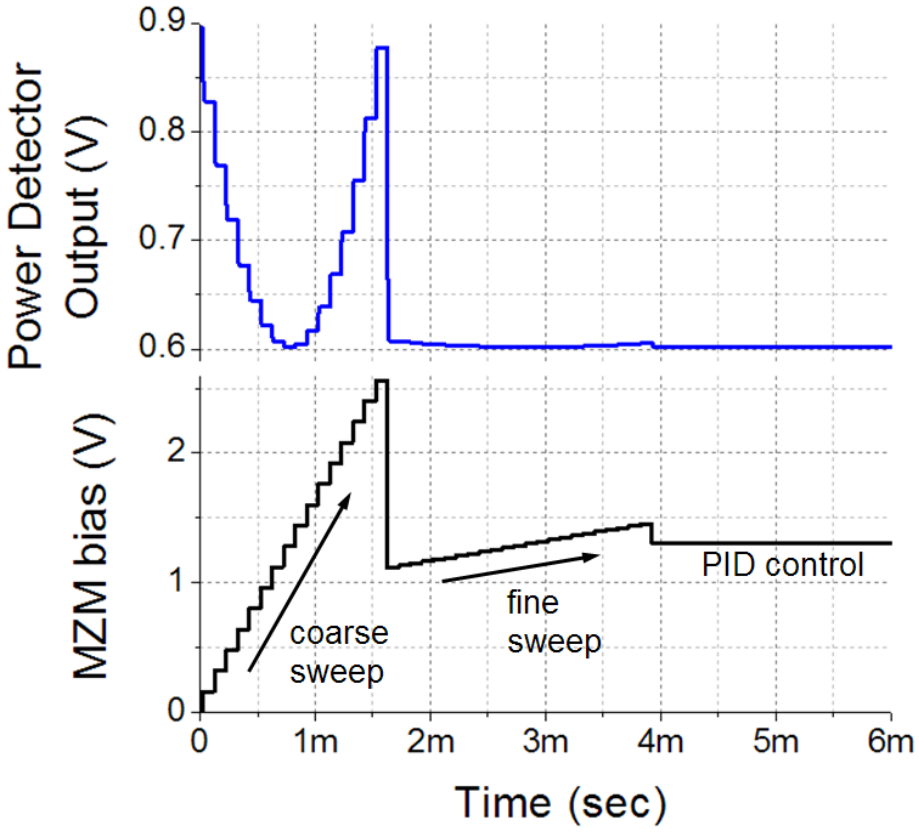


Figure 3-10. Simulated MZM bias voltage and power detector's output at initial bias scan step (First step)

3.3. Measurement Results

Figure 3-11 shows a photograph of our bias controller IC chip. To measure operations of the controller, we use the measurement setup shown in figure 3-12. It is fabricated with 28-nm standard CMOS technology and its area is about 0.017-mm^2. The other photonic IC with a Ge photodetector fabricated on Si bare die with 0.5-A/W responsivity is bonding-wired to our control IC by hybrid chip-to-chip integration [32]. A portion of optical power for monitoring is coupled to a grating coupler and waveguide with a lensed fiber.

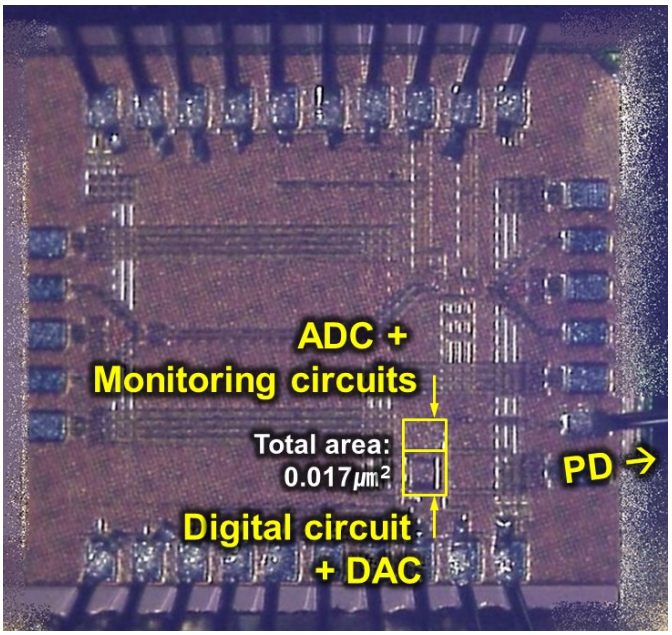


Figure 3-11. Photograph of bias controller IC chip

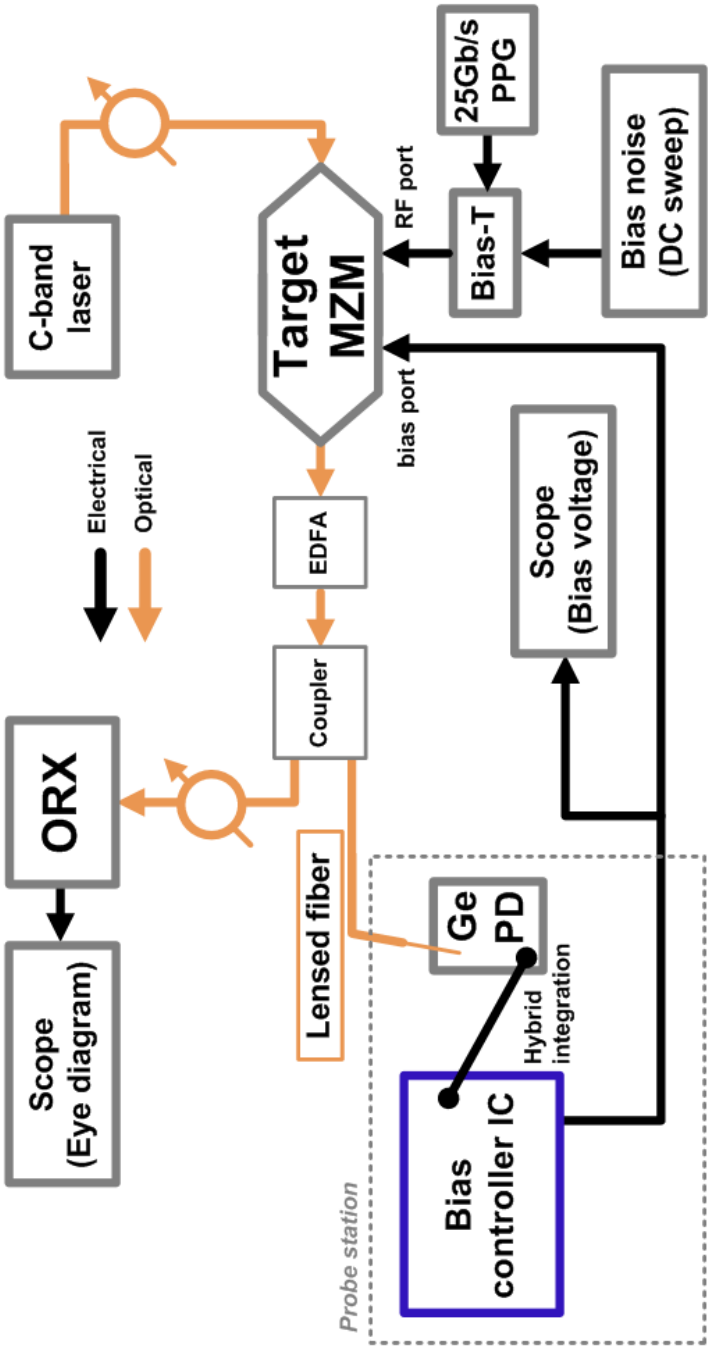


Figure 3-12. Measurement setup for demonstration of bias controller with 1550-nm MZM and hybrid-integrated Ge photodetector

The 1.2-V supply voltage is applied to the circuit except for the DAC, which uses a higher 2.6-V supply for that the MZM having 5-V V_π is to be provided with the wide bias control range. In the first step, the circuit consumes 3.69-mW power. In the second step with that the OMA monitoring circuit is turned off, it is only 1.59-mW, which is about 60 times better than chapter 2. The 16-kHz clock signal is introduced to the digital circuit, which speed can be slower as much as possible to minimize power consumption. However, the digital circuit can have up to several MHz control speed for reducing initial acquisition time with increased power consumption. In other words, there is a trade-off between initial acquisition time and power consumption. The ADC samples the optical average power with 1-MHz Σ-Δ modulation. Prior to the experiment, figure 3-13 shows DC characteristic curves of the target MZM and 25-Gb/s eye diagrams modulated with 2-V_{P2P} at several bias voltages.

In order to influence the MZM operation with an emulated external thermal drift, an intentional bias noise is introduced to the target MZM's RF port using a bias-T while the MZM is modulated with 25-Gb/s PRBS7 data and at the same time the modulated optical eyes are monitored. Figure 3-14 shows the measured bias voltages during the second step when the intentional bias noise is ramping with 1.7-V range

and speed of 5-mV/sec. As can be seen, our controller provides the expected ramped bias transient so that the MZM has the optimal bias. Figure 3-15 shows the eye diagrams during the figure 3-14 process. We can see the accumulated clean eye diagram compared to not introducing bias controller.

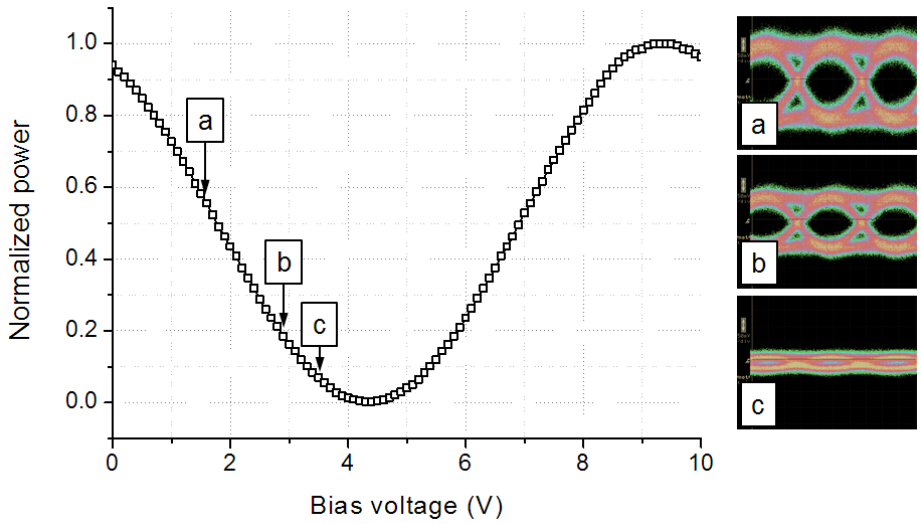


Figure 3-13. DC characteristic curves of 1550-nm MZM used in measurement and modulated eye diagrams according to three different bias voltages

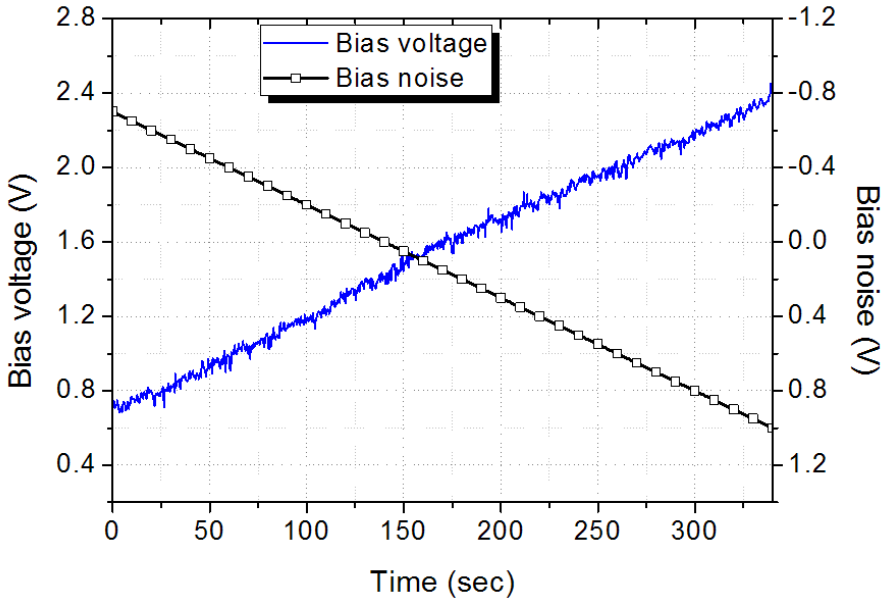


Figure 3-14. Bias noise transient into MZM RF port and measured MZM bias voltages determined by the bias controller

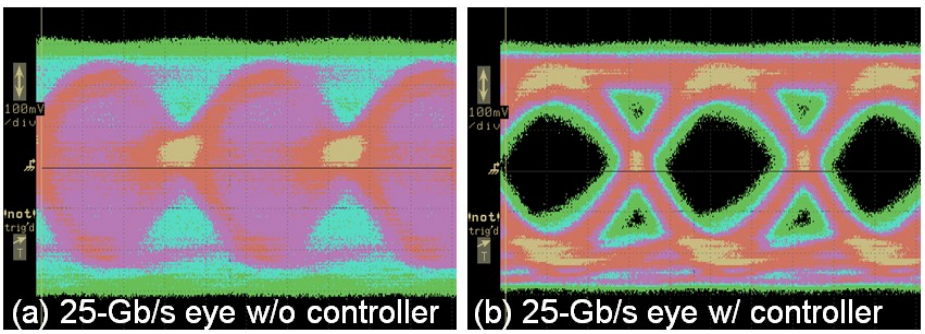


Figure 3-15. Measured eye diagrams of 25-Gb/s PRBS7 accumulated for 6 minutes (a) without and (b) with the bias controller while bias noises are supplied as shown in Figure 3-13

In order to influence the MZM operation with an emulated external

thermal drift, an intentional bias noise is introduced to the target MZM's RF port using a bias-T while the MZM is modulated with 25-Gb/s PRBS7 data and at the same time the modulated optical eyes are monitored. Figure 3-14 shows the measured bias voltages during the second step when the

MZM bias control circuit				
	Yupeng Li 2013 PTL [13]	Xiaoqi Zhu 2014 JLT [14]	**M.H.Kim 2016 PW**	**M.H.Kim 2017 PTL**
Technology	-	-	**0.25μm BiCMOS**	**28nm CMOS**
Integration	External (system level)	External (system level)	**Single chip**	**Single chip**
Data rate	10Gb/s	5GBoud	**3Gb/s**	**25Gb/s**
Power(mW)	N/A	N/A	**92.5**	**1.59**
Area(mm^2)	N/A	N/A	**0.083**	**0.017**
Control scheme	Harmonics power monitoring from **pilot tone**	Coherent detection from **pilot tone**	**OMA monitoring**	**OMA & Average power monitoring**

Table 3-1. Performance comparison with MZM bias controllers

Table 3-1 shows performance comparison with others MZM bias controllers. Unlike others demonstrations that are not yet integrated and needed a pilot tone, our circuit based on OMA monitoring is integrated into a single chip, resulting in outstanding power, area, and demonstration speed.

3.4. Summary

A new bias controller IC for MZM is demonstrated. Our bias controller monitors the OMA and average power of the MZM output optical power and automatically searches and maintains the optimum MZM bias voltage with two-step approach. A prototype IC chip realized in 28nm CMOS technology can successfully provide the bias control operation for 25-Gb/s data modulation of a 1550-nm MZM. This algorithm has a matter to be improved that when an input optical power is changed, optimal OMA and average power condition is mismatched, and then the control will be incorrect. However, our controller has great advantages of huge power saving and fast bias acquisition due to two split control steps. Furthermore, our controller still has a great potential of impact monolithic integration with Si MZM on the single Si wafer with its low power consumption and small chip size.

4. Improved Control Algorithm 2: Based on Low-Power OMA Monitoring

The MZM bias controller demonstrated in chapter 2 was a breakthrough in that it proposed a new algorithm that kept the OMA constantly maximum and showed the first integration into the single IC chip. The controller demonstrated in chapter 3 could improve initial acquisition time with a two-step approach and save power consumption with average power monitoring. However, the calibration method based on average power monitoring is still having problem that it cannot be maintained maximum OMA when the DC characteristic curve changes according to the input power variation. In case of MRM which easily occurs with the self-heating phenomenon according to input power, this situation is even worse.

In this chapter, we introduce and demonstrate an improved algorithm that can calibrate even input power variation while maintaining maximum OMA. For the demonstration, we set up the micro-ring modulator (MRM) as target modulator since the MRM is more sensitive to input power variation and has better integration efficiency than the MZM.

4.1. Si MRM Characteristics

From the viewpoint of Si photonics, the MRM having a radius of several micrometers is outstanding in terms of photonic-electronic integration density compared to the MZM which has a length of several millimeters. Moreover, its small size reduces the burden of loads on the modulator driver, which can be more high-speed modulation. However, as described in chapter 1.2., the MRM have significantly higher temperature dependences of the external temperature and input power than the MZM.

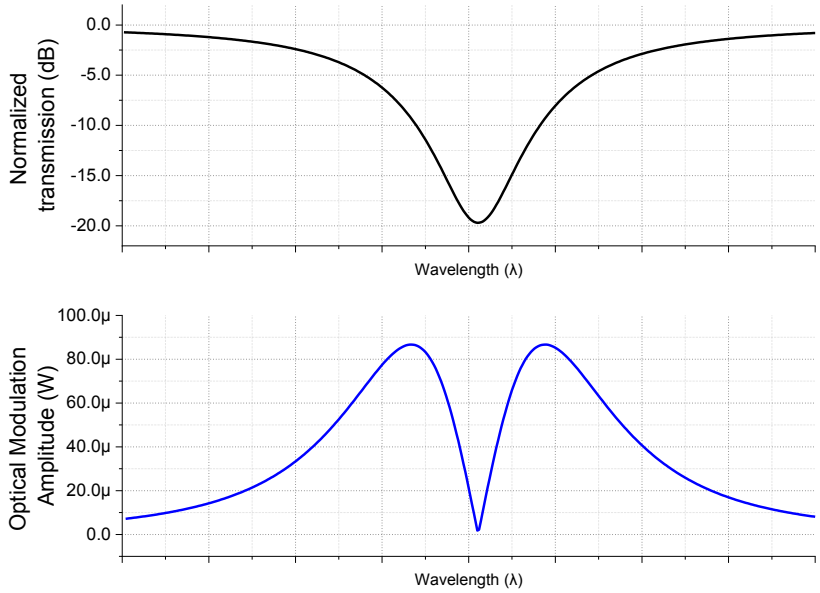


Figure 4-1. Si MRM spectra of normalized DC transmission with 0-V and OMA transmissions with ±4-V modulation

Figure 4-1 shows the MRM transmission curve and its relative OMAs of each wavelength. Through this plot, the MRM is characterized by the fact that it has two optimal wavelengths on both sides of the resonance. In particular, asymmetry occurs in the DC transmission curve with slight self-heating phenomenon. If the asymmetry occurs, the relative OMA at the left side optimal of the resonance becomes smaller but there is no bi-stable and the OMA of right side optimal of the resonance becomes larger but the bi-stability may become critical problem [34]. Therefore, this input power dependence must be considered in the control circuit design. These sensitive factors may become the disadvantages, and at the same time, they become the special reasons why the stabilization circuit is essential to MRMs.

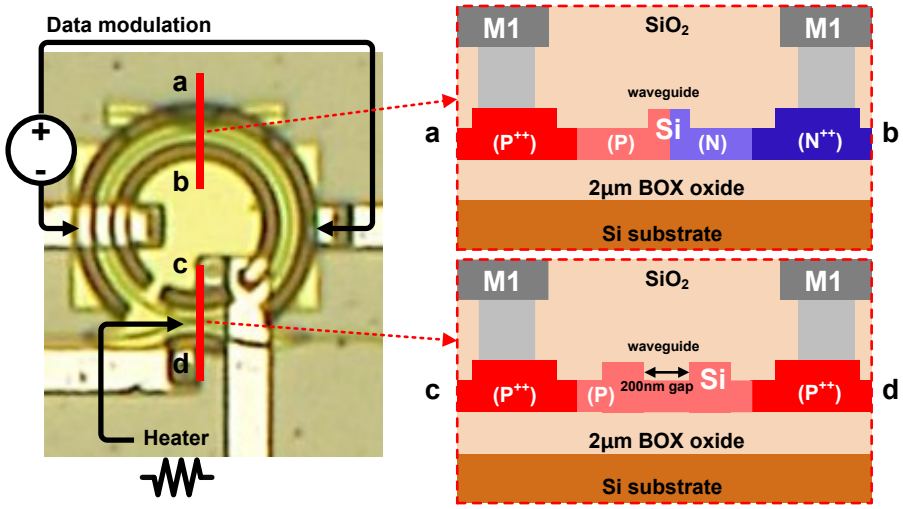


Figure 4-2. Physical structure and cross-sections of Si MRM

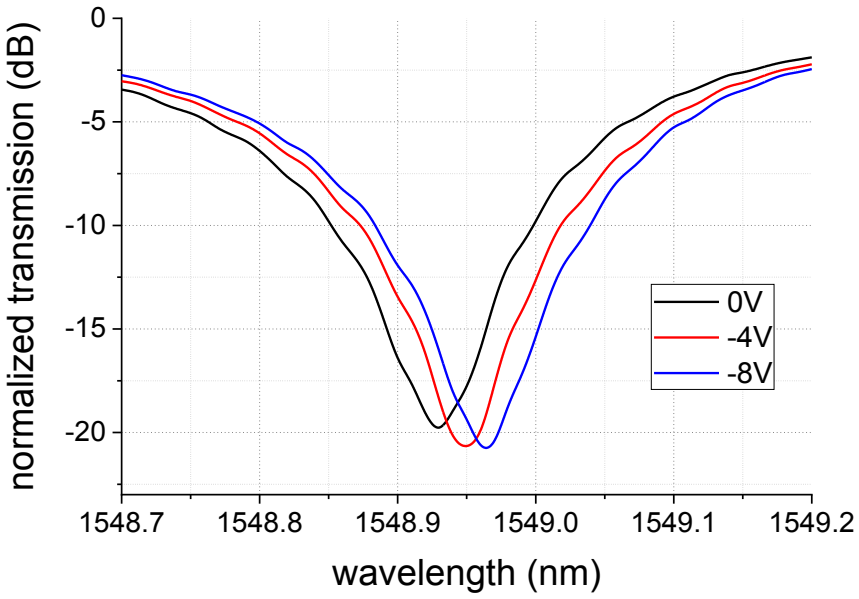


Figure 4-3. Si MRM transmission spectra according to three different DC biases

Figure 4-2 shows the physical structure and cross-sections of the MRM near modulation region and heater region respectively. A P-N reverse diode region mostly doped around the ring waveguide is used for optical modulation. The reversely bias electrical data changes the refractive index of the waveguide and optically modulates. Figure 4-3 shows the transmission curves according to the DC bias of the target MRM. According to results, electrical driving amplitude of a reverse 8-V_{P2P} can produce an OMA of about 26-μW_{P2P} for 1-mW input power.

A directly p-doped resistor on a portion of the ring waveguide can be used for the temperature control as a heater, which can raise the temperature inside the ring waveguide directly. Figure 4-4 shows an I-V curve and equivalent resistance of the heater and the resonance change of the MRM depending on the voltage applied to the heater. When the applied heater voltage is converted to electric power, the resonance shift of about 80-pm per mW can be achieved and if the maximum voltage to the heater is 3.3V, the whole control range of resonance wavelength is achieved about 440 pm, which corresponds to about 6-ºC in terms of temperature control range.

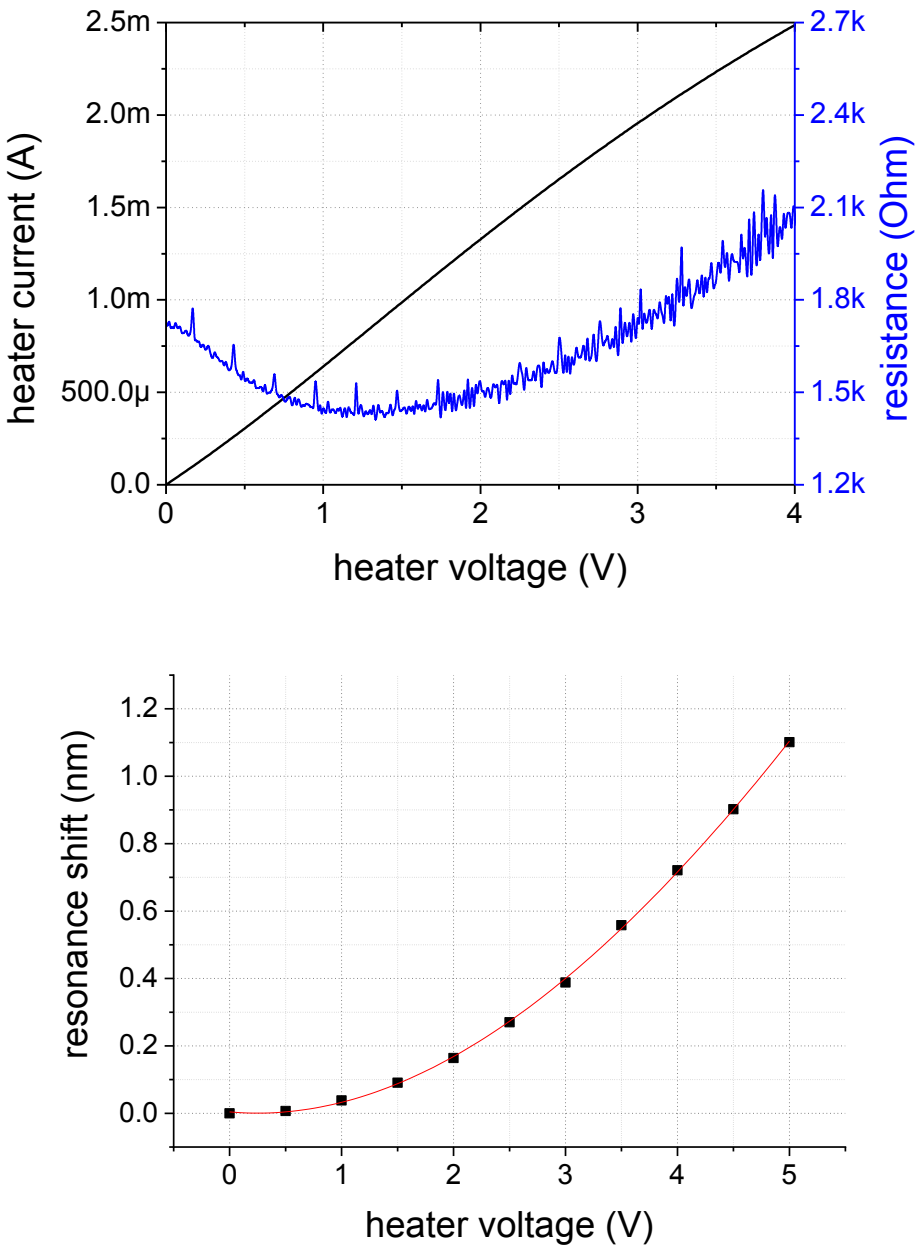


Figure 4-4. Heater I-V curve, resistance, and resonance wavelength change according to its voltages

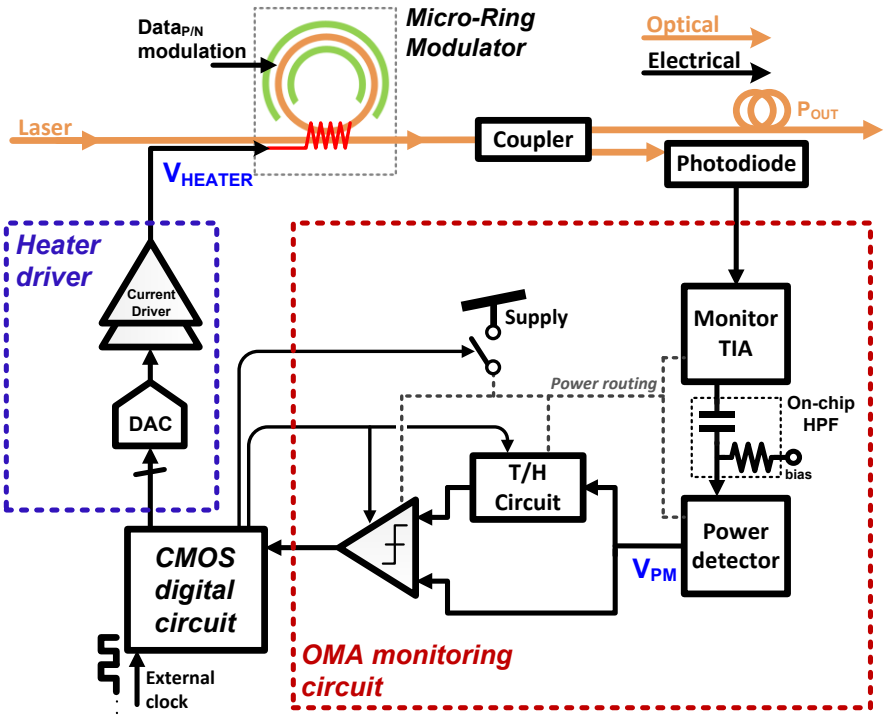


Figure 4-5. Block diagram of Si MRM wavelength (λ) stabilization circuit based on low-power OMA monitoring

4.2. Control Strategy

As introduced in chapter 1.3.2., this control circuit is called a wavelength stabilization circuit (λ-stabilization circuit) in academia [20-22] in terms of controlling the resonance wavelength which is a unique characteristic of MRM. Although the name is different from the MZM bias controller, the λ-stabilization circuit has the same control objective in that they must optimize OMA adaptively from external environment changes. In this chapter, we use the continuous-time OMA monitoring method described in chapter 2 without using the average power monitoring described in chapter 3, which is introduced to provide unconditional optimized OMA for any external variations.

However, this method has a long initial acquisition time and huge power consumption. To overcome the long acquisition time, a two-step approach (initial scan and control) is applied. A power detector structure instead of a high-speed rectifier is used to monitor high-speed signal having OMA information for saving power consumption. Additionally, since the TIA still occupies a large power portion due to its high-speed operation, we design the OMA monitoring circuit periodically turned on-and-off for saving more power. While the OMA monitoring circuit is turned off, the calibration operation pauses for a

few hundreds of millisecond. This periodical turn on-and-off is based and used on the fact that since the change speed of external temperature and input power is not as fast as several kilohertz, there is no need for continuous calibration of tens of kHz.

Figure 4-5 shows the whole block diagram of a control circuit. The λ-stabilization circuit is divided into an OMA monitoring circuit and a heater control circuit. The OMA monitoring circuit consists of high-speed TIA, power detector, T/H circuit and comparator. The signal from the control circuit is applied to the regulator to turn on-and-off the high-speed circuit. The heater control circuit consists of DAC and CMOS digital circuit. The DAC is designed to drive about killo-Ohm resistor (heater) using digital bits. The CMOS digital circuit is designed as verilog-HDL, synthesized at the gate-level, and placed and routed (PnR) to analog circuits. The detailed circuit description is described in chapter 4.3.

4.2.1. Initial Voltage Scan (First Step)

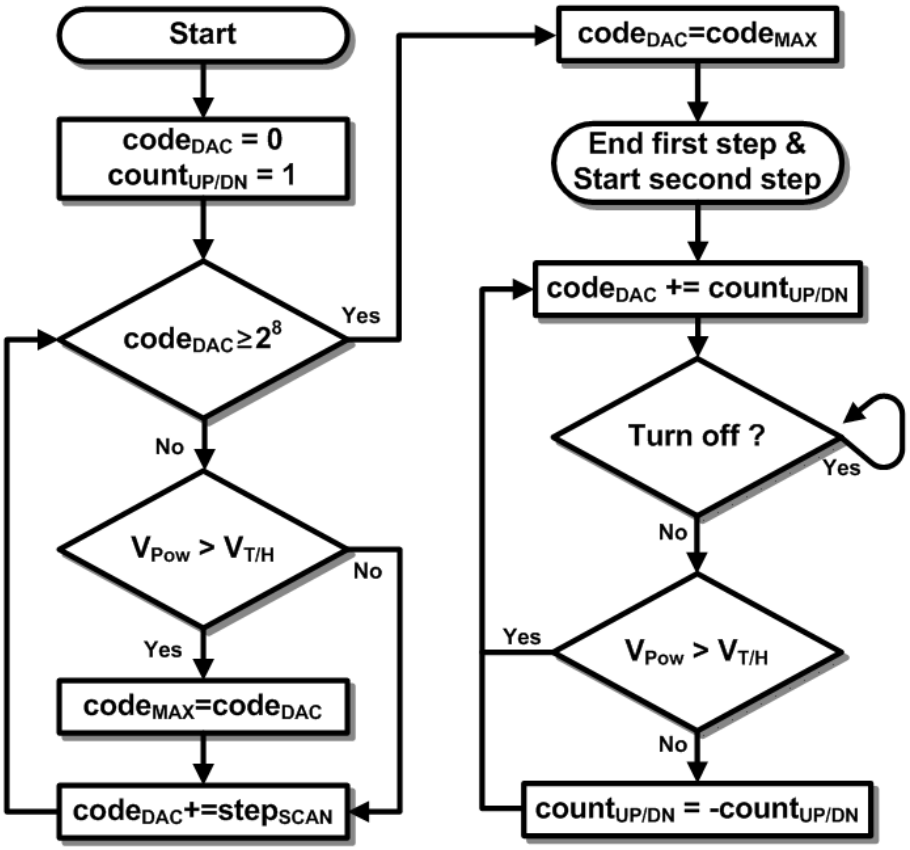


Figure 4-6. Algorithm flowchart of two-step approach based on low-power OMA monitoring

Figure 4-6 shows a flowchart of the whole control process. When the λ-stabilization circuit is turned on, it scans the entire heater voltage range, which depends to supply voltage and DAC bit (3.3-V and 2^8-bit in this design). The number of bit step used in the scan ($Step_{SCAN}$) is

adjustable to reduce the scan time depending on the situation. In this design, we use 4-bit for $Step_{SCAN}$. After each time you increase $Step_{SCAN}$ step by step, you can compare OMA state by present with one step past. If the present heater voltage generates better OMA than the past one, so the digital controller registers the present DAC code ($code_{DAC}$) to a maximum OMA code ($code_{MAX}$). If not, it skips updating $code_{MAX}$. The scan is repeated until $code_{DAC}$ reaches the maximum value. When the scan is finished, the coarsely optimized heater voltage will be determined and stored in the $code_{MAX}$ in bit form. This first step is similar to chapter 3's one, but it is slightly different in that at the moment to the second step it keeps OMA monitoring without handing over to average power monitoring.

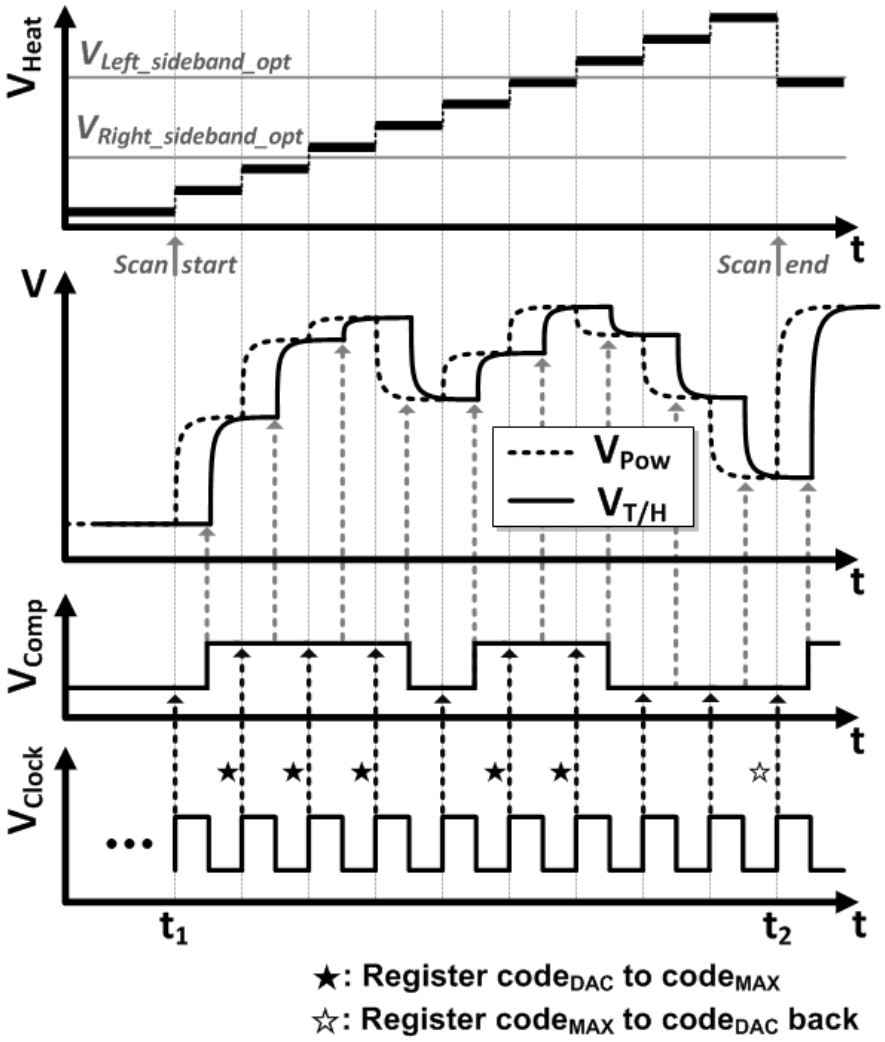


Figure 4-7. Timing diagram of initial bias scan step (First step)

Figure 4-7 shows the timing diagram in the first step. V_{HEAT} is the MRM heater voltage provided by the $code_{DAC}$, V_{POW} is the output voltage of the power detector, $V_{T/H}$ is the output of the T/H circuit which holds V_{POW} at half period of a clock cycle, V_{COMP} is the output of

the negative-edge triggered comparator, and V_{Clock} is clock signal to the control circuit. When the scan begins at t_1, V_{HEAT} will pass through two voltages representing the left and right optimal. Since the higher optimum voltage is the left side optimum of the MRM we want, it must be scanned in a direction that increases the voltage so that it is stored in the $code_{MAX}$. At the moment with the star sign (★), V_{POW} is larger than $V_{T/H}$, that is, the present heater voltage is producing better OMA than the past one, so that the $code_{DAC}$ is registered to the $code_{MAX}$. After the whole scan range, at the end of the scan (t_2 with ☆) the $code_{MAX}$ is registered back to the $code_{DAC}$ with the coarsely optimized OMA, and then the low-power continuous-time calibration (second step) begins.

4.2.2. Low-Power Continuous-Time Calibration (Second Step)

Although the second step starts, the comparator continuously compares V_{POW} to $V_{T/H}$ and calibrates heater voltage. This process is very similar to the method described in chapter 2, however, it has advantages in that it has digitally up-and-down bit counting for small dithering and that there is a turn-off time interval to save power consumption.

Figure 4-8 shows the timing diagram in the second step. During the second step, there is a 'turn-off interval'. The calibration clock speed of the circuit requires at least few kHz due to fast initial acquisition time and leakage current of the T/H circuit et al. However, since the external temperature change and the input power change do not change in units of several kHz, the monitoring circuit is wasted by fast calibration. Therefore, we design quite a long turn-off time, which improves the monitoring power saving more than half compared to when I keep it continuously turn on. In details, a 1-ms control clock period is used to the continuous changing the counting polarity with ±1bit dithering near the optimum heater voltage. This calibration time is only for 125-ms out of 1000-ms turn on-and-off periods, that is, the calibration will only

be active for 1/8 of the time and the heater voltage will be maintained for the turn-off period.

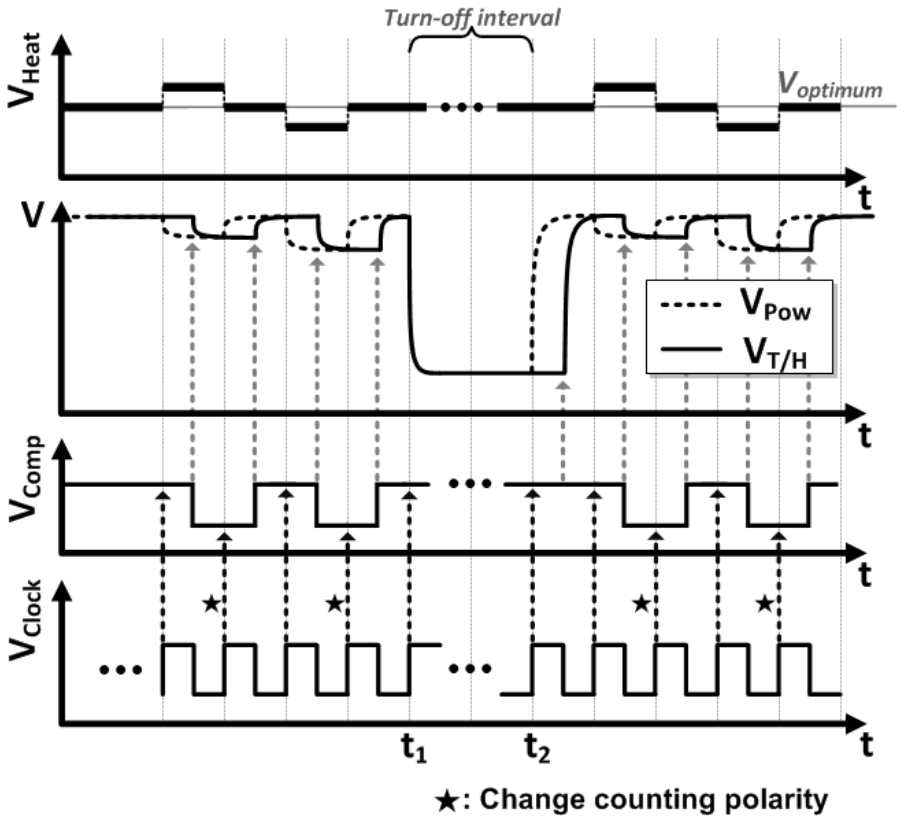


Figure 4-8. Timing diagram of low-power continuous-time calibration step (Second step)

4.3. Implementation

The OMA monitoring circuit consists of high-speed trans-impedance amplifier (TIA), on-chip high-pass filter (HPF), power detector, track and hold (T/H) circuit and comparator. The TIA converts a photocurrent provided by the monitoring photodiode into a voltage signal and the power detector produces a DC voltage corresponding to the amplitude of an AC-coupled TIA output signal.

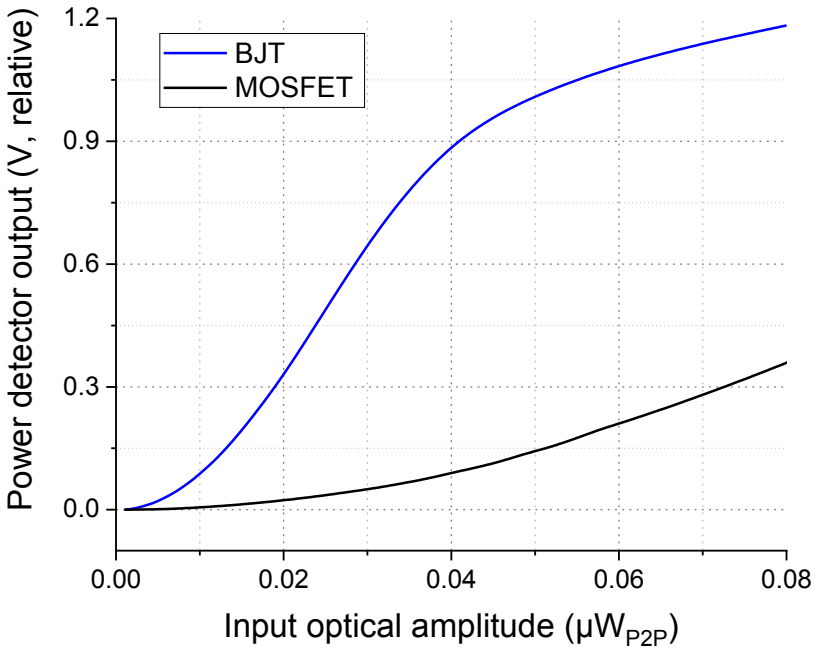


Figure 4-9. Simulation comparison between CMOS and BJT according to input pair on power detector

In case of the power detector, BJTs are used instead of MOSFETs for input pair transistors since the BJT has a larger trans-conductance change to the input swing amplitude than MOSFET. Figure 4-9 shows the simulation comparison of power detectors, which depend on the input pair of MOSFET and BJT in the same BiCMOS process. In the predicted range, the power detector using BJT shows a DC output voltage change about twice as high as that using MOSFET.

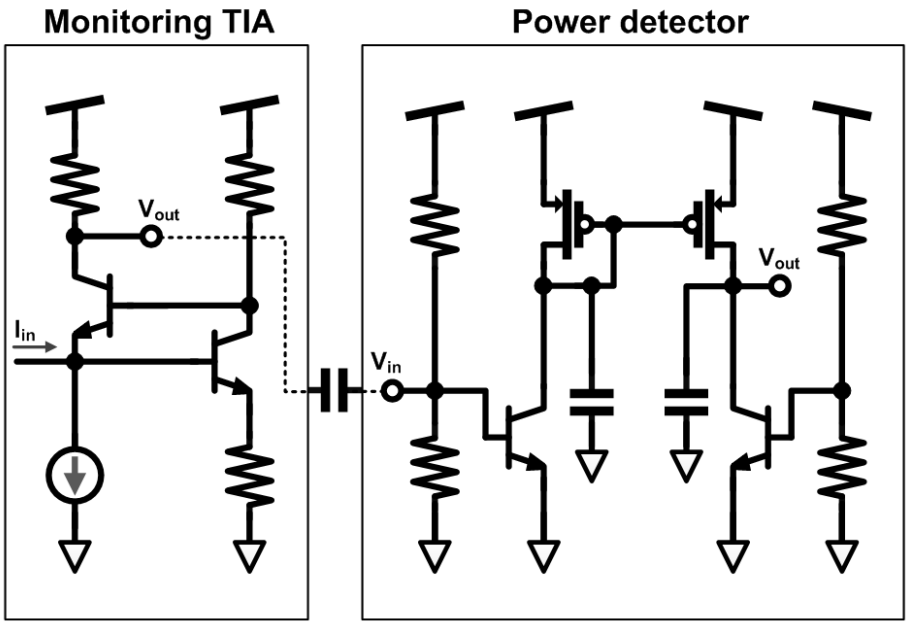


Figure 4-10. Schematic of regulated-cascode TIA and power detector based on BJT

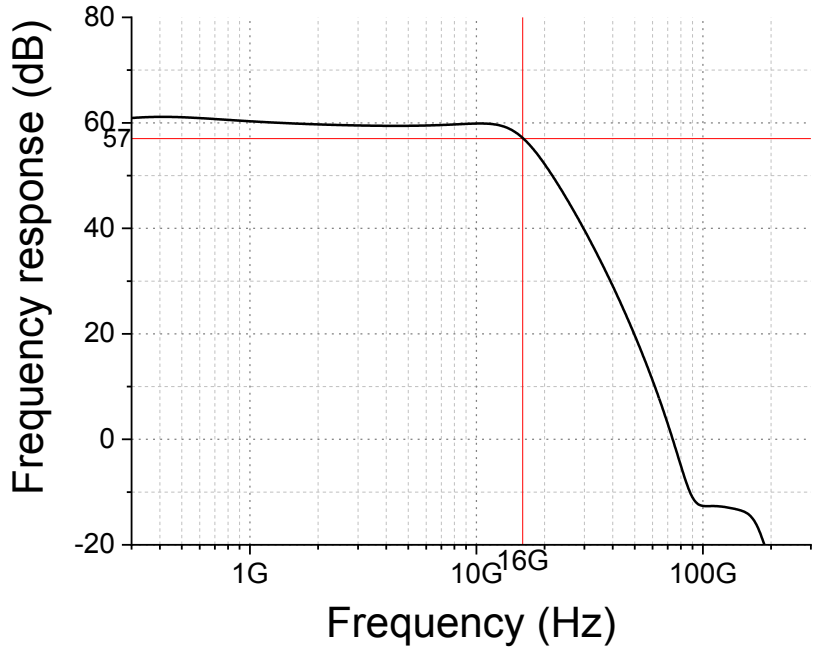


Figure 4-11. Post-layout frequency response simulation result of TIA

Figure 4-10 shows a block diagram of the TIA and power detector used in the circuit. The TIA selects a regulated cascode structure since which can be used for high-speed application with low-input impedance and high gain-bandwidth product [35]. Figure 4-11 shows a simulated frequency response of the TIA, which has 60-dBΩ DC gain and 16GHz bandwidth. This value is sufficient to monitor clean eye of a 25-Gb/s optical signal. The output of the power detector having the OMA information enters the T/H circuit and the comparator of the same structure as that used in chapter 2.

```
// Digital controller for low–power OMA monitoring algorithm
always@(posedge dacclock or negedge resetn) begin

if(!resetn) begin
        code <= 9'b000_000_000;
        maxcode <= 9'b000_000_000;
        mode <= 1'b0;
        count <= 1'b1;
end

else begin

        if(mode==1'b0) begin
                code <= code + 4;
                case({compout,code[8]})
                2'b00: mode <= 1'b0;
                2'b10: maxcode <= code;
                2'b01: begin code <= maxcode; mode<=1'b1; end
                2'b11: begin code <= maxcode; mode<=1'b1; end
                endcase
        end

        else begin // control mode
                if(turnoff[0]==1'b0) begin
                case({compout,polarc})
                2'b00: begin code <= code + 1; count <= !count; end
                2'b01: begin code <= code - 1; count <= !count; end
                2'b10: code <= code -1;
                2'b11: code <= code +1;
                endcase
                end
```

```
        end


end


end
```

Figure 4-12. Register-transfer level verilog-HDL code (only ‘always@’ blocks) for synthesizing digital circuit based on low-power OMA monitoring

The comparator output enters the digital circuit synthesized, placed, and routed computer-based on a RTL-level verilog-HDL, which is mostly same design process in chapter 3.2 except to that it is based on 0.25-μm CMOS logic gates. Figure 4-12 shows the used verilog-HDL RTL-level code, which shows that the circuit determines the DAC code while operating the initial scan step and the continuous-time calibration step, subsequently.

Figure 4-13 shows a block diagram of the DAC driving the heater. It is designed based on the R-2R ladder structure which is same with chapter 3.2. The heater driving by the DAC is composed of a p-type doping resistor, which resistance is about 1.7-kΩ, so that the regulator type output driver is used for low-output impedance.

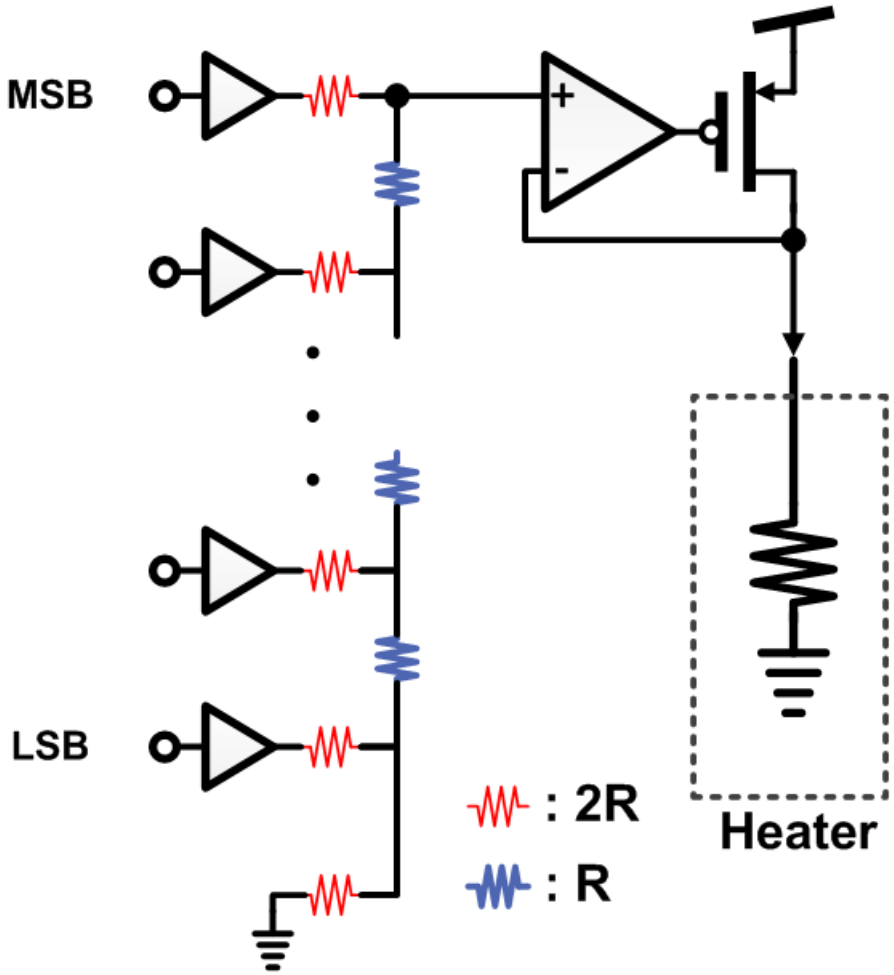


Figure 4-13. Schematic of DAC with regulator-type output buffer

4.4. Measurement Results

Figure 4-14 shows the IC chip photograph of the λ-stabilization circuit and its area is approximately 0.086-mm^2. Most area is from synthesized digital circuit, which can be shrunk with more fine CMOS process.

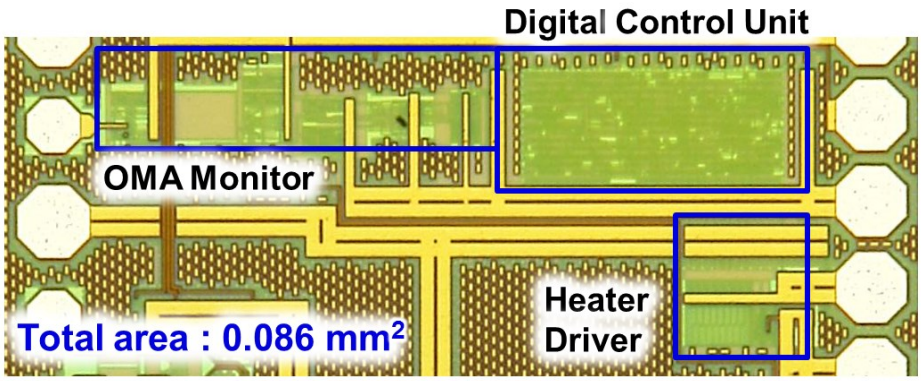


Figure 4-14. Photograph of λ-stabilization IC chip

In this measurement, we aimed at two demonstrations of whether the bias calibration is well done with the clean eye for a long time changes according to the external temperature and input laser power. Figure 4-15 shows the measurement setup. A 1550-nm grating coupler with about 4-dB loss is used for the Si MRM. The 1-mW optical power is coupled to the input of the ring modulator through the Si waveguide on the chip die through the fiber array, and then the depletion-biased

differential data of 4-V_{P2P} from 50-ohm matched transmitter equipment is modulated to optical signal. This signal is connected to 1:1 optical coupler, AGC mode EDFA, and commercial photodiode, which output is probed to our wavelength stabilization circuit through the chip-on-board (COB) of FR4 board.

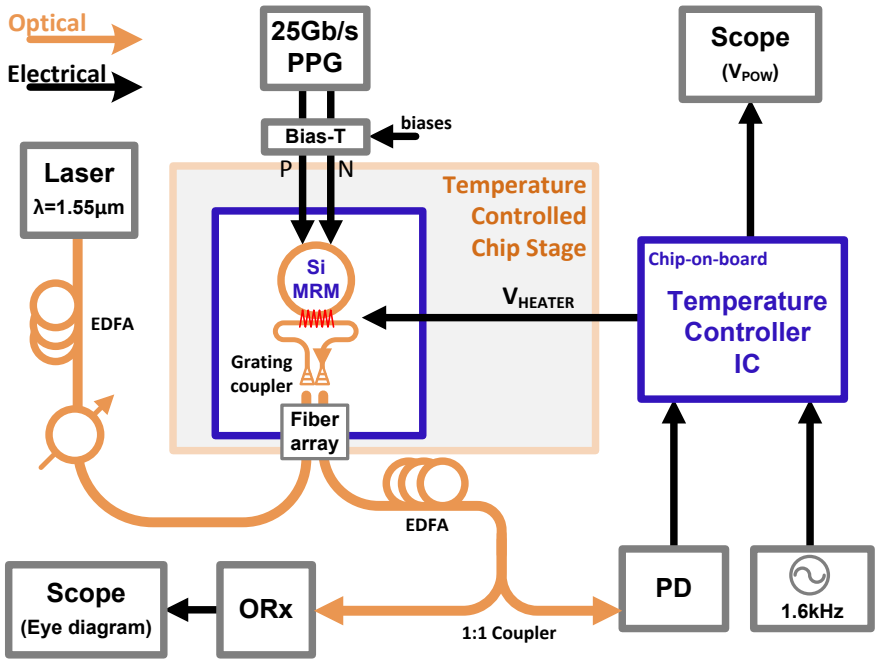


Figure 4-15. Measurement setup for demonstration of λ-stabilization circuit for Si MRM

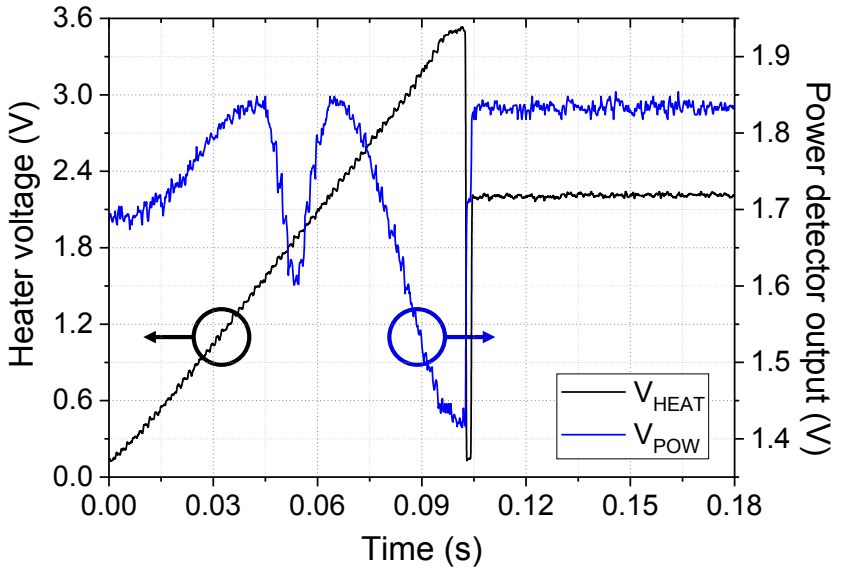


Figure 4-16. Measured transient response of power detector's output according to heater voltage at first initial scan step

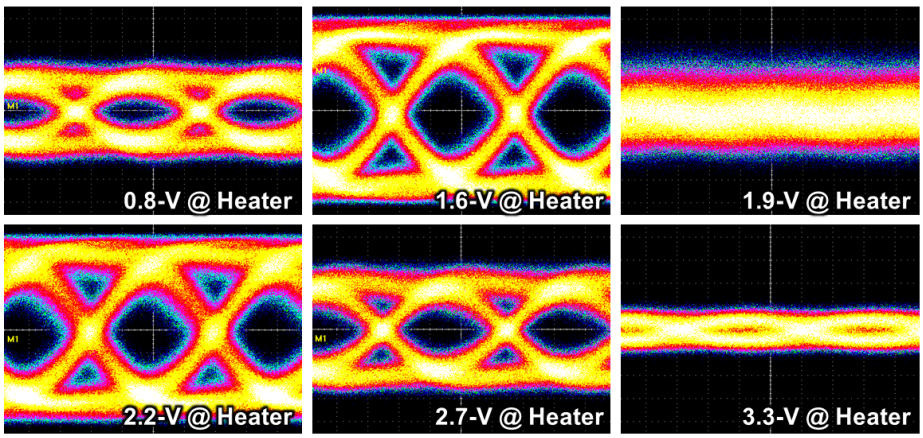


Figure 4-17. Measured eye diagrams according to six different heater voltages

Prior to two variation measurements (external temperature and input power) mentioned above, figure 4-16 shows the measured heater voltage and power detector's output of the initial scan step just after circuit reset. We can see the power detector output voltage passing two optimal heating conditions of that the right optimum at 1.6-V and the left optimum at 2.2-V. The number of coarse scan step is 4, which causes the coarse acquisition time to about 64-ms. Figure 4-17 is the measured eye diagrams according to the several heater voltage conditions. From the control algorithm, the last found maximum OMA must be our initial acquisition condition, so the heater voltage can start the calibration at the left optimal of the resonance as we want.

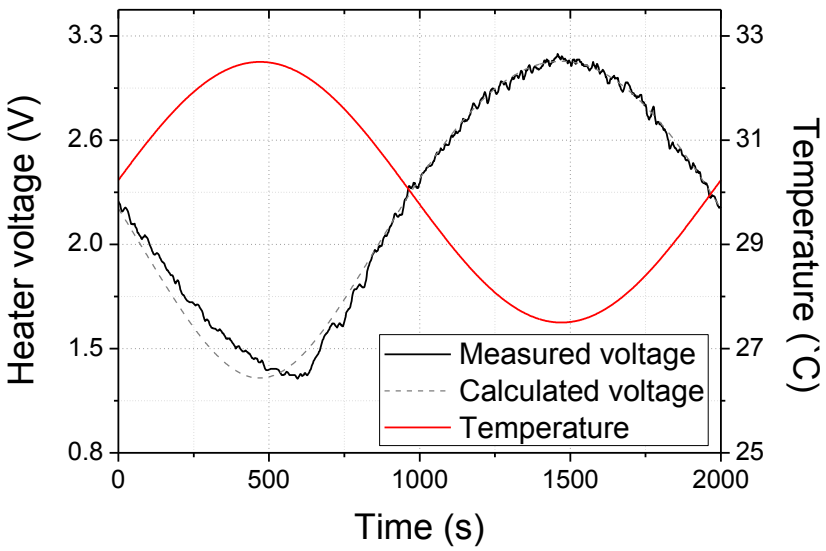
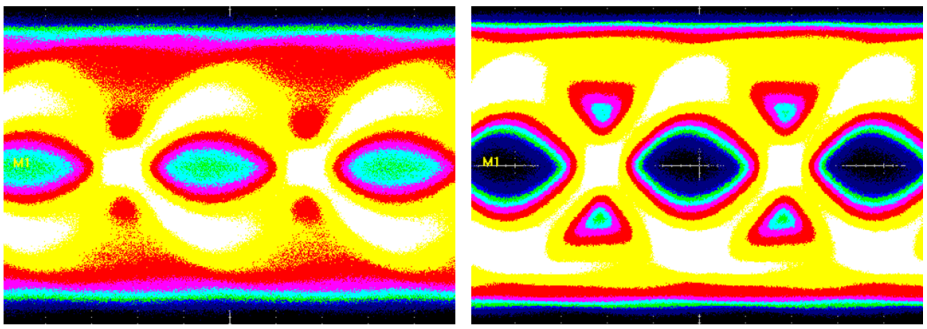


Figure 4-18. External temperature variations to Si MRM and measured heater voltages controlled by the λ-stabilization circuit



25-Gb/s PRBS7 eye diagram accumulated for 33.3 min **without controller**

25-Gb/s PRBS7 eye diagram accumulated for 33.3 min **with controller**

Figure 4-19. Measured eye diagrams of 25-Gb/s PRBS7 accumulated for 33.3 min (a) without and (b) with the λ-stabilization circuit while external temperature variations are supplied as shown in figure 4-20

Figure 4-18 shows the measurement results of the heater voltage curve when the external temperature is changed. Figure 4-19 shows the accumulated eye diagram during that time. To change the external temperature of the Si MRM, we used a device to control the temperature of the stage plate on which the photonic IC chip was mounted. According to the results, the 5-ºC temperature change corresponding to the resonance wavelength change of about 400-pm can be calibrated and the clean eye can be also maintained for about 30 minutes.

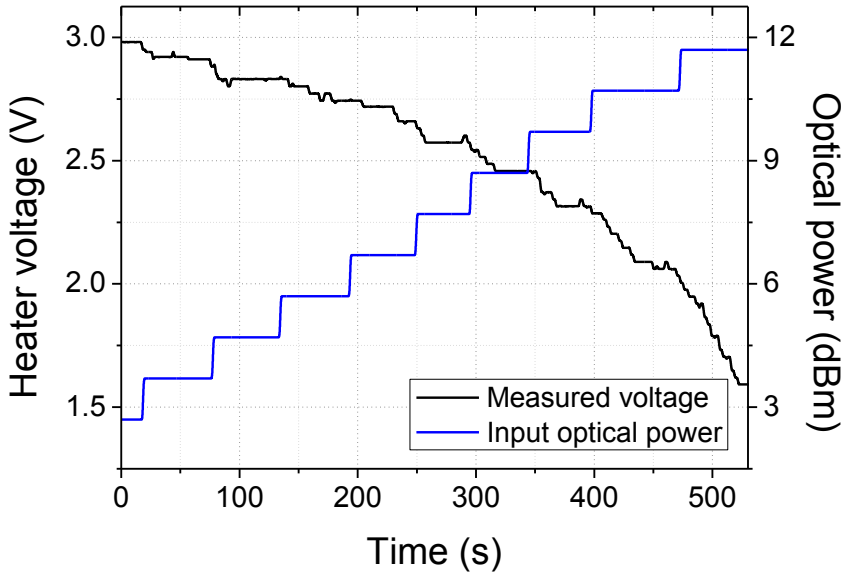
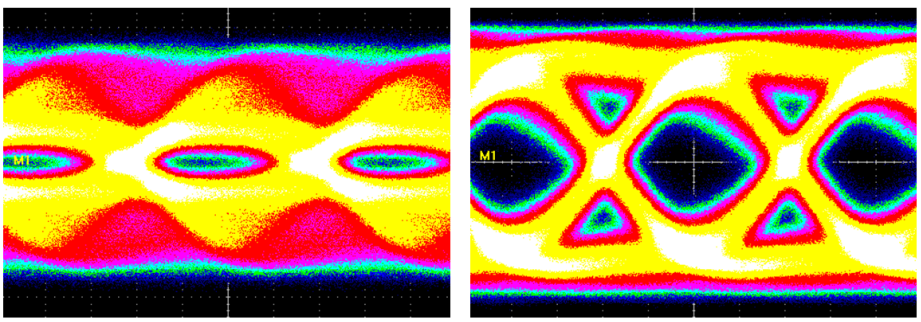


Figure 4-20. Input optical power variations to Si MRM and measured heater voltages controlled by the λ-stabilization circuit



25-Gb/s PRBS7 eye diagram accumulated for 9 min **without controller**

25-Gb/s PRBS7 eye diagram accumulated for 9 min **with controller**

Figure 4-21. Measured eye diagrams of 25-Gb/s PRBS7 accumulated for 9 min (a) without and (b) with the λ-stabilization circuit while input optical power variations are supplied as shown in figure 4-22

Figure 4-20 shows the measurement results of the heater voltage curve when the input power is changed so self-heating is worse. Figure 4-21 also shows the accumulated eye diagram during that time. Using optical attenuator before Si MRM, the input optical power to Si MRM was adjusted more and more strongly at about 1 minute intervals. According to the results, about 10 dB input power variation can be calibrated and the clean eye can be also maintained for about 9 minutes.

MRM wavelength stabilization circuit					
	K. Padmaraju 2013ECOC [18]	Hao Li 2015JSSC [20]	Chen Sun 2016JSSC [21]	S. Agarwal 2016JSSC [22]	**M.H.Kim**
Technology	-	65nm CMOS	45nm CMOS-SOI	40nm CMOS	**0.25μm BiCMOS**
Integration w/ photonics	External (system level)	Wire bond	Single chip	Flip chip	**External**
Demo. Datarate	5-Gb/s	25Gb/s	5Gb/s	2Gb/s	**25Gb/s**
Power (mW, excl. heater)	N/A	N/A	0.72	2.9	**3.91**
Area (mm^2)	N/A	N/A	0.003	0.017	**0.086**
Control scheme	Error signal monitoring from dithering	Resonance auto-align based on average power monitor	Transmitted bit-referred statistics	OMA monitoring w/ slope quantization	**Two-step approach OMA monitoring**

Table 4-1. Performance comparison with Si MRM wavelength stabilization circuits

Table 4-1 shows performance comparison with others Si MRM wavelength stabilization circuits. The total power consumption of our

circuit is 3.91-mW (excluding heater), which represent remarkable improvement of about 24 times compared to chapter 2 of the same technology. Considering that it uses 0.25-μm minimum gate length, it is expected that it will be more improved with higher CMOS technology. For example, when we use 45-nm CMOS technology having lower dynamic power due to shrunk gate length and supply voltage, it is expected to be 0.25-mW. This power is sufficiently competitive with low power designs compared to other results.

4.5. Summary

A new wavelength stabilization IC for Si MRM is demonstrated. Our bias controller directly monitors the OMA of the Si MRM output optical power and automatically searches and maintains the optimal heater voltage with low-power two-step approach. A prototype IC chip realized in 0.25-μm BiCMOS technology can successfully provide the resonance wavelength control for 25-Gb/s data modulation of a 1550-nm Si MRM. It can seem that it consumes still quite power due to the gate length and high supply voltage of the CMOS technology and that the control range is narrow due to the low heater efficiency of resonance wavelength transfer. However, our circuit and algorithm has a great advantage that it can always be optimal from any external environmental changes such as temperature and input optical power. Furthermore, our stabilization circuit has a huge potential of monolithically integrated Si optical full-transmitter with small Si MRM in the single Si wafer with its low power and extremely small chip size.

5. Conclusion

In this dissertation, several algorithms for temperature stabilization of optical modulators are demonstrated with commercial MZMs and Si MRM. These algorithms based on OMA and sometimes average power monitoring are realized using integrated photodetector, monitoring TIA, and power detector. Based on the monitored OMA or optical power information, several CMOS circuitry including synthesized digital circuitry stabilizes MZM bias or Si MRM resonance wavelength. As this is an indispensable circuit for practical use of optical transmitter, smart design with a low-power and a fast initialization is considered on various external environment changes. Prototype IC chips realized in CMOS or BiCMOS technology successfully provide control of bias or heater voltage for stable 25-Gb/s data modulation of MZM or Si MRM. These realized IC chips will be expected to have a great potential of monolithic integration with Si optical full-transmitter based on Si MZM or MRM on the single Si wafer.

Bibliography

[1] G. P. Agrawal, “Fiber-optic communication systems,” vol. 222. John Wiley & Sons, 2012.

[2] C. Gunn, “CMOS photonics for high-speed interconnects,” *IEEE Micro.*, vol. 26, no. 2, pp. 58–66, Mar./Apr. 2006.

[3] M. Hochberg, N. C. Harris, R. Ding, Y. Zhang, A. Novack, Z. Xuan, and T. Baehr-Jones, “Silicon photonics: The next fabless semiconductor industry,” IEEE Solid-State Circuits Mag., vol. 5, no. 1, pp. 48–58, Mar. 2013.

[4] D. A. B. Miller, “Device requirements for optical interconnects to silicon chips,” *Proc. IEEE*, vol.97, no. 7, pp. 1166–1185, Jul. 2009.

[5] I. A. Young, E Mohammed, J. T. S. Liao, A. M. Kern, S. Palermo, B. A. Block, M. R. Reshotko, and P. L. D. Chang, “Optical I/O technology for tera-scale computing,” *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 235–248, Jan. 2010.

[6] J.-S. Youn, M.-J. Lee, K.-Y. Park, and W.-Y. Choi, “10-Gb/s 850-nm CMOS OEIC receiver with a silicon avalanche photodetector,” IEEE J. Quantum Electron., vol. 48, no. 2, pp. 229–236, Feb. 2012.

[7] William M. J. Green, Michael J. Rooks, Lidija Sekaric, and Yurii A. Vlasov, "Ultra-compact, low RF power, 10 Gb/s silicon Mach-Zehnder modulator," Opt. Express 15, 17106-17113 (2007)

[8] Jean Paul Salvestrini, et al., "Analysis and Control of the DC Drift in LiNbO3-Based Mach-Zehnder Modulators," J. Lightwave Technol. 29, 1522-1534 (2011)

[9] Bogaerts, Wim, et al. "Silicon microring resonators." Laser & Photonics Reviews 6.1 (2012): 47-73.

[10] B. E. Little, S. T. Chu, H. A. Haus, J. Foresi and J. P. Laine, "Microring resonator channel dropping filters," in Journal of Lightwave Technology, vol. 15, no. 6, pp. 998-1005, Jun 1997.

[11] M. J. Shin, Y. Ban, B. M. Yu, J. Rhim, L. Zimmermann and W. Y. Choi, "Parametric Characterization of Self-Heating in Depletion-Type Si Micro-Ring Modulators," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 22, no. 6, pp. 116-122, Nov.-Dec. 2016.

[12] K. Sekine, C. Hasegawa, N. Kikuchi and S. Sasaki, "A Novel Bias Control Technique for MZ Modulator with Monitoring Power of Backward Light for Advanced Modulation Formats," OFC/NFOEC 2007 - 2007 Conference on Optical Fiber Communication and the National Fiber Optic Engineers Conference, Anaheim, CA, 2007, pp. 1-3.

[13] Y. Li, Y. Zhang and Y. Huang, "Any Bias Point Control Technique for Mach–Zehnder Modulator," in IEEE Photonics Technology Letters, vol. 25, no. 24, pp. 2412-2415, Dec.15, 2013.

[14] Xiaoqi Zhu, Zhennan Zheng, Cheng Zhang, Lixin Zhu, Zhenning Tao, and Zhangyuan Chen, "Coherent Detection-Based Automatic Bias Control of Mach–Zehnder Modulators for Various Modulation Formats," J. Lightwave Technol. 32, 2502-2509 (2014)

[15] C. T. DeRose, M. R. Watts, D. C. Trotter, D. L. Luck, G. N. Nielson, and R. W. Young, "Silicon Microring Modulator with Integrated Heater and Temperature Sensor for Thermal Control," in Conference on Lasers and Electro-Optics 2010, OSA Technical Digest (CD) (Optical Society of America, 2010), paper CThJ3.

[16] A. H. Atabaki, E. Shah Hosseini, A. A. Eftekhar, S. Yegnanarayanan, and A. Adibi, "Optimization of metallic microheaters for high-speed reconfigurable silicon photonics," Opt. Express 18, 18312-18323 (2010)

[17] S. Xiao, M. H. Khan, H. Shen and M. Qi, "Silicon-on-Insulator Microring Add-Drop Filters With Free Spectral Ranges Over 30 nm," in Journal of Lightwave Technology, vol. 26, no. 2, pp. 228-236, Jan.15, 2008.

[18] Padmaraju, Kishore and Keren Bergman. "Resolving the thermal challenges for silicon microring resonator devices" Nanophotonics, 3.4-5 (2013): 269-281. Retrieved 2 Apr. 2018

[19] Vilson R. Almeida and Michal Lipson, "Optical bistability on a silicon chip," Opt. Lett. 29, 2387-2389 (2004)

[20] H. Li et al., "A 25 Gb/s, 4.4 V-Swing, AC-Coupled Ring Modulator-Based WDM Transmitter with Wavelength Stabilization in 65 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 50, no. 12, pp. 3145-3159, Dec. 2015.

[21] C. Sun et al., "A 45 nm CMOS-SOI Monolithic Photonics Platform With Bit-Statistics-Based Resonant Microring Thermal Tuning," in IEEE Journal of Solid-State Circuits, vol. 51, no. 4, pp. 893-907, April 2016.

[22] S. Agarwal, M. Ingels, M. Pantouvaki, M. Steyaert, P. Absil and J. Van Campenhout, "Wavelength Locking of a Si Ring Modulator Using an Integrated Drop-Port OMA Monitoring Circuit," in IEEE Journal of Solid-State Circuits, vol. 51, no. 10, pp. 2328-2344, Oct. 2016.

[23] F.-P. Chou et al., “Silicon photodiodes in standard CMOS technology,” IEEE J. Sel. Topics Quantum Electron., vol. 17, no. 3, pp. 730–740, May/Jun. 2011.

[24] M. J. Lee and W. Y. Choi, "Performance Optimization and Improvement of Silicon Avalanche Photodetectors in Standard CMOS Technology," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 24, no. 2, pp. 1-13, March-April 2018.

[25] H. Y. Jung, J. M. Lee and W. Y. Choi, "A high-speed CMOS integrated optical receiver with an under-damped TIA," 2015 IEEE Photonics Conference (IPC), Reston, VA, 2015, pp. 347-350.

[26] A. S. Bakhtiar, M. S. Jalali and S. Mirabbasi, "A high-efficiency CMOS rectifier for low-power RFID tags," 2010 IEEE International Conference on RFID (IEEE RFID 2010), Orlando, FL, 2010, pp. 83-88.

[27] B. Wicht, T. Nirschl and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," in IEEE Journal of Solid-State Circuits, vol. 39, no. 7, pp. 1148-1158, July 2004.

[28] C. Eichenberger and W. Guggenbuhl, "Dummy transistor compensation of analog MOS switches," in IEEE Journal of Solid-State Circuits, vol. 24, no. 4, pp. 1143-1146, Aug 1989.

[29] Jae-Shin Lee, Min-Sun Keel, Shin-Il Lim and Suki Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," in Electronics Letters, vol. 36, no. 23, pp. 1907-1908, 9 Nov 2000.

[30] K. Park and W. S. Oh, "A 40-Gb/s 310-fJ/b Inverter-Based CMOS Optical Receiver Front-End," in IEEE Photonics Technology Letters, vol. 27, no. 18, pp. 1931-1933, Sept.15, 15 2015.

[31] S. Sakphrom and A. Thanachayanont, "A low-power CMOS RF power detector," 2012 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2012), Seville, 2012, pp. 177-180.

[32] J. M. Lee, et al., “Series Resistance Influence on Performance of Waveguide-Type Germanium Photodetectors on Silicon,” in Chin. Opt. Lett., vol. 15, issue 10, 2017.

[33] Qianfan Xu and Michal Lipson, "Carrier-induced optical bistability in silicon ring resonators," Opt. Lett. 31, 341-343 (2006)

[34] T. Takemoto, H. Yamashita, T. Yazaki, N. Chunjo, Y. Lee, and Y. Matsuoka, “A 4 x 25-to-28Gb/s 4.9mW/Gb/s -9.7dBm high sensitivity optical receiver based on 65nm CMOS for board-to-board interconnects,” *in Proceedings of IEEE International Solid-State Circuits Conference*, pp. 118–120, 2013.

Abstract (In Korean)

광 변조기를 위한 온도 안정화 회로

상용 데이터 센터 및 모바일 장치에 대한 수요가 급격히 증가함에 따라 넓은 대역폭의 광 인터커넥트의 쓰임이 중장거리 통신에서부터 단거리 연결 통신으로 점차 확대되고 있다. 특히, Si 광 변조기들은 Si 회로들과 쉽게 호환 될 수 있다는 큰 이점을 가지고 있기 때문에 짧은 도달 거리의 상호 연결 어플리케이션에서 많은 관심을 받고 있다. 그러나 Si 광 변조기는 온도변화로부터 영향을 쉽게 받는다는 심각한 단점을 가지고 있다. 이에 대한 해결책으로, 본 논문은 광 변조기의 상용으로써의 실질적인 사용을 위해 필수적인 온도 안정화 회로의 시연에 초점을 맞춘다.

0.25-μm BiCMOS technology로 구현된 새로운 Mach-Zehnder 변조기 (MZM) 바이어스 제어 집적회로가 850-nm 대역의 상용 MZM의 3-Gb/s 데이터 변조와 함께 시연된다. 이 제어 회로는 MZM 출력의 광 변조 진폭 (OMA) 을 모니터링하고 최대 OMA를 갖는 최적의 MZM 바이어스 전압을 자동으로 검색하고 지속적으로 유지한다.

28-nm CMOS technology로 구현된 향상된 통합 MZM 바이어스 제어 집적회로가 1550-nm 상용 MZM의 25-Gb/s 데이터 변조와 함께

시연된다. 이 제어 회로는 MZM 출력의 OMA 및 평균 전력을 모니터링하고 두 단계로 동작하는 전략을 이용하여 향상된 전력 소비 및 초기 획득 시간을 보여준다.

0.25-μm BiCMOS technology로 구현된 새로운 Si micro-ring 변조기 (MRM) 파장 안정화 집적회로는 1550-nm Si MRM의 25-Gb/s 데이터 변조와 함께 시연된다. 이 회로는 Si MRM 출력 광 전력의 OMA를 높은 수준의 저전력으로 모니터링하고 최대 OMA를 갖는 최적의 히터 전압을 자동으로 검색하고 유지한다.

시연 된 모든 집적회로는 Si MZM 또는 Si MRM을 기반으로 한 Si 광 송신기와 한 Si 웨이퍼 위에서 monolithic 집적이 가능할 것으로 기대된다.

핵심 단어: Mach-Zehnder 변조기 (MZM), micro-ring 변조기 (MRM), 바이어스 제어 회로, 파장 안정화 회로, 광 변조 진폭 (OMA), 광 검출기, 집적회로 (IC), monolithic 집적, 광 인터커넥트, Si photonics, 제어 회로, 디지털 제어.

List of Publications

International Journal Papers

[1] **Min-Hyeong Kim**, Byung-Min Yu and Woo-Young Choi, "A Mach-Zehnder Modulator Bias Controller Based on OMA and Average Power Monitoring," in IEEE Photonics Technology Letters, vol. 29, no. 23, pp. 2043-2046, Dec.1, 1 2017.

[2] Byung-Min Yu, Myungjin Shin, **Min-Hyeong Kim**, Lars Zimmermann, and Woo-Young Choi, "Influence of dynamic power dissipation on Si MRM modulation characteristics," Chin. Opt. Lett. 15, 071301- (2017)

[3] Myungjin Shin, Yoojin Ban, Byung-Min Yu, **Min-Hyeong Kim**, Jinsoo Rhim, Lars Zimmermann, and Woo-Young Choi, “A Linear Equivalent Circuit Model for Depletion-Type Silicon Microring Modulators," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 1140-1145, March 2017.

[4] Sung-Geun Kim, Jinsoo Rhim, Dae-Hyun Kwon, **Min-Hyeong Kim**, and Woo-Young Choi, "A Low-Voltage PLL With a Supply-Noise Compensated Feedforward Ring VCO," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 6, pp. 548-552, June 2016.

International Conference Presentations

[1] **Min-Hyeong Kim**, Lars Zimmermann, Woo-Young Choi, "A Wavelength Stabilization Integrated Circuit for 25-Gb/s Si Micro-Ring Modulator," to be presented in Conference of Opto-Electronics and Communications Conference (OECC) (2018).

[2] **Min-Hyeong Kim**, Hyun-Yong Jung, Lars Zimmermann, Woo-Young Choi, "An integrated Mach-Zehnder modulator bias controller based on eye-amplitude monitoring," Proc. SPIE 9751, Smart Photonic and Optoelectronic Integrated Circuits XVIII, 97510X (3 March 2016).

[3] Sung-Geun Kim, Jinsoo Rhim, Dae-Hyun Kwon, **Min-Hyeong Kim**, and Woo-Young Choi, “A Low-Voltage PLL with a Current Mismatch Compensated Charge Pump,” in proceedings of IEEE International SoC Design Conference (ISOCC) (2015).

[4] Joung-Wook Moon, Kwang-Chun Choi, **Min-Hyeong Kim**, and Woo-Young Choi, “A Spur free 0.4-V 88-uW 200-MHz Phase-Locked Loop,” in proceedings of IEEE International SoC Design Conference (ISOCC) (2013).

Domestic Journal Papers

[1] 최광천, **김민형**, 최우영, "올-디지털 위상 고정 루프용 오프셋 및 데드존이 없고 해상도가 일정한 위상-디지털 변환기," 전자공학회 논문지 SD편, 제50권 제2호, 2013년 2월.

Domestic Conference Presentations

[1] 유병민, 신명진, **김민형**, Lars Zimmermann, 최우영, "Dynamic Power Dissipation에 의한 Si Micro-Ring Modulator 변조 특성 변화," 2016 Photonics Conference, Dec. 2016, 평창.

Patents

[1] **Min-Hyeong Kim**, and Woo-Young Choi, "APPARATUS AND METHOD OF CONTROLLING OPTICAL MODULATOR BIAS BASED ON EYE-AMPLITUDE MONITORING," *Korea Patent (Registered)*, Patent No. 10-1813784, Dec. 22, 2017.

[2] **Min-Hyeong Kim**, and Woo-Young Choi, "APPARATUS AND METHOD OF CONTROLLING OPTICAL MODULATOR BIAS BASED ON EYE-AMPLITUDE MONITORING," *USA Patent (Pending)*, Application No. 15/417,319, Jan. 1, 2017.