

Rad-Hard Adaptive Design Techniques for ASICs Used in Radiation Detecting System

Minuk Seung

The Graduate School
Yonsei University
Department of Electrical and Electronic Engineering

Rad-Hard Adaptive Design Techniques for ASICs Used in Radiation Detecting System

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Minuk Seung

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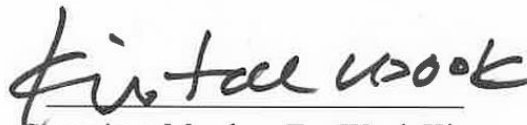
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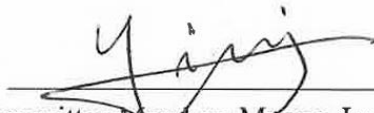
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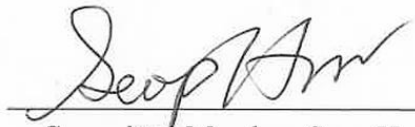
Vice-Supervisor: Inyong Kwon



Committee Member: Tae Wook Kim



Committee Member: Myung-Jae Lee



Committee Member: Seop Hur

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ABSTRACT

Rad-Hard Adaptive Design Techniques for ASICs Used in Radiation Detecting System

Minuk Seung

Dept. of Electrical and Electronic Engineering

The Graduate School, Yonsei University, Seoul, Korea

The rapid advancement of complementary metal–oxide–semiconductor technology has significantly increased the demand for Integrated Circuits (ICs) in radiation-sensitive applications, including space exploration, military systems, medical imaging, and nuclear power plants, particle physics. This surge has driven extensive research aimed at mitigating radiation-induced effects on ICs. This dissertation investigates advanced Radiation-Hardened-by-Design (RHBD) techniques through three primary studies. First, an RHBD preamplifier for general-purpose radiation detectors is examined using a binary weighted current source. The proposed preamplifier design integrates self-compensation mechanisms to alleviate total ionizing dose effects. This approach effectively identifies and compensates for radiation-induced degradation, thereby enhancing the reliability of charge-sensitive amplifiers for a wide range of radiation detectors.

Second, self-reset techniques for Micro-Pocket Fission Detectors preamplifiers are developed. To address the pile-up effect in MPFDs utilized for real-time neutron flux measurements within reactors, an Active Dead Time Control (ADTC) technique is proposed. This ADTC method dynamically adjusts the reset interval based on input signal rates, ensuring precise radiation measurements under both high and low radiation conditions. Experimental validation was successfully conducted at the Transient Reactor Test facility at Idaho National Laboratory.

Lastly, an RHBD Time-to-Digital Converter (TDC) is introduced. An adaptive TDC based on a two-step topology was designed and fabricated using a standard 180 nm CMOS process. A novel structure is proposed to mitigate radiation-induced skew error increases in the Pulse Train Time Amplifier (PTTA). Simulation results demonstrate that the proposed PTTA exhibits high linearity, with an improvement exceeding 43% compared to conventional PTTA designs.

Keywords: *Radiation-Hardened-by-Design (RHBD), Total Ionizing Dose (TID) effects, Single Event Effects (SEEs), Charge-Sensitive Amplifier (CSA), Micro-Pocket Fission Detector (MPFD), Active Dead Time Control (ADTC), Time-to-Digital Converter (TDC), CMOS technology, radiation mitigation.*

CHAPTER 1

Introduction

This chapter focuses on explaining the motivations behind the research on radiation-hardened adaptive design techniques for ASICs used in radiation detection systems. It also outlines the overall structure of the topics presented in this dissertation.

1.1 Motivation for the Dissertation

Since Röntgen's discovery of radiation in 1895, its applications across various industries have driven the development of radiation detectors and created a growing demand for radiation-hardened circuits within these systems [1]. Radiation detectors are critical instruments in numerous applications, including controlling the output of Nuclear Power Plants (NPPs) [2], monitoring the leakage of radioactive isotopes from reactors [3], and medical imaging techniques like Positron Emission Tomography (PET) for cancer diagnosis [4]. Additionally, these detectors are crucial for capturing non-visible light spectra in space, helping scientists explore the origins of the universe and understand astrophysical phenomena [5]. In fields such as particle physics, radiation detectors play a vital role in observing elementary particles like muons at accelerators like the Large Hadron Collider (LHC) at Conseil Européen pour la Recherche Nucléaire (CERN) [6]. Radiation detectors operate on the principle of detecting Electron-Ion Pairs (EIPs), or Electron-Hole Pairs (EHPs) generated through the interaction between radiation and detector materials,

such as Argon gas or Silicon semiconductor [7]. These charges are processed by analog-mixed systems. However, these interactions between radiation and materials are not limited to the target material alone. They can also occur within the semiconductor components of the detection system. When radiation effects occur on the transistor, they can lead to unintended changes in the internal electric fields of the semiconductor due to radiation-induced EHPs, potentially causing degradation in system performance [8]. Moreover, radiation-induced charge carriers can generate spurious signals or noise, which may be misinterpreted as valid events. These false signals degrade the accuracy and reliability of the measurements, leading to erroneous data interpretation. Therefore, it is crucial to develop radiation-hardened designs that can tolerate or mitigate radiation-induced effects, ensuring reliable and accurate operation in harsh environments.

In addition to the increasing importance of radiation hardening, the demand for Application-Specific Integrated Circuits (ASICs) in radiation detection systems is also growing rapidly. Traditionally, radiation detection systems have been widely designed using standard Nuclear Instrumentation Modules (NIM) and Computer Automated Measurement and Control (CAMAC) systems, which are typically housed in 19-inch relay racks [9]. However, with advancements in integrated circuit technology, many studies are now focused on achieving low power consumption, miniaturization, and high efficiency using ASICs, especially in the field of NPPs. As the development of various industrial sectors, such as the artificial intelligence field, has led to a sharp rise in electricity demand, there has been a global surge in the need for nuclear power generation. Moreover, the

development of Small Modular Reactors (SMRs) has necessitated research into new forms of instrumentation systems. Unlike conventional large-scale NPPs, SMRs are designed as compact modules. The modular design requires the miniaturization of the instrumentation system, and since the NIM system must be placed closer to the reactor than before, it will be exposed to extremely high radiation levels of approximately 0.93 Gy/h in normal operating condition and 2.91 kGy/h in accident condition [10]. For this reason, research on radiation-hardened ASICs for radiation detection systems is necessary to meet the reactor instrumentation system design criteria of each country.

Considering these challenges, this dissertation thoroughly analyzes the radiation effects that can occur in the various circuits of various radiation detectors, with a focus on total ionizing dose effects, which are predominantly generated in the NPPs circumstance. It explores the mechanisms by which radiation interacts with semiconductor devices and the consequent impact on circuit functionality. Furthermore, the study proposes circuit design techniques to mitigate these radiation-induced effects from a Radiation-Hardened-by-Design (RHBD) perspective. By integrating RHBD strategies into the design process, the research aims to enhance the tolerance of ASICs against radiation effects, thereby contributing to the advancement of reliable and efficient radiation measurement systems.

1.2 Organization of the Dissertation

This dissertation discusses the circuit blocks that utilize radiation-hardening techniques for radiation detectors. The ASIC-based circuit designs are explained, with a

brief overview of their applications provided in each chapter. The overall structure of the dissertation is as follows.

Chapter 2 explores the history of this research field, the background of radiation effects on transistors, and radiation-hardening techniques. Chapter 3 presents a Radiation-Hardened-by-Design (RHBD) preamplifier for general-purpose radiation detectors. It details the challenges encountered when the preamplifier is exposed to radiation, the RHBD techniques applied, and the measurement results from experiments conducted at a high-radiation facility. In Chapter 4, a preamplifier with a self-reset system is presented to address the pile-up phenomenon in Micro-Pocket Fission Detectors (MPFDs) designed for in-core neutron flux measurement, along with corresponding measurement results conducted at the Transient Reactor Testing (TREAT) facility in Idaho National Laboratory (INL). Chapter 5 discusses a RHBD time-to-digital converter for a silicon photomultiplier detection system used in PET. Finally, Chapter 6 provides a summary of the overall work presented in this dissertation, including additional commentary on the progression of the research, formalization of the contributions made to the science, and a future work on RHBD technology.

CHAPTER 2

Background

This chapter explains the history of the discovery of radiation, its effects on semiconductor devices, and the techniques used to minimize these effects

2.1 History

2.1.1 Brief History of Radiation Discovery

The discovery of radiation originated from experiments on the flow of current using vacuum tubes [11]. In 1895, Wilhelm Conrad Röntgen of Germany, while conducting an experiment with a Crookes tube, a device that generates electron beams, shielded with a black tube, discovered that radiation penetrated the shielding and caused fluorescence on a screen placed on the opposite side [12, 13]. He became the first to discover X-rays, marking the beginning of a remarkable advancement in nuclear physics. This discovery earned him the first Nobel Prize. In 1896, Antoine Henri Becquerel observed that potassium uranyl sulfate fluoresced after being exposed to strong sunlight, and he initially thought that the mineral absorbed sunlight and then emitted it [14]. While conducting experiments to prove this, he discovered that a photographic plate developed a dark image due to uranium that had been stored in a sealed container, leading him to believe that the uranium emitted some invisible rays, independent of sunlight. He published these findings in a paper submitted to Comptes Rendus [15]. Although he did not clearly identify the nature of these rays, he

recognized that they were different from Röntgen's X-rays and named them 'Becquerel rays' [16]. In 1897, Joseph John Thomson conducted experiments to prove the hypothesis that the rays emitted from a cathode ray tube were composed of individual corpuscles. During these experiments, he observed that the rays bent in an electric field [17]. Through his experiments, he concluded that these particles, later named electrons, were much smaller than typical atoms, and he was able to infer their mass-to-charge ratio [18 - 20]. Since all atoms are electrically neutral, he predicted the existence of positively charged particles within the atom and proposed the 'plum pudding model' of atomic theory [21]. In 1898, Becquerel's students, Marie Skłodowska Curie and Pierre Curie, introduced the term 'radioactivity' in their paper on polonium, a discovery that later earned them the Nobel Prize [22]. In 1899, Ernest Rutherford, a student of Thomson, conducted an experiment where uranium rays were passed through thin metal foils. During this experiment, he observed that the intensity of the radiation decreased inversely with the thickness of the aluminum foil and that the attenuation exhibited a pattern different from a typical exponential curve. He named the two exponential components alpha and beta, and he observed that the two particles showed different electrical properties when interacting with aluminum foil. These would later become known as alpha rays and beta rays [23, 24]. However, he was unable to distinguish another type of radiation with greater penetrating power than these two particle radiations. In 1903, this radiation was named gamma rays by Rutherford [25]. He later proved that the emission of radiation results from the decay of atoms, which earned him the Nobel Prize in 1908 [26]. In 1911, Rutherford discovered that when alpha particles

with a positive charge pass through a thin gold foil, most pass straight through, but some are reflected or scattered to the sides. From this, he proposed a model of the atom with a nucleus concentrated at the center and electrons surrounding it [27]. This was the first time the existence of the atomic nucleus was recognized. The existence of the proton was first discovered in 1886 by the German physicist Eugen Goldstein in an experiment where he observed canal rays, which exhibited properties opposite to those of cathode rays. However, he was unable to explain this phenomenon [28]. Although the existence of the proton was first discovered by Eugen Goldstein, it was Rutherford who provided the evidence. In 1919, Rutherford confirmed the existence of protons through his experiment on the collision of nitrogen and helium nuclei [29]. Neutrons, however, were discovered relatively late compared to other particles. In 1932, the possibility of neutrons was first proven by Rutherford's student, James Chadwick [30, 31].

These discoveries laid the foundation for the essential elements necessary to utilize radioactive elements. As a result, the field of radiation detection began to develop, and simultaneously, various research efforts involving radiation, such as radiation therapy, medical imaging, and nuclear power generation, commenced. Additionally, studies on the harmful effects of radiation on the human body also began. However, the impact of radiation on circuits had not yet become a significant consideration.

2.1.2 Brief History of Radiation Effects on the electronics

Research on the effects of radiation on semiconductor devices began in the mid-20th century. In the 1950s, gamma rays were used in studies to measure the diffusion length

and lifetime of PN junctions, but this research did not extend to understanding the effects of radiation on semiconductor devices [32]. In 1962, the National Aeronautics and Space Administration (NASA) launched Telstar 1 for satellite communication experiments. Alongside the communication system, equipment was included to analyze the radiation effects, which led to a comprehensive study of ionizing dose effects, specifically the cumulative effects known as Total Ionizing Dose (TID) effects [33].

During the Cold War in 1965, the threat of nuclear weapons increased, prompting research into the damage caused to MOS transistors due to radiation pulses emitted from nuclear weapons [34]. That same year, J.T. Wallmark and S.M. Marcus were the first to raise concerns about Single Event Effects (SEEs) [35]. In their paper, they predicted that cosmic rays could cause Single Event Upsets (SEU), limiting the minimum volume of semiconductors to 10 μm , though this was not based on observed data. Later, in 1975, D. Binder and colleagues reported that SEUs occurred in satellite flip-flops due to cosmic rays [36]. They noted that during 17 years of satellite operation, four anomalous events were observed [37]. In 1978, it was discovered that SEUs were caused by uranium and thorium used in the package materials and solder of RAM [38]. In 1979, a significant number of SEUs were reported in DRAM developed by Intel, which was later attributed to uranium contamination in the DRAM packaging, leading to increased alpha particle emissions [39]. The first paper reporting the effects of cosmic rays on electronic circuits in the atmosphere was written by F. Ziegler and W. A. Lanford [40]. This paper discussed methodologies for predicting the frequency of SEEs occurrences caused by cosmic rays in electronic circuit

components. Subsequently, reports emerged that SEEs were caused by protons and neutrons, and the first case of Single Event Latch-up (SEL) was reported [41 - 43]. While previous SEEs reports, such as SEUs, described soft errors, SELs were particularly significant as they resulted in permanent damage to transistors. By the 1980s, various types of SEEs were identified, leading to extensive research into IC hardening techniques.

Research on radiation effects is progressing steadily, driven by the continuous miniaturization of semiconductor devices, advancements in the space industry, and updates to nuclear power plant safety regulations. As semiconductor device feature sizes shrink to the nanometer scale, the sensitive volume susceptible to radiation decreases. However, this reduction in size leads to an increase in Multi-Bit Upsets (MBUs), which heightens overall sensitivity to SEEs. Consequently, these phenomena result in a growing number of errors, even in terrestrial environments [44, 45].

As the space industry continues to advance, the impact of radiation has become a significant concern for satellite operations. Studies estimate that approximately 20% of anomalies in space satellites are caused by radiation exposure [46]. In Low Earth Orbit (LEO), where the majority of satellites operate, the concentration of protons and electrons is particularly high, subjecting satellites to charged particles with energies ranging from 70 to 180 MeV [47, 48]. The radiation dose rate in LEO is approximately 2.74 Gy/h, which cumulatively degrades the satellite's electrical systems over time, potentially causing failures beyond their design margins [49]. In addition to Earth-orbiting satellites, various space agencies are conducting exploratory missions to study other celestial bodies in our

solar system. For example, NASA's upcoming Europa Clipper mission will explore the potential habitability of Europa, one of Jupiter's moons. During its four-year mission, the probe will encounter extreme radiation levels in Jupiter's magnetosphere, with exposure expected to exceed 41.7 Gy/h [50]. Additionally, researchers predict that particles with significantly higher energy and flux than those within Earth's magnetic field will be distributed around Jupiter [50, 51]. After the Fukushima nuclear disaster, regulatory guidelines for nuclear power plants were revised. The Institute of Electrical and Electronics Engineers (IEEE) updated its standards related to internal instrumentation and control systems. These documents outline the configuration, key requirements, and performance of accident monitoring systems, and mandate the survivability of monitoring systems designed to track nuclear fuel damage following an accident. Based on this, the U.S. Nuclear Regulatory Commission (NRC) revised its regulatory guide RG-1.97 to Rev.5, while the European International Electrotechnical Commission (IEC) updated IEC-63147 [52, 53]. Consequently, research is now being conducted to ensure the survivability of internal systems in high-radiation environments during severe accidents [54 - 56].

2.2 Radiation Effects on the MOSFET

There are two major effects that result from the interaction between Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) and radiation as shown in Fig. 2.1. The first is cumulative effects, which cause gradual performance degradation as the MOSFET is exposed to radiation over time, and the second is the impact caused by single events. TID effects are caused by electron-hole pairs (EHPs) generated in the dielectric

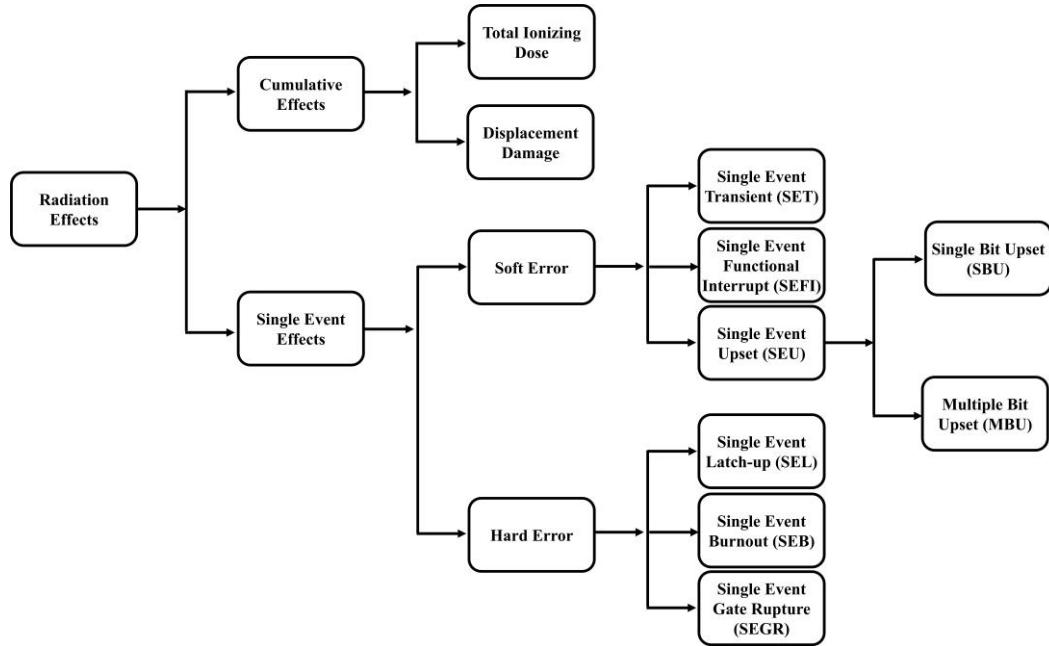


Fig. 2. 1. Categorization of Radiation effects on the MOSFET devices

layer of a MOSFET, leading to performance degradation such as threshold voltage shift, leakage current increase, and noise increase [54]. Displacement damage is non-ionizing process, causing lattice defects in the silicon structure of semiconductors, and leading to issues such as changes in carrier concentration, leakage current increase, noise increase, and carrier mobility decrease. SEEs are categorized into soft errors, which flip the logic of digital circuits or generate spurious signals, and hard errors, which cause transistor malfunction [45].

2.2.1 Total Ionizing Dose Effects

The fundamental principle of radiation and material interaction is the transfer of energy by radiation. When radiation penetrates through a material, it ionizes the atoms within it. In the case of MOSFETs, this process occurs in the dielectric layers, such as the gate oxide and shallow trench isolation (STI) in modern MOSFETs, where radiation creates EHPs along the radiation path. Typically, one EHP is generated for every 17 to 18 eV of absorbed energy [57]. Radiation-induced charges disrupt the internal electric field of the transistor, leading to performance degradation [58].

The degree of EHP recombination varies depending on the type of radiation. Previous research indicates that TID effects caused by photon radiation, such as X-rays or γ -rays, result in the highest EHP yield. This is because photon radiation, due to their high penetration ability, produces fewer EHPs within SiO_2 , which reduces the probability of recombination and thus increases TID effects. On the other hand, high-energy particles transfer a large amount of energy along their path, generating many EHPs, which leads to more recombination and makes TID effects less pronounced [59]. In addition to EHPs yield, charged particles lose energy rapidly due to their electrical interactions with matter. Thus, they cannot travel long distances and can be easily shielded by thin barriers. Therefore, although TID effects can occur in semiconductor devices due to all types of radiation, degradation is more severe with photon radiation.

2.2.1.1 Threshold Voltage Shift

The threshold voltage shift occurs due to radiation-induced charge in the gate oxide. Fig. 2.2 shows the mechanism of threshold voltage shift in an NMOS transistor. When EHPs are generated in the dielectric layer of the gate, some promptly recombine within the gate oxide. However, under the influence of the strong electric field within the transistor, the remaining electrons and holes are separated and driven toward opposite electrodes. In this process, electrons, which move faster than holes due to their higher mobility, can escape from the gate oxide layer [58]. The remaining holes now cause a threshold voltage shift. At this point, depending on the defects created by the holes, there are two mechanisms: oxide traps and interface traps.

The remaining holes migrate toward the Si/SiO₂ interface following the electric field, disturbing the local potential field of the SiO₂ lattice as they move. This disturbance increases the depth of traps, causing the holes to become trapped at those locations [54]. Subsequently, holes move through a process called hopping transport, which is a thermally assisted tunneling phenomenon of charge carriers between localized sites [57, 60]. holes can rearrange silicon-oxygen bonds within the oxide or interact with existing defects to form E' centers, which are dangling bonds. E' centers are defects in the oxide where a silicon atom is in a singly occupied state, possessing one unpaired electron, as illustrated in Fig. 2.3 [61]. When the E' center formed in this way is located within the oxide, it can trap holes and act as a permanent positive defect [62]. Holes trapped within the oxide are referred to as oxide traps, and these oxide-trapped holes can affect the threshold voltage (ΔV_{ot}). In an

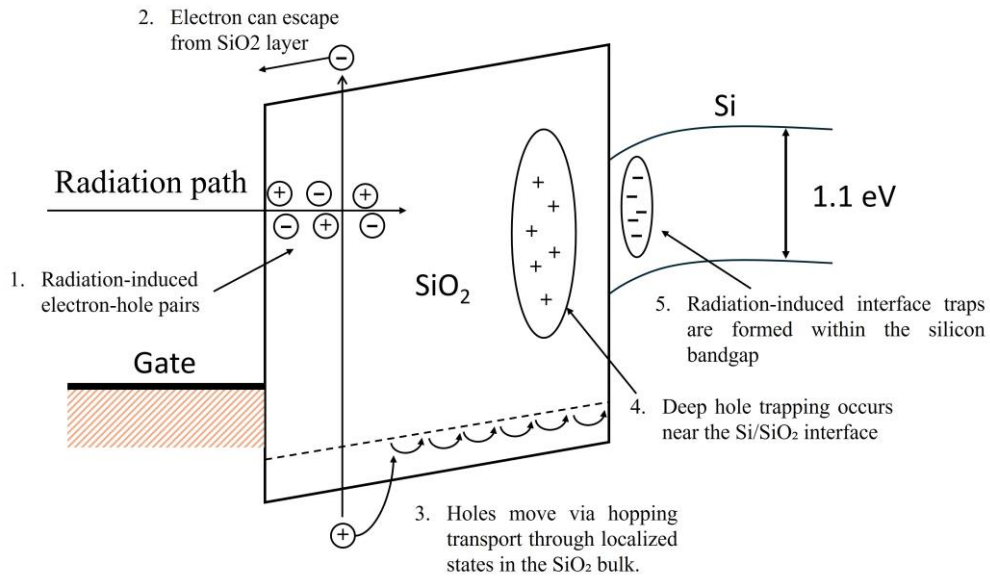


Fig. 2. 2. Energy band profile with NMOS and threshold voltage shift process

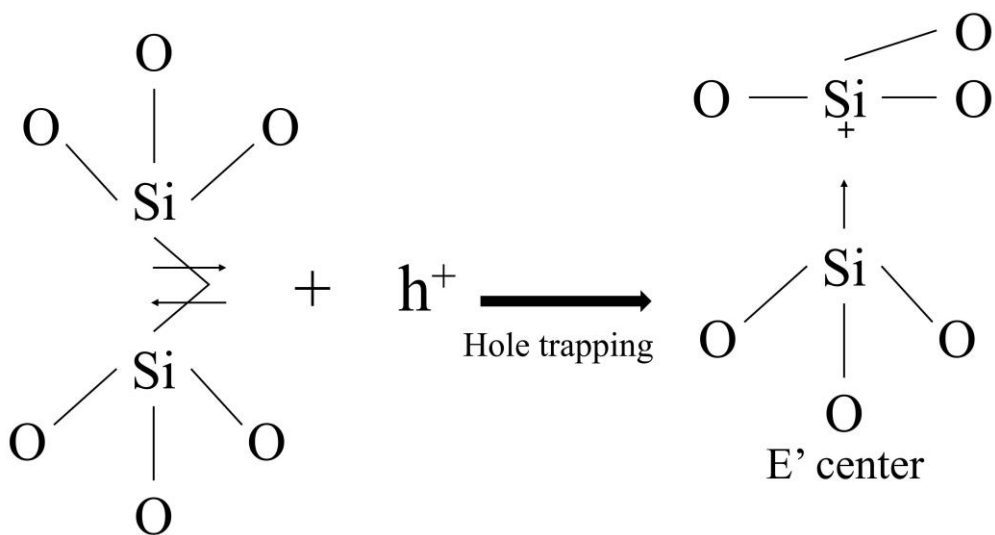


Fig. 2. 3. Process of E' center defect generation. In silicon-oxygen structure formed by oxygen defects, holes move through hopping, breaking Si-Si bonds and forming E' centers.

N-type MOSFET, this causes a negative shift in the threshold voltage, whereas in a P-type MOSFET, the threshold voltage shifts positively in terms of its absolute value [63]. The ΔV_{ot} can decrease following a logarithmic function during the annealing process and may vary depending on the fabrication process [59].

Another mechanism is called an interface trap (ΔV_{it}). There are two types of interface trap mechanisms. First, if an E' center is generated near the interface rather than inside the oxide, it captures electrons from the substrate through the tunneling effect, which is called the switching state [61]. The second cause is that, as holes move through hopping, hydrogen ions are generated, and these hydrogen ions bond with hydrogen-passivated dangling bonds near the interface. This occurs due to the interaction between proton and Si-H bonds near the Si/SiO₂ interface, which generates P_b centers as shown in Fig. 2.4 [64]. These interface traps do not anneal at room temperature but can be annealed at around 100°C [65]. Interface traps cause an increase in ΔV_{it} in both NMOS and PMOS devices, as called as rebound phenomenon.

Finally, the threshold voltage shift (ΔV_{th}) is represented as the sum of both traps. Mathematically, the threshold voltage shift caused by the oxide-trapped charges is defined as shown in (2.1).

$$\Delta V_{ot} = -\frac{1}{\epsilon_{ox}} \int_0^{x_{ox}} x \rho_{ox}(x) dx \quad (2.1)$$

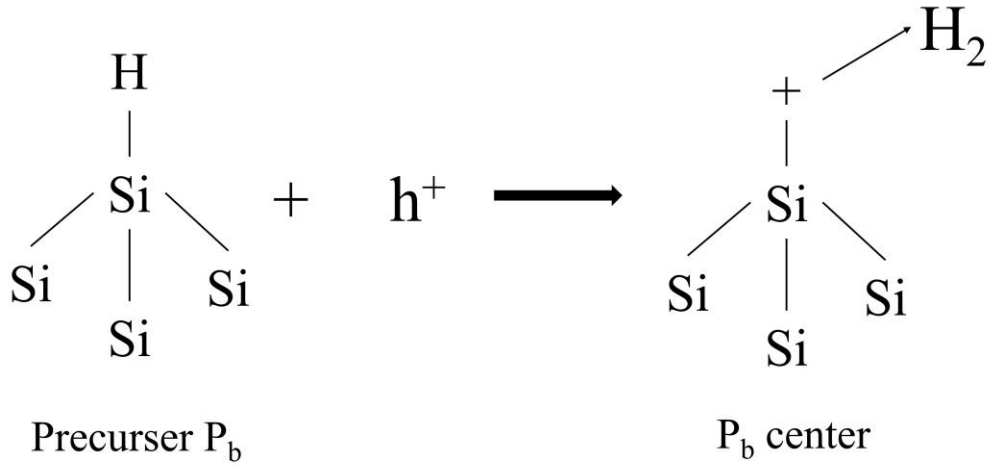


Fig. 2. 4. Process of Pb center defect generation. Due to interaction between hydrogen-passivated dangling bonds near the interface and proton (hydrogen), hydrogen molecules are formed, leaving the silicon in a dangling bond state.

where ϵ_{ox} is the dielectric constant of oxide, x_{ox} is the oxide thickness, ρ_{ox} is the volume charge density within the oxide, and x is the position within the oxide. Moreover, the threshold voltage shift induced by trapped holes at the SiO_2 -Si interface is given (2.2).

$$\Delta V_{it} = -\frac{Q_{int}}{C_{ox}} \quad (2.2)$$

where Q_{int} is the trapped charge at the SiO_2 -Si interface. Therefore, the total threshold voltage shift is calculated by summing (2.1) and (2.2):

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} = -\frac{1}{\epsilon_{ox}} \int_0^{x_{ox}} x \rho_{ox}(x) dx - \frac{Q_{int}}{C_{ox}}. \quad (2.3)$$

2.2.1.2 Leakage Current Increase

As modern semiconductor processes continue to scale down, the gate oxide thickness becomes thinner. It was discovered in the late 20th century that decreasing gate oxide thickness reduces the impact of threshold voltage shifts caused by radiation [66, 67]. Therefore, in the 180 nm process, which is the most widely used for general purposes today, a threshold voltage shift of only tens of millivolts typically occurs [68]. However, as processes shrink further, TID effects increase in the field oxide used for cell insulation, known as STI [69]. As shown in Fig. 2.5, STI surrounds the MOSFET. Radiation-induced charges become trapped in the SiO₂ of the STI, forming two leakage paths [61]. One leakage path forms from the parasitic transistor between the source and drain of the NMOS, while the other occurs between the drain and the N-well when a PMOS is adjacent [70]. The leakage current path caused by the parasitic transistor forms in the gate area outside the active region. Therefore, when designing circuits, using multipliers for common centroid design to reduce mismatch or employing fingers to minimize parasitic capacitance can create more leakage paths compared to using a single transistor, leading to an increase in leakage current [71].

The holes trapped in the STI exhibit a positive polarity, preventing the formation of a parasitic channel in PMOS, while predominantly forming in NMOS. The leakage current increase prevents the transistor from fully turning off, which poses a significant issue, especially in digital circuits and low-power devices. For instance, in memory cells such as

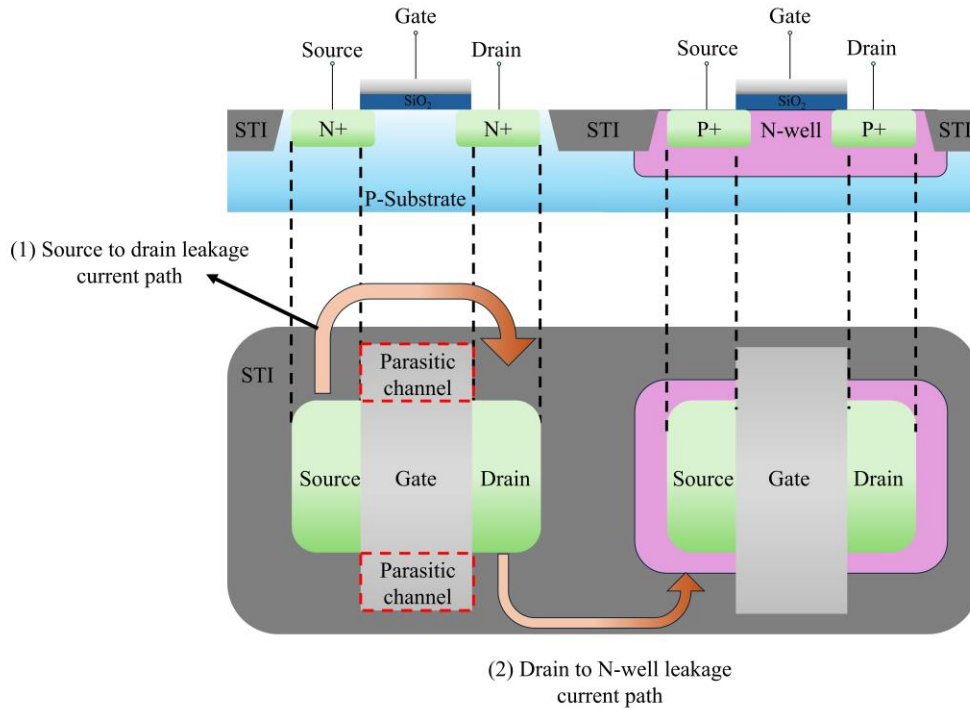


Fig. 2. 5. Process of forming a leakage current path: Two parasitic channels are formed due to the charge accumulated in the STI—one from source to drain and the other from drain to N-well

DRAM, an increase in leakage current necessitates a faster data refresh cycle, which can lead to reduced operation speed and increased power consumption.

2.2.1.3 Variation in semiconductor device characteristics

Due to TID effects, changes in threshold voltage shift and leakage current were previously observed. Moreover, key parameters of MOSFET transistors, such as transconductance (g_m) and output resistance (r_o), undergo changes due to TID effects. In analog circuits, g_m and r_o directly influence gain, bandwidth, and other performance metrics, making it crucial to maintain consistent g_m values for stable analog circuit design. Previous

research has shown that MOSFETs exposed to radiation experience a reduction in g_m , which can alter the characteristics of analog circuits, potentially compromising the overall system's reliability [64]. In contrast, due to the threshold voltage shift, r_o has been found to increase [69]. These changes lead to various impacts at the device level, significantly affecting the overall circuit system, which necessitates further analysis.

2.2.2 Singel Event Effects

As the feature size of modern CMOS technologies decreases, the increasing complexity of geometries, reduction in parasitic capacitance, and operation at higher frequencies have made circuits more susceptible to SEEs, which have emerged as a significant issue [71]. Unlike TID effects, which increase over time due to prolonged radiation exposure, SEEs are independent events that occur when a single radiation particle penetrates the sensitive area of a MOSFET device or a single cell in a system. When high-energy charged particles collide with semiconductor devices or ICs, they can cause digital logic states to flip, resulting in temporary malfunctions known as soft errors or cause permanent damage known as hard errors. SEEs are observed not only in space applications—environments rich in charged particles—but also in terrestrial memory devices due to atmospheric cosmic radiation, mainly neutrons. They can also be caused by alpha particles resulting from impurities in the solder of semiconductor packages [73]. SEEs occur when charges generated by radiation in the depletion region drift under the influence of a strong electric field. Thus, the most sensitive area is the reverse-biased PN

junction of semiconductor devices having strong electric field. In the next section, I will explain the two main mechanisms by which SEEs occur: charge deposition and charge collection [74].

2.2.2.1 Charge Deposition Mechanism

The interaction between radiation and devices can generally be quantified by the Linear Energy Transfer (LET) [7]. LET is a concept that describes the energy loss per unit length as a charged particle passes through a material as (2.4) [8].

$$\text{Linear Energy Transfer} = \frac{dE_d}{dx} [MeV \cdot cm^2/mg] \quad (2.4)$$

where x is the distance traveled, and E_d is the energy lost due to interactions with the target material [75, 76]. LET can be normalized by the density of the target material as (2.5).

$$\text{Linear Energy Transfer} = \frac{1}{\rho} \frac{dE_d}{dx} [MeV \cdot cm^2/mg] \quad (2.5)$$

where ρ is the density of the target material.

Direct ionization generally refers to the phenomenon where high-energy charged particles lose their energy within a semiconductor due to a high LET, directly generating a large number of electron-hole pairs (EHPs). The higher the LET, the more energy is

transferred to the material per unit distance, resulting in the generation of more EHPs. Typically, in silicon, a charged particle with $LET = 97 \text{ MeV-cm/mg}$ can generate a charge of 1 pC [77]. However, when the LET is low, especially for light particles like protons or neutrons, they may not generate enough EHPs to induce SEEs. Therefore, light charged particles mainly cause SEEs through indirect ionization. Indirect ionization occurs due to secondary radiation generated when high-energy protons or neutrons interact with the nuclei of semiconductor materials via nuclear reactions or various processes such as inelastic scattering [77].

2.2.2.2 Charge Collection Mechanisms

Charges generated by the charge deposition mechanism are collected through drift, diffusion, and parasitic bipolar transistor (BJT) operation, leading to the occurrence of SEEs [74]. Based on this mechanism, SEEs can be classified into soft errors and hard errors.

Soft errors, such as Single Event Transients (SETs) and SEUs, are the most well-known types. These occur when charges generated by charge deposition primarily move through the source and drain regions of a MOSFET. The most vulnerable area of the CMOS to SETs and SEUs is the reverse-biased PN junction [77]. Typically, when radiation passes through the depletion region of a reverse-biased PN junction, it generates charges. Due to the high electric field applied to form the depletion region, charge collection through drift processes occurs rapidly from these radiation-induced charges. As a result, a high transient current momentarily occurs at junction [78]. Additionally, SEEs sensitivity increases due

to the funneling effect. This phenomenon causes the electric field around the PN junction to become abnormally shaped like a funnel due to radiation, as shown in Fig. 2.6. Consequently, even if EHPs are generated far from the depletion region, they are drawn into it by the distorted electric field, leading to increased charge collection [79]. This can result in a significant source-drain current, causing the transistor to behave as if it is in the on-state or generating spurious signals, which can disrupt analog or digital circuit systems.

Hard errors include Single Event Latch-up (SEL), Single Event Burnout (SEB), and Single Event Gate Rupture (SEGR). SEL typically occurs in bulk CMOS technologies when N-type and P-type devices are fabricated on the same substrate [78, 79]. Although SEB and SEGR are also observed in bulk CMOS, they are primarily found in power transistors [82, 83].

SEL occurs due to parasitic BJT formed within CMOS circuits, as shown in Fig. 2.7 (a). When CMOS is fabricated on a common silicon wafer, the formation of the N-well naturally leads to the creation of two parasitic BJTs [81]. SEL is triggered when charge deposition causes charges to accumulate in the well region, turning on these parasitic BJTs. Fig. 2.7 (b) illustrates the classical latch-up model. For example, when BJT A is turned on, its collector current feeds into the base of BJT B, and the amplified current from BJT B causes a voltage drop across resistor R1, increasing the collector current of BJT A. This positive feedback leads to an overcurrent, which can ultimately damage the CMOS device [84]. This mechanism is called the regenerative latch-up mechanism [80]. The phenomenon worsens as temperature increases due to higher well resistance and forward voltage drop.

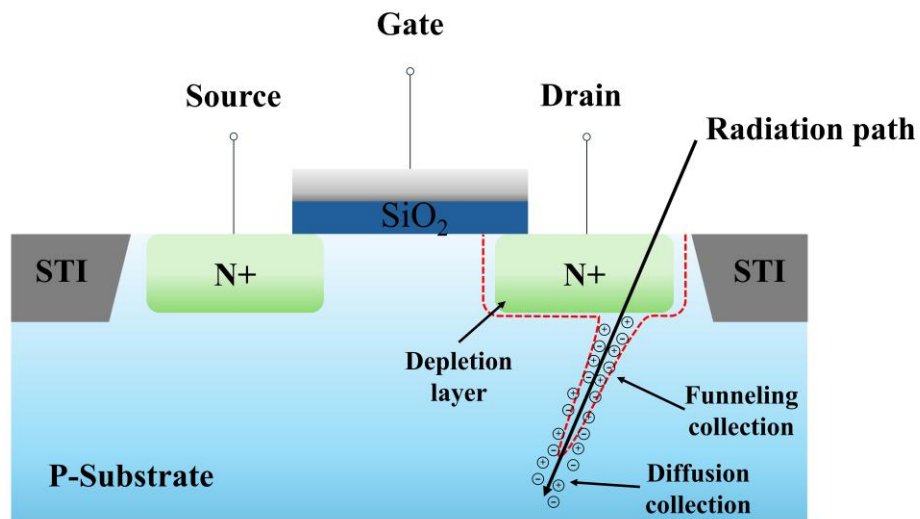


Fig. 2. 6. Process of charge collection due to the funneling effect: When radiation enters the depletion region of a transistor, electron-hole pairs are generated, and the depletion region expands due to the funneling effect. As a result, charges generated far away diffuse toward the drain.

To prevent SEL, techniques such as Silicon on Sapphire (SOS) and Silicon on Insulator (SOI), which eliminate PNPN parasitic BJTs, can be employed [85, 86].

In SEB, parasitic BJTs are also the cause [87]. Fig. 2.8 shows a graph to explain the breakdown mechanism in power MOSFETs. When the drain voltage of a power MOSFET exceeds a certain point, it reaches the normal avalanche breakdown point. Beyond this point, the drain current increases sharply with even a small increase in drain voltage. If this condition persists, the drain current causes a voltage drop in the P-body region, turning on the parasitic BJT. The drain current begins to flow not only through the source but also through the P-body region. As a result, although more drain current flows, but the drain voltage decreases. When the device reaches an uncontrolled current state, known as second breakdown, failure occurs [88]. This phenomenon can be triggered by radiation. If a high-

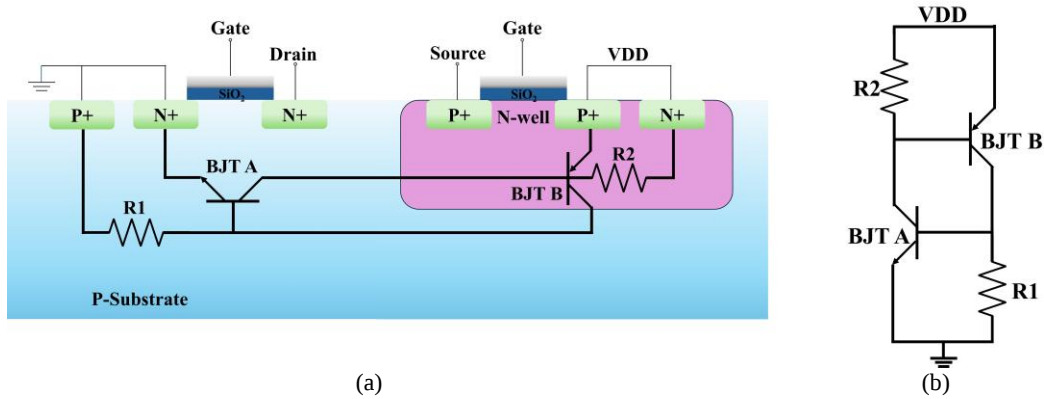


Fig. 2. 7. CMOS inverter cross section. (b) simplified parasitic latch-up model. Two parasitic bipolar junction transistors are naturally formed due to the N-well. If radiation-induced charge generates enough charge to trigger the BJT, positive feedback leads to an overcurrent, causing SEL.

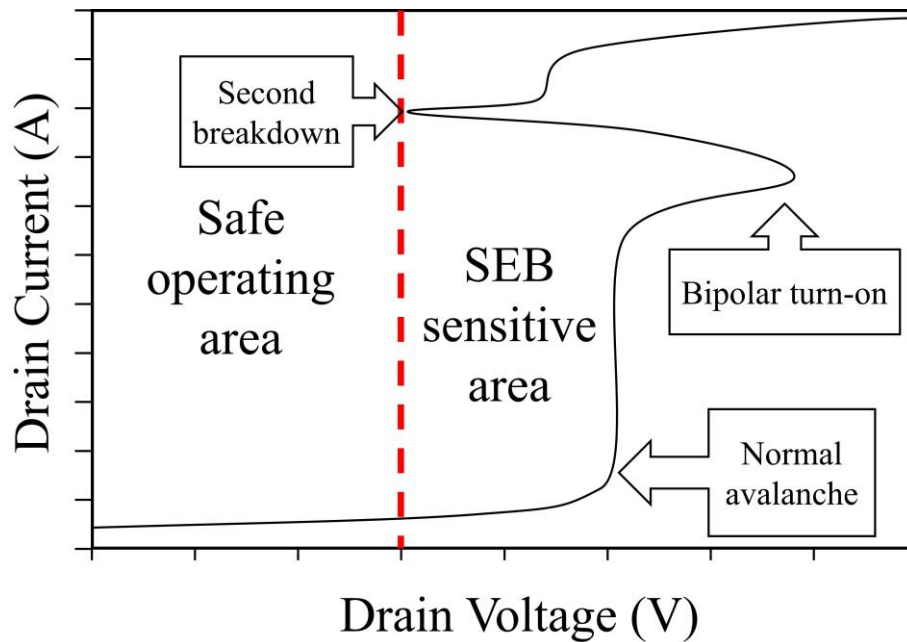


Fig. 2. 8. Breakdown mechanism of power transistor. When the voltage exceeds certain threshold and reaches normal avalanche, even a slight increase in voltage causes the current to increase excessively, turning on parasitic bipolar junction transistor. As the current flows through the p-body and source, it reaches an uncontrolled current state, leading to device failure.

energy charged particle passes through the sensitive area and generates a large number of EHPs, the parasitic BJT may turn on, resulting in a secondary breakdown [89].

SEGR is a phenomenon where the gate oxide layer becomes permanently damaged, occurring when heavy ions strike the neck region of a power transistor, as shown in Fig. 2.9 [90]. EHPs generated along the radiation path are separated by the applied voltages: electrons flow toward the drain, while holes flow toward the gate. This charge collection leads to a plasma sheath phenomenon, causing permanent damage [91]. Due to the slow mobility of holes, they diffuse into the p-body at a slower rate than they drift toward the interface, resulting in a hole pile-up. The accumulation of holes creates a positive charge pool at the interface, momentarily increasing the strength of the electric field. When the electric field strength exceeds the critical value of the gate oxide, oxide breakdown occurs, shorting the gate and substrate [92]. Although there are other SEEs, their impact on this study is minimal; therefore, they will not be discussed in this work.

2.3 Radiation Hardening Techniques

After it was discovered that radiation affects electronic circuit systems, many ideas and techniques were proposed to mitigate these effects. These approaches can be broadly classified into two categories: Radiation-Hardened-by-Process (RHBP), which involves modifying and altering semiconductor fabrication processes, and RHBD, which minimizes radiation effects at the circuit design level [93], as shown in Fig. 2.10. In the next section, each technique will be briefly discussed.

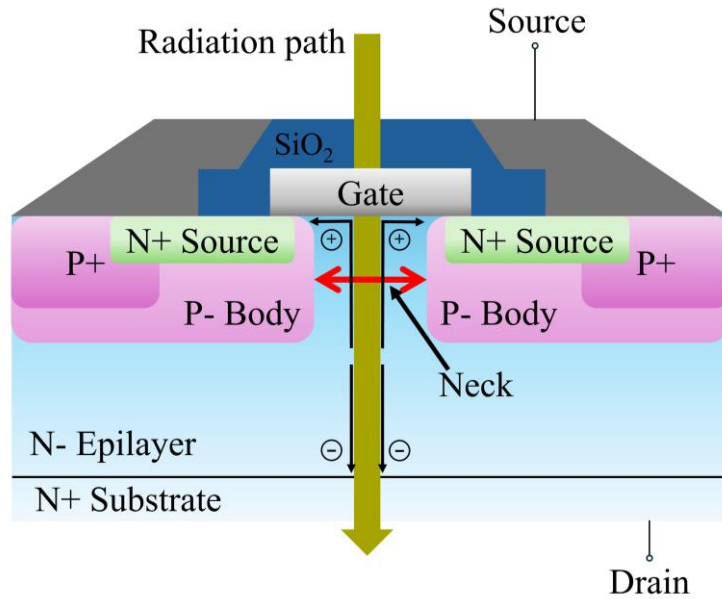


Fig. 2. 9. Mechanism of single event gate rupture. When radiation strikes neck of power transistor, electron-hole pairs diffuse along each terminal. Due to difference in mobility, a plasma sheath phenomenon occurs, leading to the rupture of the gate oxide.

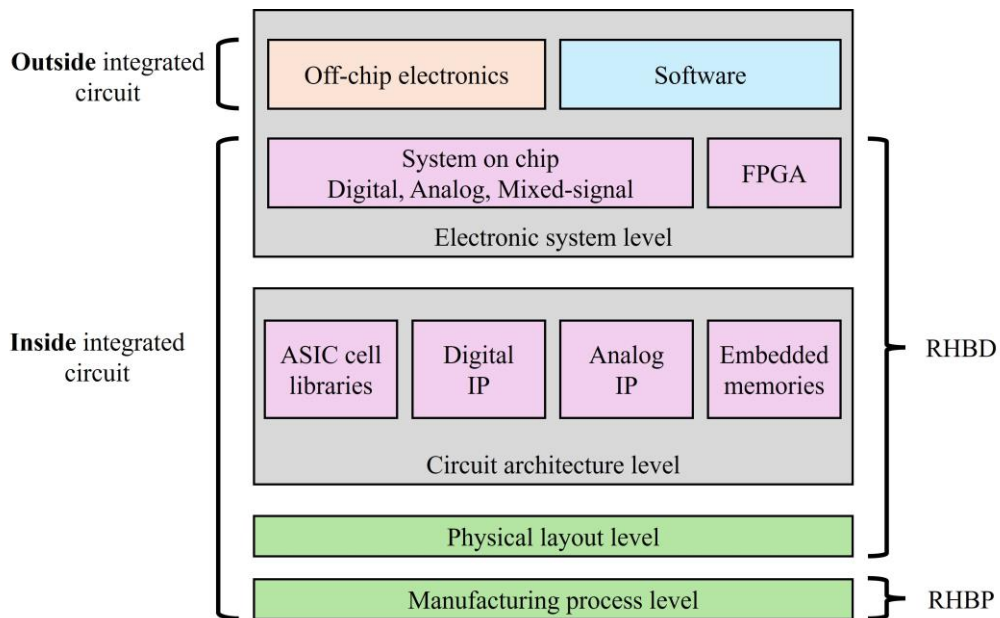


Fig. 2. 10. Classification of radiation hardening techniques.

2.3.1 Radiation-Hardened-by-Process

RHBP techniques minimize the effects of radiation on semiconductor devices by modifying cell structures and materials or using other processes instead of standard CMOS processes.

One of the most well-known layout techniques to mitigate TID effects is the Enclosed Layout Transistor (ELT) structure, which eliminates edges to minimize leakage current increases caused by STI charge traps [63]. Fig. 2.11 shows a MOSFET with an ELT structure. In this design, gate oxide surrounds the active area instead of STI, reducing hole traps compared to the relatively thicker field oxide. This decrease in leakage current path formation helps alleviate leakage current issues [94]. In 1995, IBM demonstrated that the first-generation SiGe Heterojunction Bipolar Transistor (HBT) had high radiation resistance, making it a promising candidate for use in space and military applications. The radiation tolerance of SiGe HBT was found to be due not so much to the presence of Ge, but rather to structural design features such as a thin, heavily doped base, shallow trench isolation (STI), and a thin emitter-base oxide layer [95]. However, HBTs are sensitive to the effects of SEE and have limited applicability due to scaling limitations [96].

To minimize the impact of SEEs, structures like SOI and SOS are used. SOI technology has been extensively researched in the aerospace and military fields and has now become a commercial technique. In SOI, active devices are implemented on a dielectric layer called the buried oxide (BOX). This configuration reduces the cross-section that interacts with charged particles and inherently removes the PNPN structure responsible for SEL, resulting

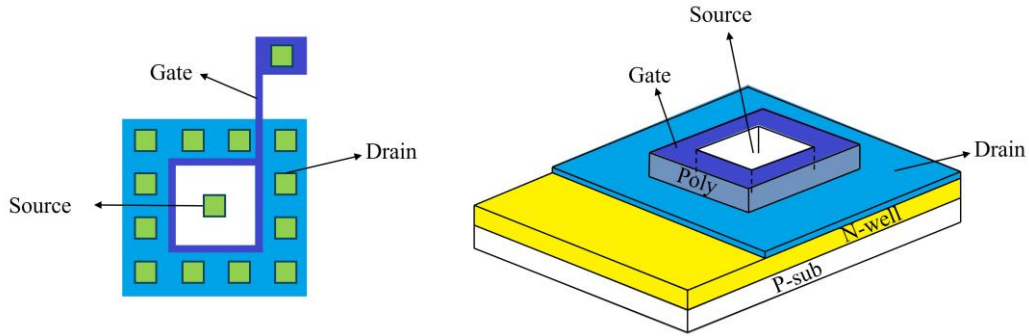


Fig. 2. 11. ELT structure. (a) Bird-eye view and (b) cross-sectional view. Thanks to the edgeless structure, the leakage current path is suppressed.

in better radiation resistance than bulk silicon transistors [97]. However, the BOX layer can be susceptible to TID effects. Trapped holes within the BOX can form channels, leading to increased leakage current in the transistor. Additionally, SOI devices are still vulnerable to Single Event Snapback (SESB) due to remained parasitic BJT [98].

SOS transistors are fabricated by forming an epitaxial silicon film on sapphire (Al_2O_3). Sapphire possesses properties such as a high dielectric constant, low dielectric loss tangent, excellent thermal conductivity, low substrate capacitance, and full dielectric isolation due to its high resistivity [99]. Since SOS lacks bulk silicon, the number of radiation-induced charges is significantly reduced. Therefore, compared to bulk silicon transistors, SOS devices have very low SEEs sensitivity and do not experience SEL [100]. However, hole trapping occurring in the backside sapphire can form parasitic inversion leakage paths. Moreover, due to high production costs and the development of alternative technologies,

commercial foundries rarely offer this process, limiting its use to certain military and aerospace applications.

Although these various devices and techniques help achieve radiation hardening through RHBP, ELT structures still have some drawbacks. ELT structures remain susceptible to SEEs issues and are not supported by process design kits (PDKs) from commercial foundries. Consequently, circuits designed using ELT face design challenges, such as difficulties in conducting electrical simulations and increased area consumption. Therefore, it is necessary to study RHBD alongside RHBP to improve radiation-hardened performance.

2.3.2 Radiation-Hardened-by-Design

Recently, significant research has focused on radiation mitigation techniques utilizing the RHBD approach. RHBD compensates for and mitigates the radiation effects at the circuit design level rather than at the transistor or process level. One fundamental RHBD method involves increasing the width and length ratio (W/L) of semiconductor devices during the chip design phase. By enlarging the gate size, the effects of radiation are relatively reduced due to increased parasitic capacitance and current levels [101]. In addition to adjusting the gate size, employing guard-ring techniques can prevent SEL and reduce leakage current between devices [102].

From a circuit design perspective, various techniques can be applied to mitigate TID effects. One method replaces conventional diodes with Dynamic-Threshold MOS

Transistors (DTMOSTs). DTMOSTs are primarily used in low-power circuit systems, and utilizing a PMOS DTMOST provides inherent radiation resistance because the field oxide near the PN junction is smaller compared to that of conventional diodes [63]. Y. Cao et al. proposed the Dynamic Base Leakage Compensation (DBLC) technique to minimize radiation effects on the BJT in a bandgap reference (BGR) circuit. Since the collector current of the BJT is scarcely affected even when the total dose rate increases, radiation hardness was enhanced by maintaining a constant base current [103]. In [104], radiation hardness was improved through the chopper stabilization technique. To minimize radiation effects caused by mismatch and offset in BGR circuits using DTMOSTs, the design incorporated chopper-based switching. In [105], a method to enhance the radiation hardness of BGRs using a first-order cancellation technique that offsets radiation effects was proposed. S. T. Vibbert et al. introduced a technique to detect increases in leakage current in real time. When leakage current rises in a parallel transistor array, a photocurrent-controlled oscillator generates a sawtooth voltage signal with a frequency proportional to the leakage current, allowing for continuous monitoring [106].

SEEs mitigation techniques are even more diverse. One proposed method involves designing at the layout level so that multiple MOSFETs share a weak node through charge sharing, allowing EHPs generated in a specific cell to be dispersed across multiple cells [107-109]. Additionally, various topologies have been proposed to mitigate SEEs in SRAMs. Notably, the 12T Dual Interlocked Storage Cell (DICE) [110], the 10T Quatro [111], and the improved 12T We-Quatro [112] structures exhibit high resistance to SEEs

due to their dual interlocking configurations. In [113], the radiation tolerance of a 6T SRAM structure was improved by covering a single cell with two metal layers, increasing parasitic capacitance and raising the critical value at which radiation-induced charge causes SEEs. Studies have also reported using inverse-mode SiGe HBT, which electrically swap the emitter and collector terminals of a BJT, to mitigate Analog Single Event Transients (ASET) in communication circuit systems [114-118]. These works employed a cascode design combining a standard forward-mode SiGe HBT and an inverse-mode SiGe HBT sharing a buried subcollector to reduce radiation effects. In [119], an RHBD Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) was presented, featuring three error detection techniques: over- and under-flow detection, extra-bit detection, and parity bit error detection. Utilizing these techniques, SEEs can be detected, thereby achieving radiation tolerance.

CHAPTER 3

Rad-Hard Preamplifier for Versatile Radiation Detector

In this chapter, I will discuss the design of a Radiation-Hardened-by-Design (RHBD) preamplifier using a 180 nm standard process to mitigate Total Ionizing Dose (TID) effects for general-purpose radiation detectors, such as those used in high-radiation environments like nuclear power plants or space exploration probes. Additionally, the irradiation results of gamma-ray are discussed, conducted at the Korea Atomic Energy Research Institute (KAERI) gamma-ray facility up to 230 kGy (SiO₂).

3.1 Background

The preamplifier, which converts an incoming charge-based signal into a voltage, is a fundamental element in radiation detection systems. Since radiation cannot be directly measured, the charge generated through its interaction with the target material of detectors must be recorded [120]. Charges can be generated from various interactions within materials. For example, a common type of radiation detector, the ionization chamber, measures the charge produced when radiation ionizes gases, such as Argon or Helium, and then uses a strong electric field generated by a high voltage to collect these charges at the electrodes. Other detectors involve employing a scintillator to convert radiation into detectable photons that are then transformed into electrons, or detecting the Electron-Ion Pairs (EIPs) produced by fission fragments during nuclear fission. Regardless of the

method, the fundamental task is to transform radiation into charge. This charge is eventually converted into a form that can be processed by analog-mixed systems. At this stage, the weak and noisy signal generated by the detector is transformed into a voltage signal by a preamplifier, which also amplifies weak signal and reduces noise, thereby enhancing the Signal-to-Noise Ratio (SNR) [121]. Thus, the preamplifier plays a critical role in analog-mixed systems.

Fig. 3.1 illustrates the front-end system of a radiation detector, where a Charge-Sensitive Amplifier (CSA) serves as the preamplifier [122]. The CSA is commonly chosen due to its high linearity and sensitivity. It is constructed from an operational amplifier (OP-AMP), feedback resistor (R_F), and feedback capacitor (C_F) with C_{det} representing the detector capacitance. By using the feedback capacitor to collect radiation-induced charge, the CSA provides a fixed gain. Its output is directly proportional to the input charge (Q_{in}), and can be described by the following equation:

$$V_{out} = -A_V \frac{Q_{in}}{C_{det} + (A_V + 1)C_F}. \quad (3.1)$$

Where, A_V is the open loop gain. If the detector capacitance is less than $(A_V + 1)C_F$, the output voltage can be expressed as follows [123]:

$$V_{out} = -\frac{Q_{in}}{C_F}. \quad (3.2)$$

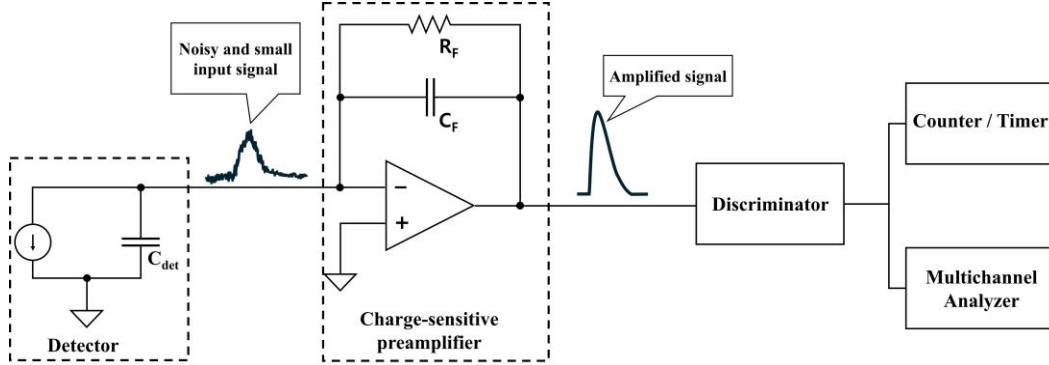


Fig. 3. 1. Block diagram of a radiation detector. Charge-sensitive amplifier receive input signal from detector and amplifies the signal. The amplified signal is then transmitted to shaping amplifier and discriminator for signal processing.

However, in radiation environments, CSAs are prone to performance degradation caused by TID effects.

3.2 Rad-Hard Charge-Sensitive Amplifier

The preamplifier is designed with a two-stage differential OP-AMP that is well known for its low noise, low power consumption, high speed, and appropriate gain. Fig. 3.2 illustrates the fundamental configuration of the two-stage OP-AMP. Long-term exposure of an OP-AMP to radiation can induce TID effects such as threshold voltage shift, leakage current increase, and noise increase, which in turn cause a reduction in both gain and SNR. The critical parameters of the OP-AMP, such as open loop gain, Gain Bandwidth Product (GBWP), transconductance (g_m), and output resistance (r_o) are as follows:

$$A_V = -g_{m3}g_{m6}(r_1//r_3)(r_6//r_7), \quad (3.3)$$

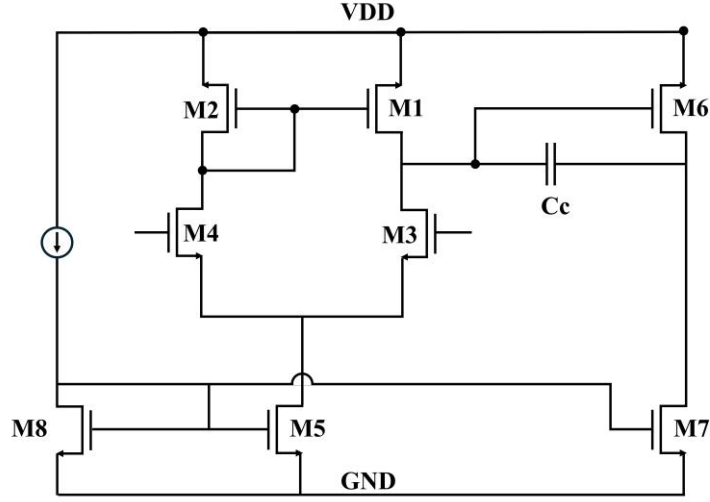


Fig. 3. 2. Schematic of conventional two-stage differential operation amplifier.

$$GBWP = \frac{g_{m3}}{C_c}, \quad (3.4)$$

$$g_m = \frac{2I_D}{V_{OV}}, \quad (3.5)$$

$$r_o = \frac{1}{\lambda I_D}. \quad (3.6)$$

Where, C_c is the Miller capacitance, I_D is the drain current, and V_{OV} refers to the overdrive voltage, which is the difference between the gate-source voltage and the MOSFET's threshold voltage. Additionally, λ is the channel length modulation coefficient. As a result of TID effects, these properties are variated, leading to performance degradation. Typically, TID effects lead to a rise in the threshold voltage of PMOS, resulting in reduced gain. For NMOS, the impact varies depending on whether the oxide trap or interface trap

has a more dominant effect. Additionally, an increase in leakage current paths may cause a slight increase in current.

3.2.1 Design of RHBD Amplifier

The radiation-hardening strategy involves compensating for changes in the preamplifier's current level to minimize TID effects, achieved through the use of a 6-bit Binary Weighted Current Source (BWCS). The proposed preamplifier, shown in Fig. 3.3, consists of two primary components: the CSA part and a replica part. The CSA part consists of a 6-bit BWCS OP-AMP with feedback network, enabling it to operate as the CSA for radiation detectors. The replica part is used to compensate for TID effects by detecting output change induced by TID effects. It is composed of an OP-AMP with the same as the CSA part, two continuous comparators that detect radiation-induced changes, and a BWCS control circuit. The two-stage OP-AMP in the preamplifier consists of a bias circuit, transmission gates for switches, and a 6-bit BWCS, as illustrated in Fig. 3.4. The BWCS control circuit includes a 6-bit up-and-down counter, counter control logic, and a ring oscillator to trigger the counter, as shown in Fig. 3.5. The BWCS can supply current to the OP-AMP in increments from $1I$ up to $64I$, based on the control circuit's output signal.

3.2.2 Operating Principle of the RHBD CSA

Within the replica part, the OP-AMP acts as a sensor, detecting current fluctuations that result from TID effects. Under normal situation, when both inputs of the OP-AMP are

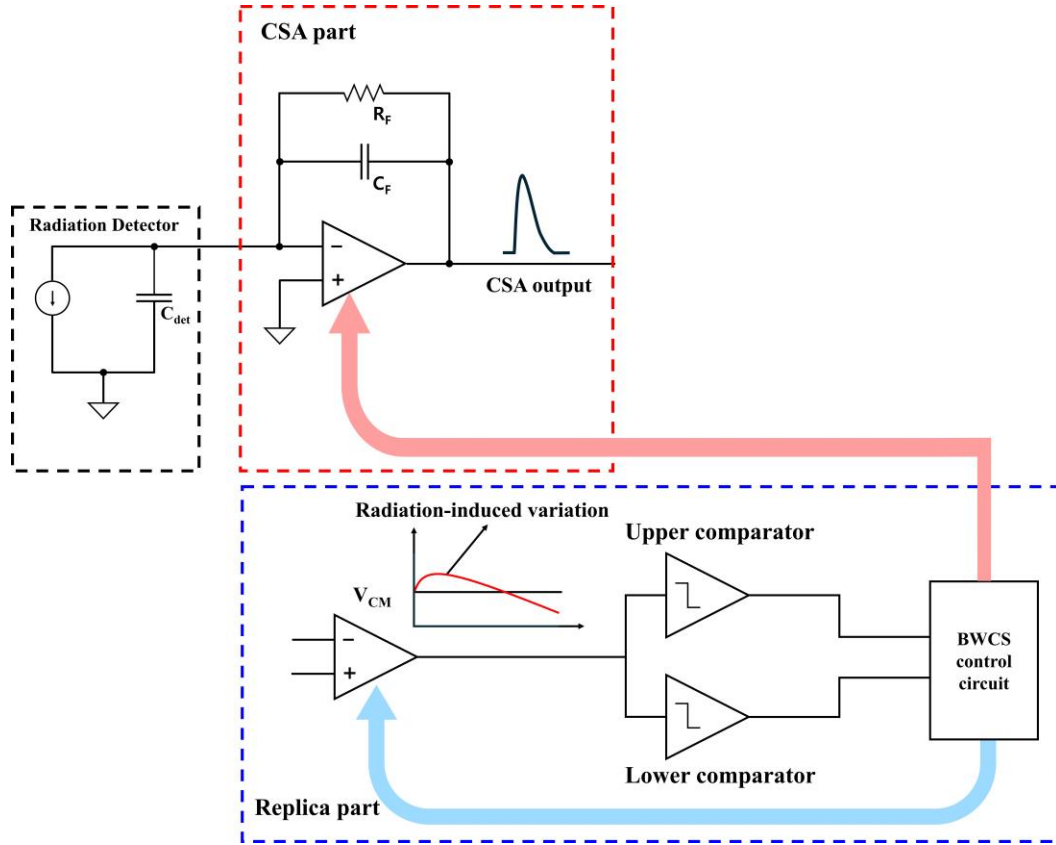


Fig. 3. 3. Block diagram of proposed charge-sensitive amplifier. The proposed preamplifier is composed of two the CSA part and replica part.

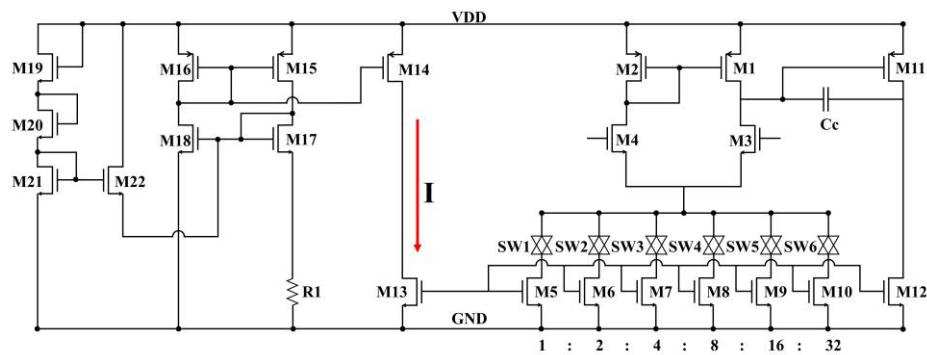


Fig. 3. 4. Structure of operational amplifier used for proposed preamplifier. The amplifier has a 6-bit binary weighted current source to compensate for TID effects.

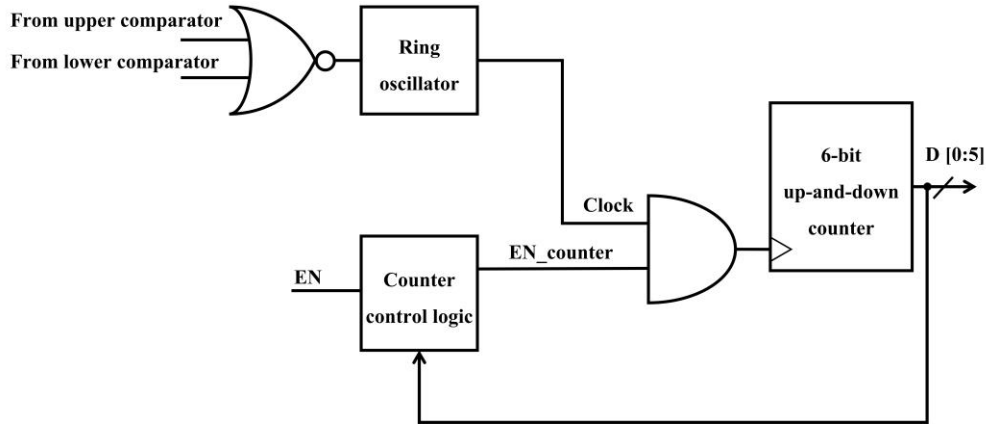


Fig. 3. 5. Configuration of the BWCS control circuit. The circuit consists of a ring oscillator, counter control logic, and a 6-bit up-and-down counter.

maintained at a common-mode voltage, the output should remain at the common-mode level. However, when the circuit is exposed by radiation, the resulting current fluctuations shift the operating point of OP-AMP.

To detect these fluctuations, two comparators are employed, each set with reference voltages that are close to the common-mode level but differ by approximately ± 200 mV to account for noise variations. When the common-mode voltage shifts above or below these reference thresholds, the comparators output a HIGH signal. The counter can be operated as either an up-counter or a down-counter depending on which comparator is triggered. The resulting digital code from the counter then controls the BWCS switches, allowing the current supplied to both OP-AMPs to be adjusted to compensate for TID-induced changes. For instance, if radiation exposure shifts the operating point of replica OP-AMP upward, the upper comparator outputs the HIGH signal, causing the 6-bit up-and-down counter to

function as a down counter, which reduces the current of the two OP-AMPs. Conversely, if the output decreases, the lower comparator signals the counter to increase the current.

The ring oscillator generates a 1.9 μ s pulse which used as the clock signal of the counter. If the clock is faster than the propagation delay of BWCS system, the counter might count multiple cycles before the BWCS code is updated, leading to potential errors. Additionally, because the counter operates cyclically, failure to stop at critical points would result in an infinite loop, cycling between 000000 and 111111. For example, if the counter reaches 111111 and the lower comparator signals a decrease, the counter resets to 000000, reducing the preamplifier's current from 64 I to 1 I, which could indicate a system malfunction. To prevent this, when the counter reaches certain limits, such as saturation states like 000001 or 111111, it must be halted. To prevent this, an arbiter circuit controls the operation of counter at saturation points using logic gates.

To verify the performance degradation of the CSA in radiation environments before fabrication, simulation validation was conducted. As mentioned in Chapter 2, TID effects primarily result in threshold voltage shift and increased leakage current. In modern semiconductor processes, threshold voltage shift has been reduced due to process scaling. However, the influence of leakage current increase has intensified. Thus, for the verification simulation, a simple leakage current model was designed, as shown in Fig. 3.6. An ideal current source was connected between the source and drain of the NMOS to simulate a specific level of leakage current flow. Radiation effects can vary depending on factors such as voltage bias level, dose rate, and doping concentration. Therefore, exact

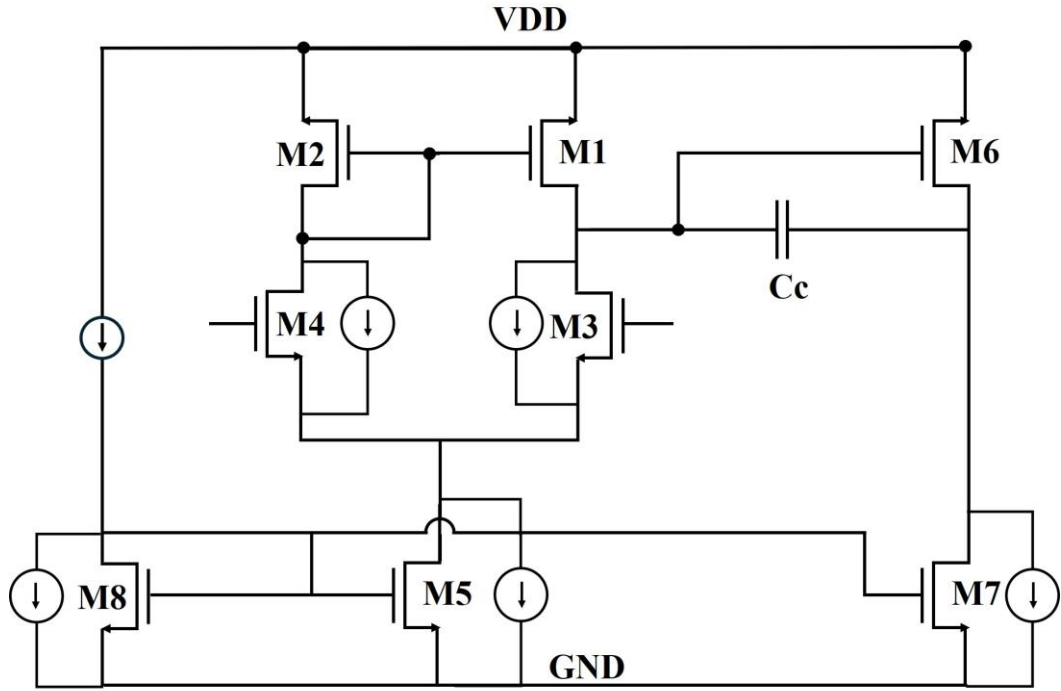


Fig. 3. 6. Simplified TID model for two-stage OPAMP. Ideal current source is connected between source and drain of the NMOS, creating leakage current path.

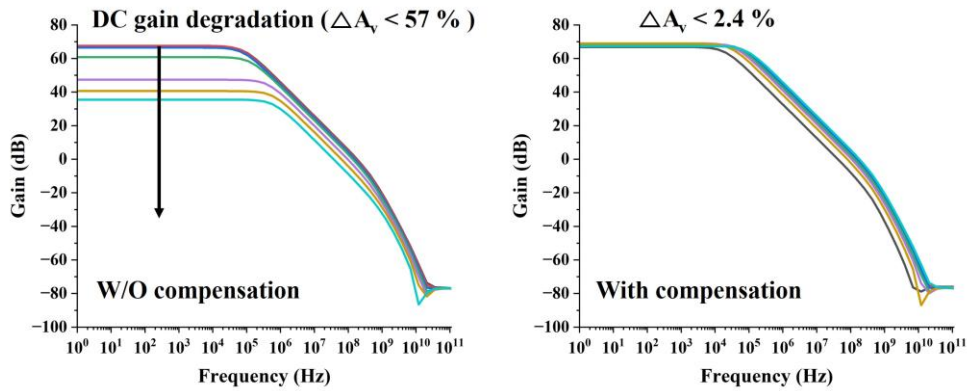


Fig. 3. 7. Simulation results of simple TID model for two-stage OPAMP. In OPAMP without compensation, increase in leakage current results in significant gain reduction up to 57 % (a). In contrast, OPAMP with compensation shows very small error of less than 2.4 % (b).

simulation validation is not feasible; however, this model allows for an approximate evaluation of the impact of increased leakage current.

The simulation results are shown in Fig. 3.7. Fig. 3.7 (a) illustrates the effect of increased leakage current on an uncompensated OPAMP. The current was swept up to a total of 60 μA in increments of 10 μA , and it was observed that the gain decreased by more than 57% depending on the leakage current level. In contrast, for the circuit with the compensation technique applied, a change of approximately 2.4% was observed, demonstrating very stable operation according to the simulation results as depicted in Fig 3.7 (b).

3.3 Chip Implementation Details

The proposed preamplifier was implemented using a 180 nm standard complementary metal-oxide-semiconductor (CMOS) technology. A photograph of the fabricated chip is provided in Fig. 3.8, with the active area of the circuit occupying 0.1208 mm². Table 3.1 details the electrical specifications of the OP-AMP used in the proposed preamplifier. The proposed circuit operates at 1.8 V, with an open loop gain of 66 dB, a 3 dB bandwidth of 112.5 kHz, and a GBWP of 217.15 MHz. The phase margin is 55°. To reduce the impact of process variation, external Surface Mount Device (SMD) type resistors and capacitors were used for the feedback components.

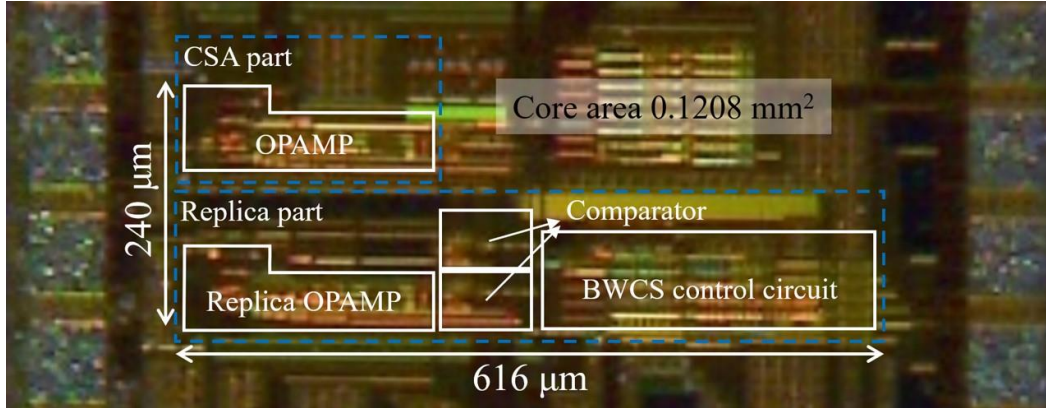


Fig. 3. 8. Photograph of the proposed preamplifier circuit in 180 nm standard MOS technology.

Table 3. 1

ELECTRICAL PARAMETERS OF THE TWO-STAGE OPAMP.

Parameters (unit)	Value
Supply voltage (V)	1.8
Miller capacitance (pF)	1
Open loop gain (dB)	66
3dB BW (kHz)	112.5
GBWP (MHz)	217.15
Phase margin (°)	55

3.4 Measurement Results

A verification test of the radiation-hardened preamplifier was conducted at the KAERI using a cobalt-60 gamma-ray source. During testing, the Design Under Test (DUT) board was exposed to radiation up to 230 kGy (SiO_2) at a rate of 10.46 kGy (SiO_2)/h. Fig. 3.9 illustrates the test setup. As shown in Fig. 3.9 (a), the radiation source initially remained submerged in water and then was raised to the surface once testing began. The DUT board

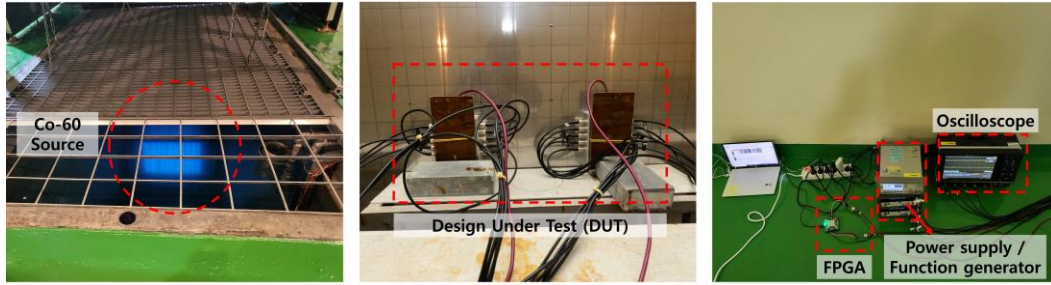


Fig. 3. 9. (a) Cobalt-60 gamma ray source for irradiation test. (b) DUT board and (c) electrical equipment for experiment.

was placed in front of the source as depicted in Fig. 3.9 (b). To shield the measurement equipment from radiation, it was positioned behind a 30 cm-thick concrete wall, as shown in Fig. 3.9 (c). Long cables, approximately 15 m in length, were used to connect the DUT to the equipment. Two types of data were collected for analysis: analog outputs from the CSA were recorded using an oscilloscope, while digital outputs from the BWCS control circuit were captured by an FPGA. Data logging took place every 20 seconds.

Fig. 3.10 shows the changes in the output of the counter for compensating TID effects during the irradiation test. In the experiment, the digital code value had a maximum of 42 and a minimum of 29, whereas it had an initial of 39 before the irradiation. The result indicates that the system current level tended to decrease as a result of radiation exposure. This behavior might have been related to the leakage current increase. When the leakage current increased, the system current level also increased. Consequently, the BWCS reduced the system current. The small and regional variation in the code could have occurred as a result of a quantization error caused by the current changing in increments of

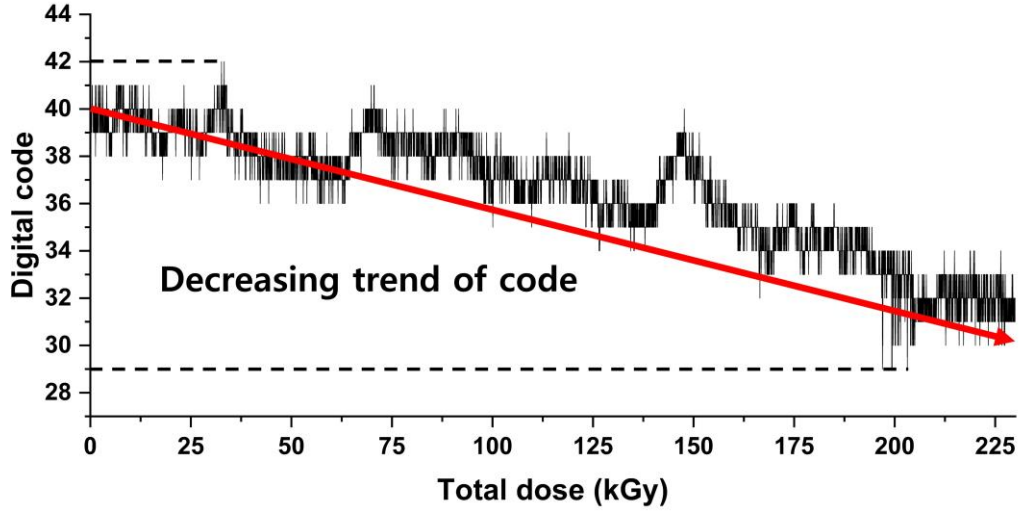


Fig. 3. 10. Trend curve for output of the BWCS control circuit in relation to the total dose. As the total dose increases, the graph exhibits a downward trend. An initial value of 39, a maximum value of 42, and a minimum value of 29 were recorded.

1 I. In other words, because the system required a value between two specific codes, a fluctuation error occurred.

Fig. 3.11 (a) displays the output of the preamplifier at 50 kGy (SiO_2) intervals during the irradiation test. Variations in the amplitude of the output could occur as a result of changes in the current. As previously discussed, the open loop gain was determined by the transconductance and output resistance of the OP-AMP. Radiation effects could cause changes in the current level of the system, resulting in fluctuations in the system's gain and GBWP. Fig. 3.11 (b) depicts the error rate of the normalized maximum amplitude of the proposed preamplifier. A maximum error of 2.39% was observed at 100 kGy (SiO_2), with the digital code reaching 38. Fig. 3.12 (a) shows the rise time variation during the gamma-ray exposure test. It was calculated at 20% and 80% of the peak voltages, avoiding the

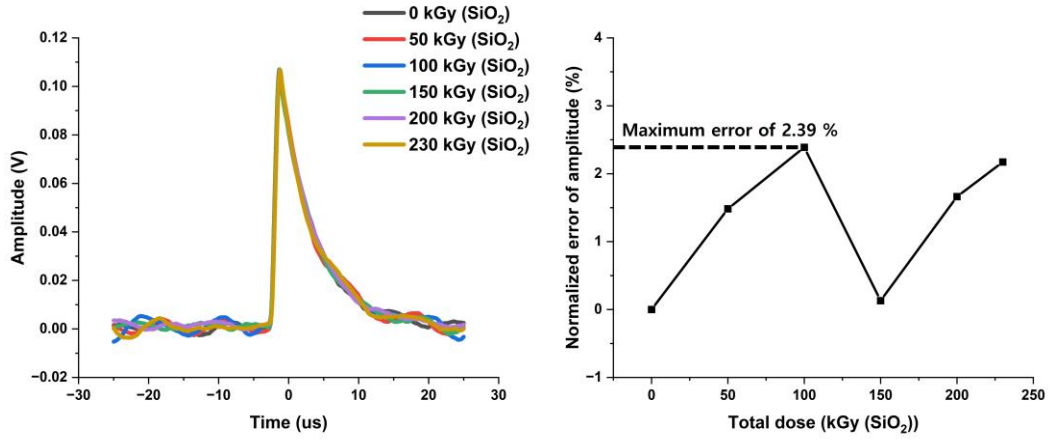


Fig. 3. 11. During irradiation test with gamma rays up to 230 kGy (SiO₂): (a) recorded output of CSA and (b) error rate of normalized amplitude of the preamplifier obtained as a maximum error rate of 2.39%.

impact of the noise. The rise time was measured as 0.577 μ s before the irradiation test. A maximum rise time of 0.588 μ s was observed, along with an error of 1.96% at a total dose of 100 kGy (SiO₂). The rise time variation was also related to the system current level because the slew rate was obtained using [124]:

$$Slew\ rate = \frac{C_c}{I_D}. \quad (3.7)$$

The SNR exhibited a range of 49.64 dB–60.31 dB, depending on the total radiation dose, as illustrated in Fig. 12 (b). The SNR is a crucial parameter for a preamplifier because it quantifies the noise level relative to the readout system signal. It provides a measure of the ability to distinguish the desired signal from the unwanted noise originating from the detectors. The gate-referred noise voltage spectrum is represented by:

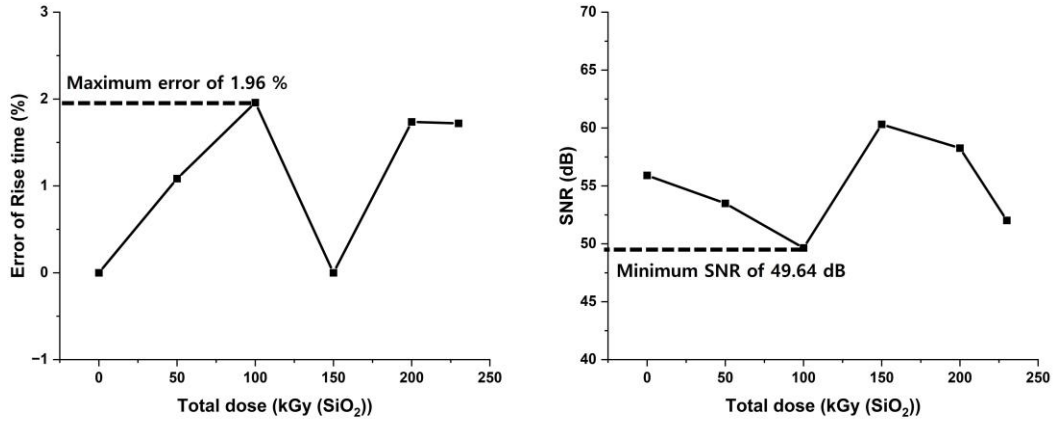


Fig. 3. 12. During irradiation test with gamma rays up to 230 kGy (SiO₂): (a) maximum rise time of 0.588 μ s and (b) SNR in range of 49.64 dB to 60.31 dB.

$$S_e^2(f) = 4kT \frac{\alpha}{g_m} + \frac{K_f}{C_{ox}WL} \frac{1}{f}. \quad (3.8)$$

The first term is the thermal noise term. k is the Boltzmann constant, T is the absolute temperature, and α is the channel's thermal noise coefficient. Thus, the degradation of the transconductance results in an increase in noise within the circuit [125]. The second term is the flicker noise term ($1/f$) [68]. K_f is intrinsic process parameter, C_{ox} is the gate capacitance. As previous studies, $1/f$ noise is also affected by radiation, resulting variation of K_f [63]. As the test result, the maximum error rate of the SNR, in terms of its absolute value, was measured at 11.2% when subjected to a total radiation dose of 100 kGy (SiO₂).

Table 3.2 shows comparison result in terms of amplitude variation, SNR variation, maximum dose, and the specifications of the OPAMP used for CSA. In [56], an idea was

Table 3. 2

COMPARISON RESULTS OF RHBD OPAMPS

	Technology		Dose rate (kGy/h)	Total dose (kGy)	Amplitude variation (%)	SNR variation (dB)
This work	180 nm Si CMOS		10.46	230	2.39	-5.74
[54]	180 nm BiCMOS		8	50	0.9 / 8.1	5 / 4.7
[55]	180 nm CMOS		1	10	N/A	11.7
[120]	250 nm SiGe BiCMOS		0.0025	10	18	N/A
[121]	180 nm BiCMOS	Basic	1.04	20	34.3	11.6
		Double width			16.7	3.12
	180 nm Si CMOS	Basic			2.85	2.4
		Double width			2.32	0.07
	130 nm SiGe CMOS	Basic			3.6	0.314
		Double width			2.23	0.202

applied to compensate for the current by measuring the variation in the duration of the input signal. Two samples were tested, showing amplitude variations of 0.9% and 8.1%, respectively, with SNR variations measured at 5 dB and 4.7 dB. A BiCMOS process, which is relatively radiation-resistant, was used, and a lower total dose was irradiated; however, the effects of radiation were still significant. In [127], the study discusses how noise characteristics change in a conventional two-stage OP-AMP due to radiation exposure. The experimental results showed that SNR decreased by 11.7 dB. In [126], radiation testing on a low-noise amplifier was reported, with a decrease in amplitude of 18% observed at 10 kGy. In Ref. [124], they conducted an analysis of the radiation effects on the CSA configured with a conventional two-stage OPAMP. They considered three types of processes: SiGe CMOS, Si CMOS, and Si BiCMOS technologies, while also varying

MOSFET channel size and system current levels. The term “basic” refers to the conventional two-stage OPAMP structure for the CSA, while “double width” indicates an OPAMP configuration with transistors having twice the width of the basic circuit. The “tail current” signifies the current level flowing through the OPAMP. As comparison results, the proposed CSA is observed that there is less variation in the amplitude at higher dose. Although the proposed circuit experienced greater SNR degradation due to radiation, its inherent circuit SNR is significantly higher, resulting in even the lowest SNR of proposed CSA being greater compared to the highest SNR of [124]. Comparing these results, it demonstrates that the circuit proposed in this paper is effective in mitigating performance degradation caused by TID effects in radiation environments.

CHAPTER 4

Preamplifier with Self-Reset System for Neutron Detector

4.1 Background

In the nuclear power industry, active research and development of in-core neutron measurement systems is being conducted to ensure safe and cost-effective operation of nuclear power plants. Nuclear power has been a fundamental source of global energy production since the 1950s [128]. The rapid advancement of Artificial Intelligence (AI) technologies has necessitated the increased use of large-scale servers for AI computations, significantly elevating global energy consumption. Although many countries have implemented eco-friendly energy solutions to mitigate global warming, these measures have not entirely kept pace with rising energy demands. Consequently, nuclear power is being reconsidered by some countries and companies, such as Microsoft, and Amazon, as part of broader carbon-free energy strategies, sparking renewed interest in nuclear energy [129, 130]. As the demand for nuclear power plants (NPPs) increases, concerns regarding safety and cost-effectiveness have emerged, spurring extensive research aimed at enhancing safety standards and economic efficiency. This has also led to active research and development of instrumentation used within nuclear power plants. Commercial NPPs employ a variety of instruments to ensure operational reliability and safety, including radiation detectors, thermometers, and pressure gauges [131]. Among these instruments, understanding the power distribution profile is essential for the economical and reliable

operation of NPPs. This profile is typically assessed using neutron detectors, such as ion chambers positioned outside the reactor, where the detector response is expected to be proportional to neutron flux. However, ex-core detectors are often inefficient, as they can only measure leakage neutrons from the reactor core [132]. Previous studies have reported errors of up to 15% when using ex-core ion chambers to measure reactor power distribution [133]. Therefore, the use of in-core detectors is required for accurately monitoring the neutron flux profile within the reactor.

In addition to in-core detectors, significant size reduction is necessary for small modular reactors (SMRs), which have been recently developed to generate less than 300 MWe [134]. SMRs offer several advantages, including cost efficiency, flexibility, reliability, and reduced risk of sabotage [135]. However, monitoring the neutron flux profile of SMRs using ex-core detectors remains challenging due to the limited number of neutrons leaking from the core, a result of enhanced propagation resistance, one of the key advantages of SMRs [136]. Traditional in-core fission chambers may be unsuitable for SMR applications due to their limited operational lifespan and susceptibility to significant flux perturbations [137].

4.1.1 Micro-Pocket Fission Detectors

Micro-pocket fission detectors (MPFDs) were developed and verified over several years by Kansas State University and Idaho National Laboratory (INL) [138] for real-time measurement of neutron flux inside reactors. Previous studies have demonstrated that these

compact detectors offer numerous advantages for in-core applications, including their small size, ability to operate in high neutron flux environments, uniform charge deposition, gamma-ray discrimination, radiation hardness, and minimal neutron perturbations [139-142]. A prototype of the MPFDs is shown in Fig. 4.1 [143, 144]. The detector design incorporates multiple nodes coated with varying fissile materials, each with a thickness of less than 1 μm , to interact with both fast and thermal neutrons in the reactor [138, 139]. When a neutron interacts with the neutron-reactive material, fission occurs, producing fission fragments. These fragments can initiate ionization reactions within the gas-filled cavity, and the resulting Electron-Ion pairs (EIPs) flow along the electrodes. To accurately measure the generated charge and monitor power distribution with MPFDs, a dedicated readout system must be designed to interface with the detectors.

4.1.2 Electronics System of MPFDs

Previous studies primarily used discrete components to configure the MPFD readout system [143]. However, commercial-off-the-shelf (COTS) electronics present several limitations, including large size, high power consumption, and complex designs unsuitable for miniaturized applications. Consequently, the MPFDs readout system must be redesigned using application-specific integrated circuits (ASICs) to overcome these challenges.

MPFDs generate output in the form of charge, making a Charge-Sensitive Amplifier (CSA) a suitable preamplifier for converting current to voltage [145]. However, in high-

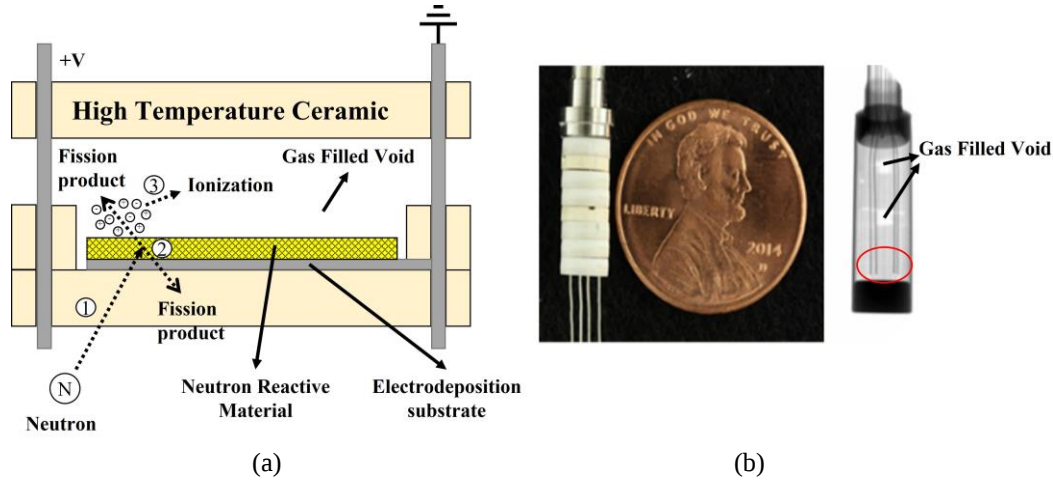


Fig. 4. 1. Prototype MPFD structure is shown with active fission area. (a) Neutron reactive material as a fissile layer generates fission fragments of which energy is deposited by interacting with Argon gas [145], [146]. (b) X-ray image of the single MPFD [145].

radiation environments, such as those found in-core, general-purpose CSAs are prone to a pile-up phenomenon [146]. Since the CSA output is directly proportional to the input charge, if the MPFD response time is significantly faster than the CSA's discharge period in high-power nuclear reactors, charge may accumulate continuously in the CSA's feedback capacitor. This accumulation can lead to preamplifier saturation at its maximum output, thereby preventing accurate signal acquisition.

This work seeks to develop the first MPFDs readout system using ASICs for the measurement of high neutron flux in an in-core setting. The sensor interface incorporates a preamplifier with a self-reset technique, data loggers for processing, and a remote monitoring algorithm to facilitate real-time measurement.

4.2 Self-Reset Preamplifier Design

4.2.1 Design Overview

The overall MPFDs readout system is illustrated in Fig. 4.2. This system is installed inside the reactor of the Transient REActor Test (TREAT) facility at INL for verification testing. To minimize radiation exposure, the readout system is housed in a separate data acquisition system (DAS) room, located away from the reactor. The MPFD signal is transmitted via an RG58 cable to the preamplifier. Two laptops are stationed in the DAS room: one is used for controlling the data loggers, while the other processes the acquired data and displays the neutron flux on the user interface. These laptops communicate using the RS-422 wireless communication protocol, with a consistent time interval of 10 ms. The second laptop is connected to a third laptop located in the control room via a LAN cable, enabling real-time monitoring of the reactor transient from a distance of 1 km.

4.2.2 Readout System Operation Principle

The readout system operates in two detection modes: single event and integration. The single event mode can measure the analog data at the output of the preamplifier. On the other hand, the integration mode is utilized in a high radiation environment, such as the inside of the reactor, and merged with the current mode and count mode detectors [147, 148]. The distinction between the current mode and the integration mode lies in their measurement approach. In the current mode, the average current is measured, whereas in the integration mode, this is not the case. Instead, the proposed readout system maintains a

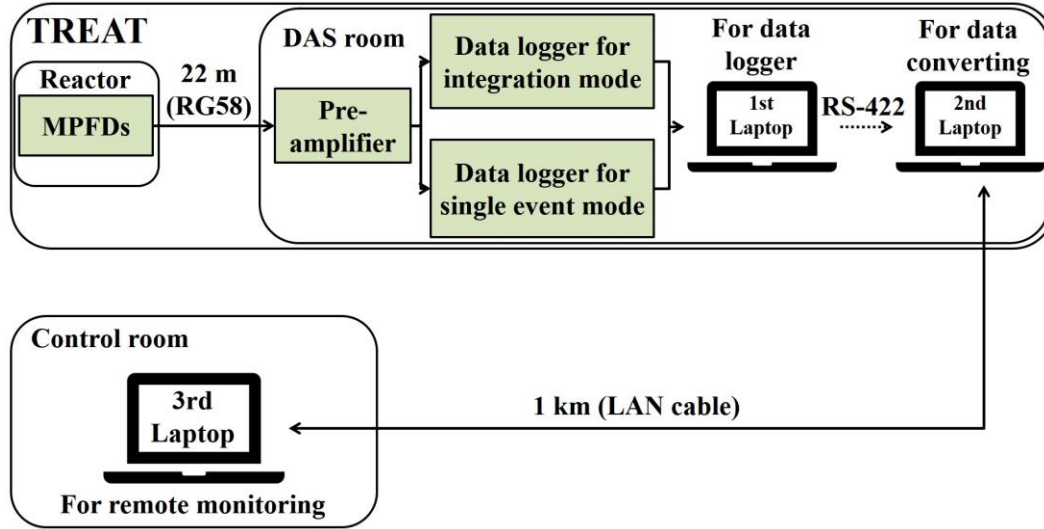


Fig. 4. 2. Overall MPFD readout system block diagram. The system consists of the preamplifier, two data loggers for integration mode and single event mode operations, and the laptop for monitoring measured data in real time.

constant charge on the feedback capacitor of the preamplifier. Whenever the output of the preamplifier is saturated in the high radiation field, the data logger for the integration mode counts the number of saturations of the CSA as the count mode detector. The remote monitoring system displays the neutron count rate using the measured data.

4.2.3 Preamplifier Design with Self-Reset Technique

The operation principle of the CSA is that the input charges induced from radiation detectors are stored in the feedback capacitor (C_F) and converted into the output voltage as determined by (4.1) [123].

$$V_{out} = -A_V \frac{Q_{in}}{C_{det} + (A_V + 1)C_F} \quad (4.1)$$

where A_V is the open loop gain of the OPAMP and C_{det} is the detector capacitance. When C_{det} is lower than $(A + 1)C_F$, the equation can be simplified as written by [122]:

$$V_{out} = -\frac{Q_{in}}{C_F}. \quad (4.2)$$

As aforementioned, the self-reset technique is applied to compensate for the output saturation in the high radiation field. The proposed preamplifier consists of the following circuits: CSA, comparator, monostable circuit, and feedback network, including a switch to reset saturated signals, as shown in Fig. 4.3 (a). The two-stage operational amplifier (OPAMP) with a self-bias circuit is used for the CSA. The two-stage OPAMP is well known for its high speed, low noise, low power, and proper gain. Fig. 4.3 (b) displays the schematic of the two-stage OPAMP. The feedback components are a capacitor of 0.75 pF and a resistor of 2 MΩ. Thus, the time constant is calculated as 1.5 μs. The value of each component is set by using an electronic design automation (EDA) tool. The feedback gain of the CSA is defined as the inverse of the feedback capacitance. A low feedback capacitance can allow the CSA to achieve a high feedback gain. However, it can quickly saturate the output of the CSA in the high radiation field, leading to a degradation in count rate. In terms of resistor, the feedback resistor is for discharging the capacitor after completion of the input signal conversion. The value of this resistor should be sufficiently

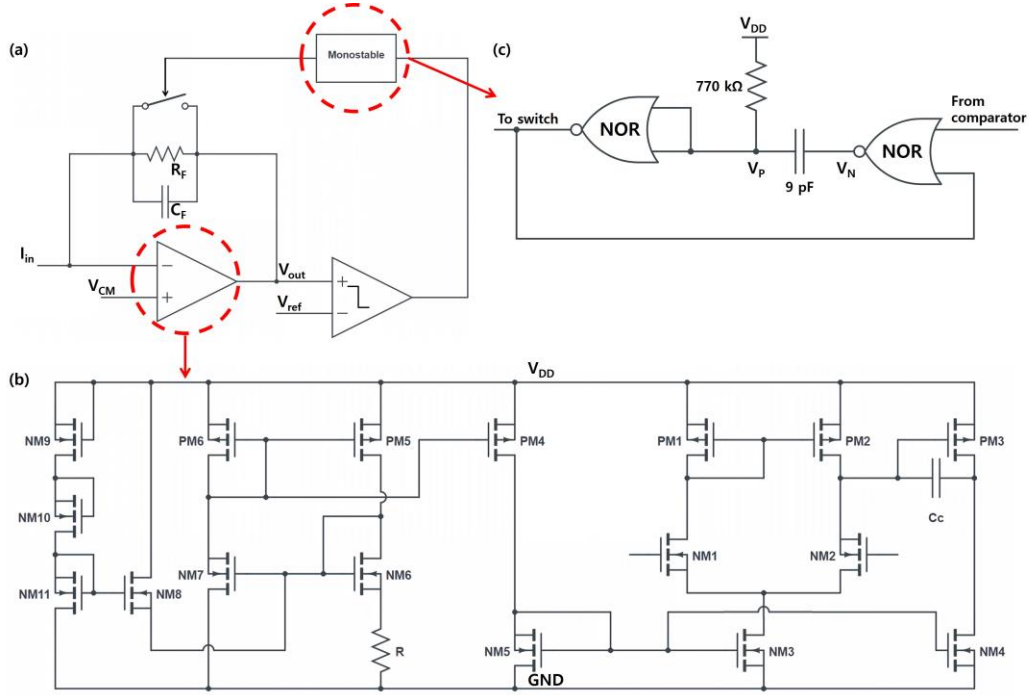


Fig. 4. 3. (a) Proposed preamplifier diagram including OPAMP, feedback network, comparator, and monostable circuit. (b) Conventional two-stage OPAMP topology. (c) Monostable circuit diagram.

large to ensure that all the charges inputted are stored on the feedback capacitor. However, if the resistance is too large, it can increase the RC time constant, resulting in a longer discharge time. Moreover, passive components can undergo the process variation during the fabrication. Therefore, the feedback components are used at the printed circuit board (PCB) level after being validated through EDA simulation.

The preamplifier could operate as a conventional CSA in a low radiation environment. On the other hand, when the preamplifier is used during high radiation events, the output of the CSA becomes larger than the reference voltage of the comparator due to

the pile-up phenomenon. Subsequently, the continuous comparator produces a reset signal employed by the monostable circuit to detect the input signal and trigger the feedback switch.

The monostable circuit comprises two NOR gates and an RC network, as depicted in Fig. 4.3 (c). It operates under the law of conservation of charge. As shown in Fig. 4.4, when the HIGH signal of the comparator enters the monostable input, the output voltage V_N of the NOR gate goes LOW and V_P also goes to LOW due to the charge conservation. Even if the input returns to LOW, the capacitor charges slowly, allowing the monostable output to remain HIGH. V_P increases to V_M , which is the voltage where the second NOR gate transition occurs, upon charging. The monostable output becomes LOW, provided to the first NOR gate, and V_N goes to HIGH. Subsequently, the V_P also increases up to the voltage expressed in (4.3) according to the charge conservation law.

$$V_P = V_M + V_{DD} \quad (4.3)$$

The capacitor is discharged slowly to V_{DD} , while the input of the NOR gate is zero.

The monostable circuit produces pulses with sufficient time to stabilize the system, even in process variations. During the reset phase, the charges stored in the feedback capacitor of the CSA may rapidly decrease, leading to instability caused by underdamping, occurring multiple up-and-down signals generated by the comparator that causes a

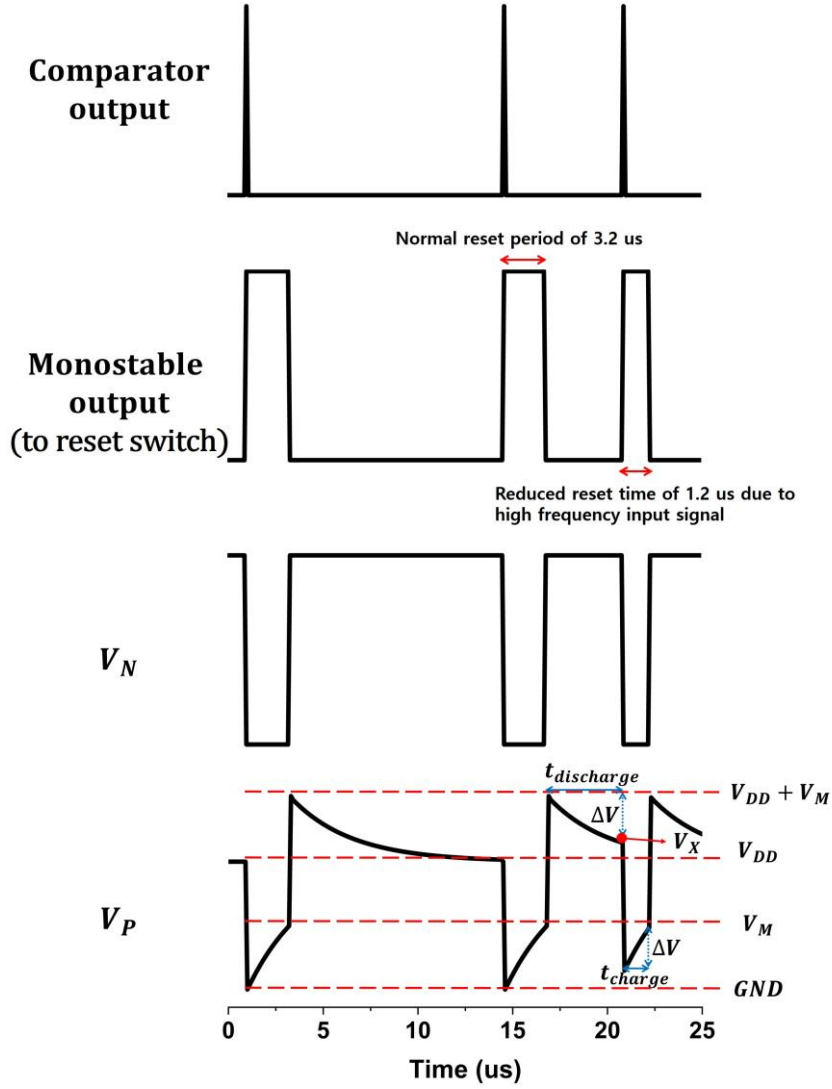


Fig. 4. 4. Operation principle of monostable circuit. When comparator signal enters monostable, the monostable output is generated. If discharge time is not sufficient due to high frequency input signals, the reset time will decrease.

malfunction of the self-reset technique. Thus, sufficient reset time can help minimize process variation and mismatch issues during the fabrication.

The reset time of the preamplifier is considered as a dead time of the system, causing the count rate degradation. However, the monostable circuit acts as an active dead time control (ADTC) circuit. For a complete reset, V_X should decrease to the V_{DD} in the discharge phase to maintain the constant pulse width. If the input signal speed is too high, V_X voltage may be higher than V_{DD} , namely insufficient discharge time, which reduces t_{charge} due to remaining charges. In other words, the dead time is actively controlled by the input period. Consequently, the degradation of the count rate can be reduced by using the monostable circuit.

4.2.4 Data logger and Remote Monitoring System

The signal processing unit and remote monitoring system have been developed to monitor measured data in the TREAT facility's control room in real-time. Analog and digital data loggers are used to collect and process the preamplifier data in integration and single-event modes, respectively. Table 4.1 shows the properties of the data loggers, respectively.

Whenever the CSA is saturated, the comparator generates the pulse. The analog data logger can function as an oscilloscope, allowing for monitoring of the preamplifier output state and logging of analog data within a 1 ms time window. On the other hand, the digital data logger counts the number of pulses generated by the comparator every 10 ms for integration mode detection, and then transfers the data to the monitoring system for post

Table 4. 1
PROPERTIES OF THE DATA LOGGER UNITS

Type	Digital	Analog
Channels	24	2
Sampling rate	800 MS/s	100 MS/s
Bandwidth	100 MHz	10 MHz
Voltage range	1.2 V to 3.3 V	$\pm 25V$
Manufacturer	Digilent	

processing from the count data to neutron flux. The software for the data loggers was provided by the manufacturer.

The remote monitoring system displays transient data acquired through the MPFDs readout system and reactor trigger signal on a PC in the control room. The user interface for remote monitoring utilized self-developed software. The monitoring system interface is shown in Fig. 4.5. The remote monitoring system receives cumulated data from the software for the data loggers over a duration of 10 ms. Users can set the baud rate to the desired speed. The baud rate was set to 115200 to obtain as much data as possible in this work. This program automatically detects and sets the USB port connecting the data logger. The data log window displays the parsed time and transferred data from the data logger. The main screen draws the count rate over time as a graph. All data, including the graph, can be stored on the laptop.

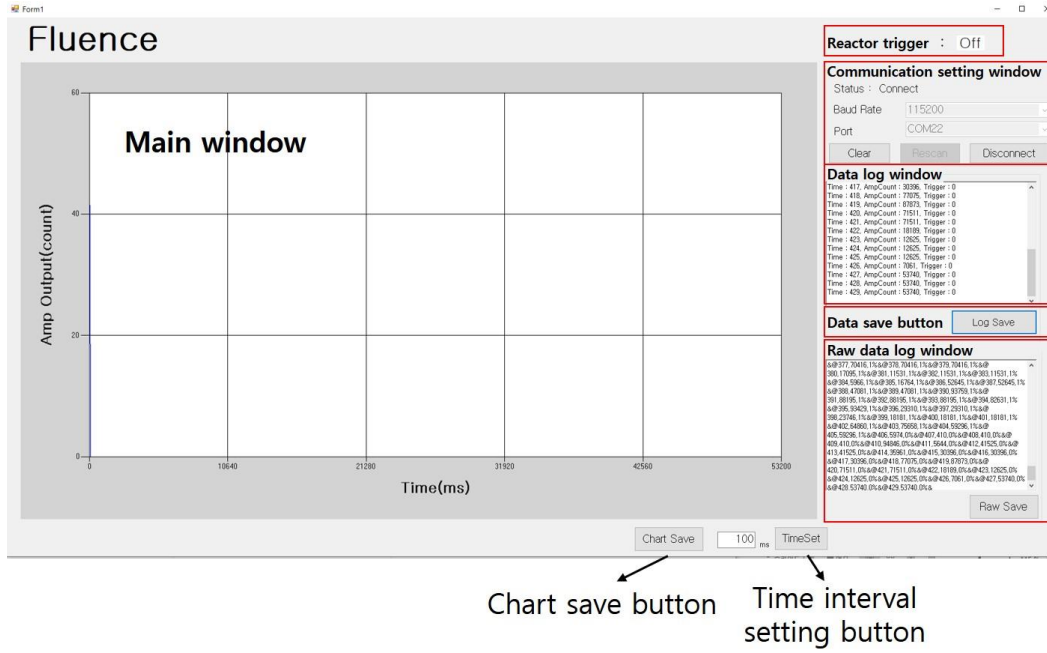


Fig. 4. 5. Software interface of the MPFD readout system.

4.3 Chip Implementation Details

The proposed preamplifier was realized in a complementary 180 nm CMOS technology process. A die photograph of the fabricated chip is shown in Fig. 4.6. The active area of the proposed circuit occupies 0.032 mm². The power is consumed about 63 mW at the steady state. Table 4.2 shows the specifications of the OPAMP for the CSA.

4.4 Measurement Results

4.4.1 Laboratory test

Before conducting neutron flux measurement tests in coupling with MPFDs, the operation of the proposed circuit was verified in laboratory environments. The proposed

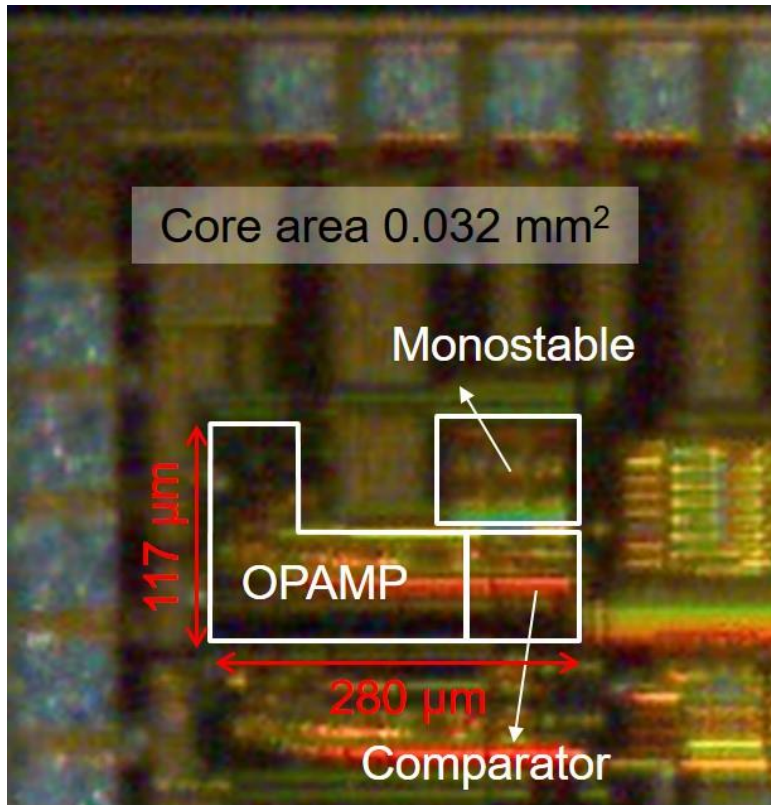


Fig. 4. 6. Die photograph of the fabricated preamplifier.

Table 4. 2
ELECTRICAL PARAMETERS OF THE OPAMP

Design Specifications	Value
Supply voltage (V)	1.8
Miller capacitance (pF)	1
Gain (dB)	66
3dB BW (kHz)	112.5
GBWP (MHz)	217.15
PM (°)	55
Power consumption (mW)	63

CSA was tested by applying a test current to verify the functionality of the preamplifier system. The discharge time was measured for both single event mode and integration mode, and the deadtime of the self-reset mechanism was also evaluated. To verify single mode operation, the test current was set to model the pulse generated by a single neutron in MPFDs, allowing a charge of 20 fC to flow with a pulse width of 200 ns. To verify integration mode, the pulse width was set to 10 μ s, ensuring continuous current flow. The reference voltage of the comparator was set to 1.6 V, activating the self-reset when the CSA output reached 1.6 V due to saturation.

As shown in Fig. 4.7 (a), in single event mode, the discharge of the input signal takes approximately 18 μ s. In integration mode, it was confirmed that the self-reset system operates as intended. The pulse width output from the monostable circuit was measured at 3.37 μ s.

4.4.2 Test Environment

The MPFDs readout system verification test was conducted at the TREAT reactor at INL, an air-cooled research reactor capable of generating up to 20 GWth of thermal reactor power within approximately 300 ms [138]. The tests were conducted twice under conditions of 2.1 GWth and 5.3 GWth, respectively. Fig. 4.8 provides an overview of the TREAT facility where the MPFDs are positioned in the reactor core. Signals of the MPFDs are transferred via a long cable of 22 m to the preamplifier in a DAS room inside TREAT to minimize the radiation effect on the system, as depicted in Fig. 4.9. The first laptop

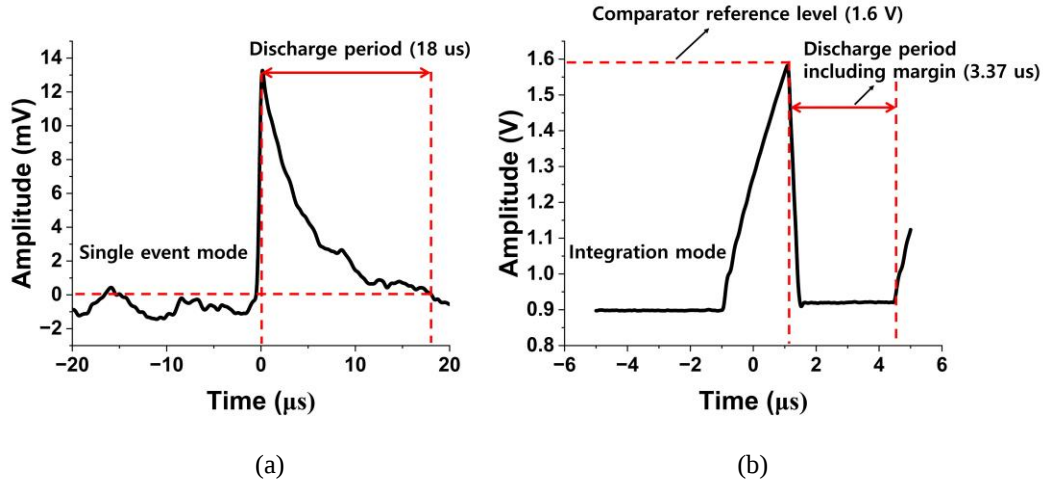


Fig. 4. 7. Verification test results for the self-reset technique of the CSA part: single event mode (a) and integration mode (b).

placed in the DAS room is connected to the second PC through the RS-422 communication protocol. For real-time monitoring, the second PC is controlled by the third PC located in the control room, which is approximately 1 km from the TREAT reactor, using the LAN cable. The DUT board has one preamplifier and a large coupling capacitor having a rated voltage of 1100 V to block the high supply voltage of 100 V at the input port. The additional comparator is installed to trigger the integration mode data logger, and the power supply box is used to minimize the overall system area.

4.4.3 Measured Pulses from a Reactor Transient Test

Fig. 4.10 illustrates the preamplifier output recorded during the reactor transient, revealing that the preamplifier becomes saturated due to the high neutron flux. Furthermore, the CSA undergoes an automatic reset whenever its output approaches 1.6 V, a reference

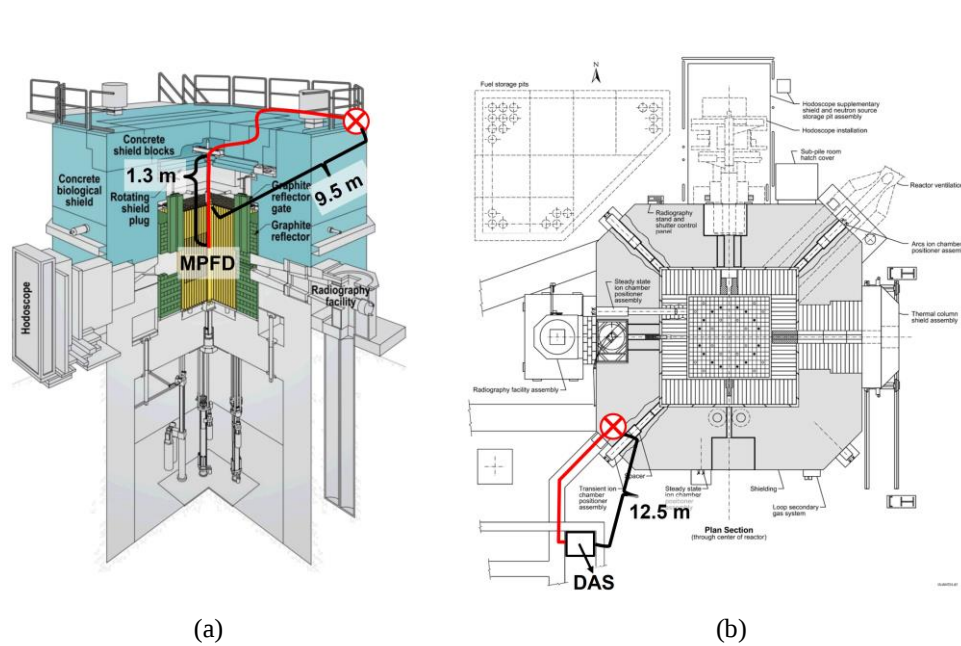


Fig. 4. 8. Overview of the TREAT facility. (a) Reactor cross-sectional view and (b) Reactor bird-eye view. Total distance from MPFDs to DAS is approximately 22 m.

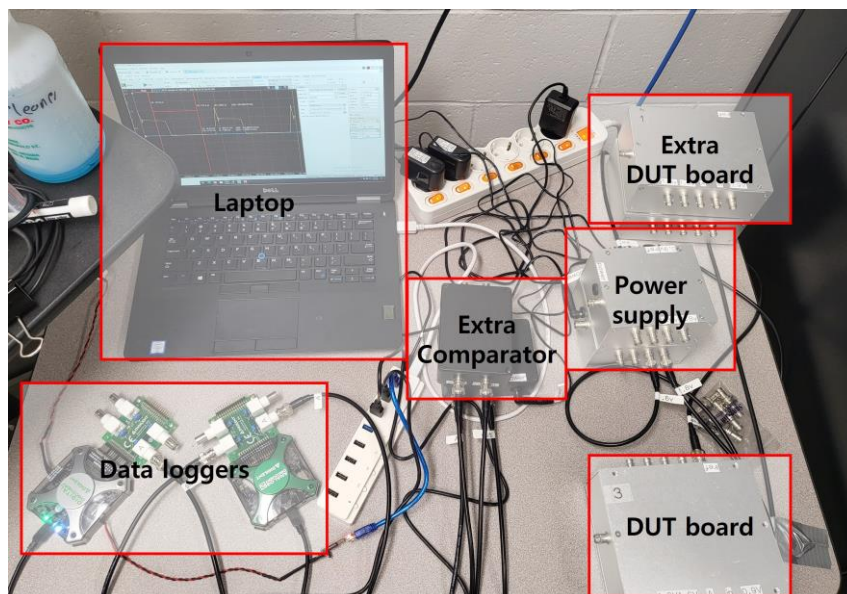


Fig. 4. 9. Developed MPFD readout system was installed at DAS. The overall system consists of the following blocks: DUT board, extra comparator, power supply, data loggers, and laptop.

voltage for the comparator that generates a reset signal. The saturation time and dead time are both dependent on the neutron flux. Specifically, in high neutron environments, the saturation period is relatively shorter, as illustrated in Fig. 4.10 (a), 3.72 μs and 2.76 μs , respectively. On the other hand, as shown in Fig. 4.10 (b), the rising time takes longer to saturate the CSA when the neutron flux is relatively low, 7.44 μs . Moreover, as mentioned before, the dead time is proportional to the input rising time due to the ADTC. Therefore, the dead time was measured as 2.04 μs , 1.8 μs , and 2.88 μs , respectively. As the test result, the range of the dead time is from 0.84 μs to 3.36 μs during the transient test according to the input frequency.

4.4.4 Transient Data Conversion Method

The obtained data need to be converted from the count rate to the neutron flux. The conversion of the MPFDs readout system was conducted using (4.4).

$$\varphi \text{ (n/cm}^2 \cdot \text{s)} = \frac{\alpha n}{S} \quad (4.4)$$

where α is the minimum number of neutrons required to saturate the CSA, n is the ideal count rate, and S is the sensitivity of MPFDs. The sensitivity S of the MPFDs was investigated using the MCNP6 in a full energy range of the neutron for the natural uranium having 300 Å thickness as expressed in (4.5) [138].

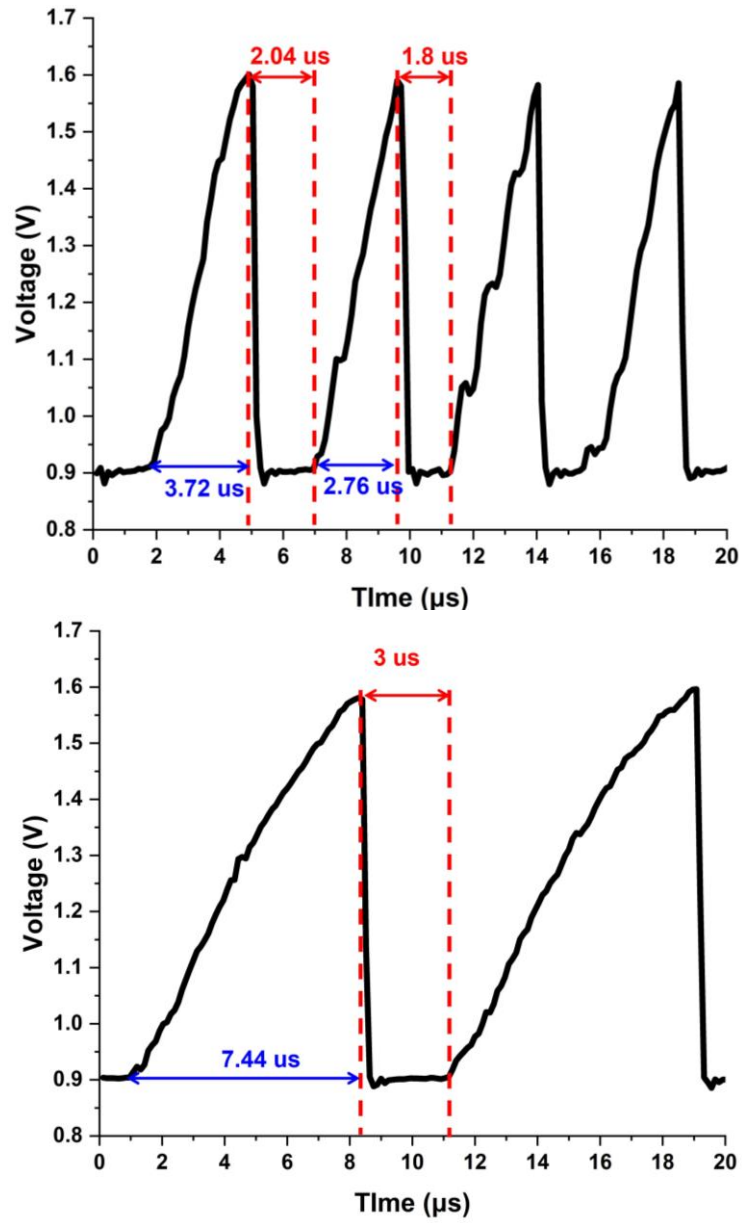


Fig. 4. 10. Analog result of transient tests. The preamplifier is automatically reset whenever output is saturated. The input rising time is determined by neutron flux and dead time. (a) Since the neutron flux is relatively high, the input rising time is also fast and dead time is short. (b) Since the neutron flux is relatively low, input rising time is slow and dead time is long.

$$S = 2.85 \times 10^{-9} \text{ cm}^2 \quad (4.5)$$

The α can be calculated as a ratio between the charge generated per reaction and the charge that can be stored in the circuit. The MPFDs is characterized by high repeatability in terms of charge generation, with approximately 20 fC charges generated per neutron interaction [143]. Since the input charges are deposited at the preamplifier up to 525 fC, which is calculated using (4.2), the minimum number of the pulse can be calculated as twenty-seven per saturation. Namely α is 27. Moreover, the proposed system can reduce the deposited charge variation due to the advantages of the current mode operation of the system [149].

The ideal count rate, n , is related to the dead time generated by electric circuits instead of the sensor in modern radiation detectors, including the MPFDs readout system [150]. Since the MPFDs readout system is considered the nonparalyzable model, (6) might be used for compensating the dead time in this work [148].

$$n = \frac{m}{1 - m\tau_{deadtime}} \quad (4.6)$$

where m is the measured count rate. To obtain the actual count rate, it is essential to be studied the dead time. As previously mentioned, the ADTC circuit can generate pulses of varying widths depending on the input rising time. Therefore, the following steps outline the calculation method for determining the dead time. The discharge phase of the

monostable is defined as (4.7). On the other hand, the charge phase is expressed as (4.8). The maximum charge time, denoted as $t_{charge,max}$, was determined to be 3.36 μs through experimental results.

$$V_X = ((V_M + V_{DD}) - V_{DD})e^{-\frac{t_{discharge}}{\tau}} + V_{DD} \quad (4.7)$$

$$V_M = -V_{DD}e^{-\frac{t_{charge,max}}{\tau}} + V_{DD} = (V_X - 2V_{DD})e^{-\frac{t_{charge}}{\tau}} + V_{DD} \quad (4.8)$$

Equation (4.9) is obtained by substituting (4.7) for (4.8) and rearranging the equation.

$$\frac{V_M}{V_{DD}}e^{-\frac{(t_{discharge}+t_{charge})}{\tau}} - e^{-\frac{t_{charge}}{\tau}} = \frac{V_M}{V_{DD}} - 1 \quad (4.9)$$

where τ is the RC constant of the monostable circuit. V_M and τ might be varied during the fabrication at a maximum rate of 30 %. Thus, V_M and τ values should be investigated before $t_{discharge}$ and t_{charge} are calculated. V_M term can be eliminated by replacing (4.8) with (4.9), and then the τ is the only variable.

$$e^{-\frac{(t_{discharge}+t_{charge})}{\tau}} - e^{-\frac{(t_{discharge}+t_{charge}+t_{charge,max})}{\tau}} - e^{-\frac{t_{charge}}{\tau}} + e^{-\frac{t_{charge,max}}{\tau}} = 0 \quad (4.10)$$

$t_{discharge}$ can be expressed as the rising time of the input, and t_{charge} is identical to the dead time of the preamplifier. Equation (4.10) is solved using the data shown in Fig. 4.10. As the result, the RC-constant was calculated as 4.9883 μ s, and V_M is 0.9178 V. The average period of a single saturated pulse could be obtained by dividing the analog data acquisition time into the count rate during the acquisition. Herein, it is necessary to establish the correlation between the pulse period and the dead time to compensate for the dead time degradation into total counts. The correlation is calculated by evaluating (4.10). The period is defined as the summation of the discharge and charge time. As mentioned above, the charge time of the monostable is replaced with the dead time. The exponential terms in (4.10) are replaced as shown in (4.11) in order to simplify the calculation.

$$X = e^{-\frac{t_{charge}+t_{discharge}}{\tau}}, Y = e^{-\frac{t_{charge}}{\tau}} \quad (4.11)$$

Therefore, the correlation equation is obtained:

$$Y = 0.49X + 0.51 \quad (0 < X, Y < 1) \quad (4.12)$$

The correlation graph between period and dead time is plotted as shown in Fig. 4.11, where the abscissa is the rising time of the average period, and the vertical axis is the dead time of the system. As the analysis result, the asymptotic line is drawn near 3.35 μ s, similar

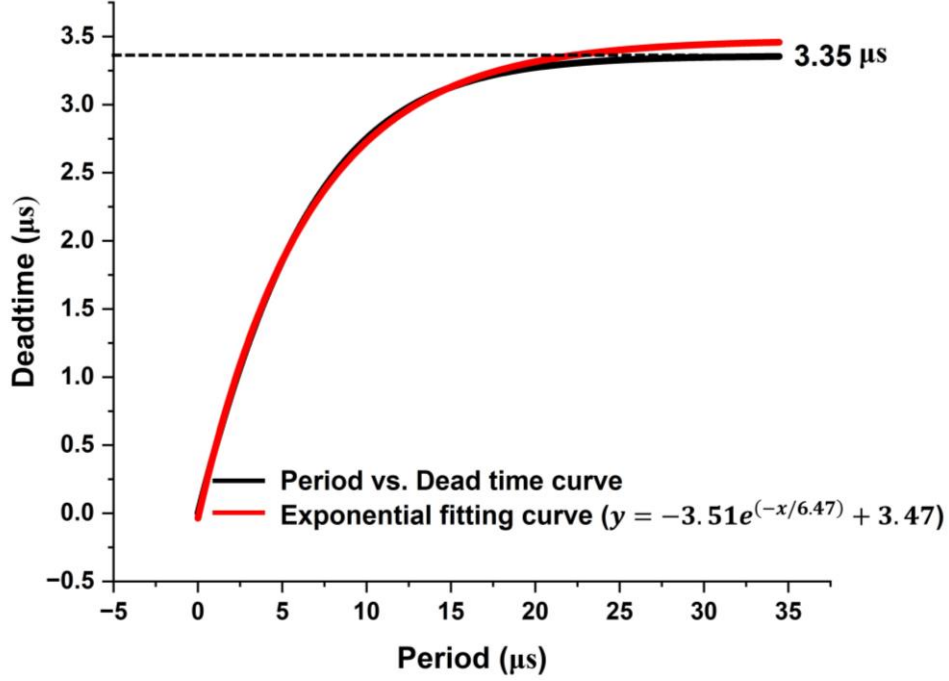


Fig. 4. 11. Correlation curve between input period and dead time. Since the correlation curve follows exponential function, the curve approaches to asymptotic line of 3.35 μs . The exponential trend curve is used for obtaining dead time by using the count rate.

to the maximum dead time of measured data during the transient test, as mentioned before.

The exponential trend curve is drawn to derive the period in which the asymptotic line is 3.47 μs as expressed in (4.13).

$$\tau_{dead\ time} (\mu\text{s}) = -3.51e^{\left(\frac{-avg.period}{6.47\ \mu\text{s}}\right)} + 3.47 \quad (4.13)$$

Therefore, the dead time compensation is achieved by substituting (4.6) with (4.13), as shown in (4.14),

$$n = \frac{m}{1+m(3.51e^{(\frac{1 \mu s}{m \times 6.47 \mu s})-3.47})} \quad (4.14)$$

Fig. 4.12 shows the simulation results of dead time variations under temperature variations from -20 °C to 80 °C. The x-axis represents the input time period, while the y-axis displays the variation in dead time. The degree of dead time variation is directly proportional to the period, with a maximum rate of 1045 ppm/°C.

4.4.5 Neutron Flux Data Conversion

The neutron flux data underwent cubic interpolation to increase the data points for accuracy analysis. The data was then processed using the conversion method from count rate to neutron flux. Fig. 4.13 illustrates the results of the TREAT transient test, including measuring reactor power through existing ex-core ion chambers positioned in the northwest, southwest, and southeast corners, as well as the neutron flux converted using the proposed method. The neutron flux was measured up to $7.2 \times 10^{15} \text{ n/cm}^2 \cdot \text{s}$ with full-width half maximum (FWHM) of 126 ms at the thermal power of 2.1 GWth during the 1st transient. According to the 2nd transient test, the neutron flux was counted as $1.24 \times 10^{16} \text{ n/cm}^2 \cdot \text{s}$ with FWHM of 136 ms while the maximum power was 5.1 GWth.

4.4.6 Transient test result analysis

The transient test results are discussed based on the conversion results in this section. To qualify the accuracy of the measured neutron flux, data from previous research

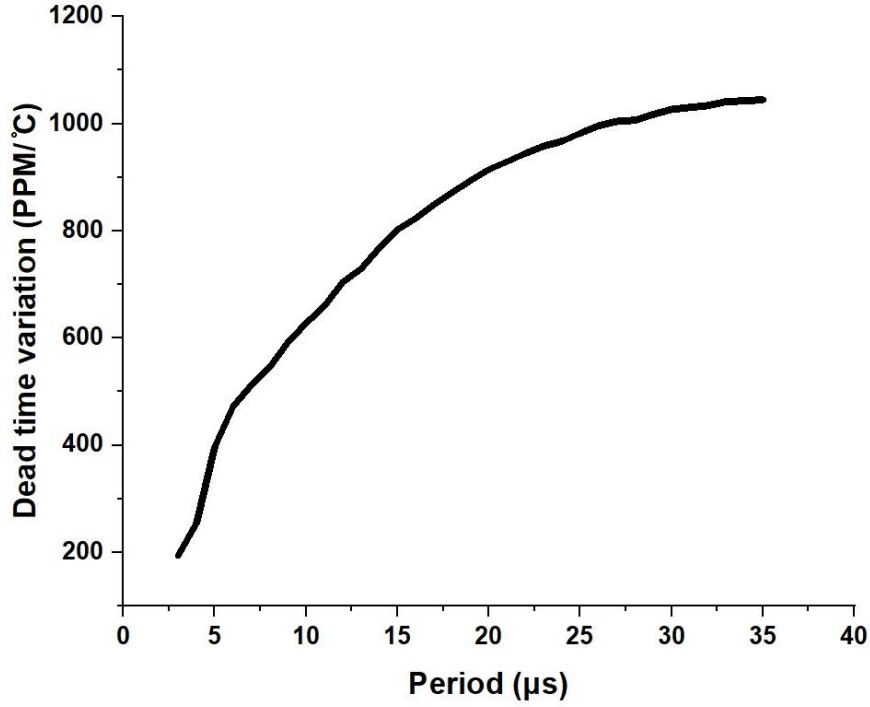


Fig. 4. 12. Simulation result of temperature variation from -20 °C to 80 °C. The result shows how the dead time varies for each input period as the temperature changes. The investigation revealed that as the input period increases, the variation in dead time also increases.

conducted with MPFDs experiments at TREAT in 2017 was used as a reference. The comparison between the converted neutron flux values from the current experiment and the previously reported data allows for a qualitative assessment of the accuracy and reliability of the measurements. The reported neutron flux was $4 \times 10^{11} n/cm^2 \cdot s$ during the steady-state test with a maximum thermal power of 120 kW [151]. By using the thermal power obtained during the reactor transient tests, which was 2.1 GW and 5.1 GW, we can convert this neutron flux to be $7.1 \times 10^{15} n/cm^2 \cdot s$ and $1.71 \times 10^{16} n/cm^2 \cdot s$, respectively. After the conversion process, the error was observed as -1.5 % and 38 %

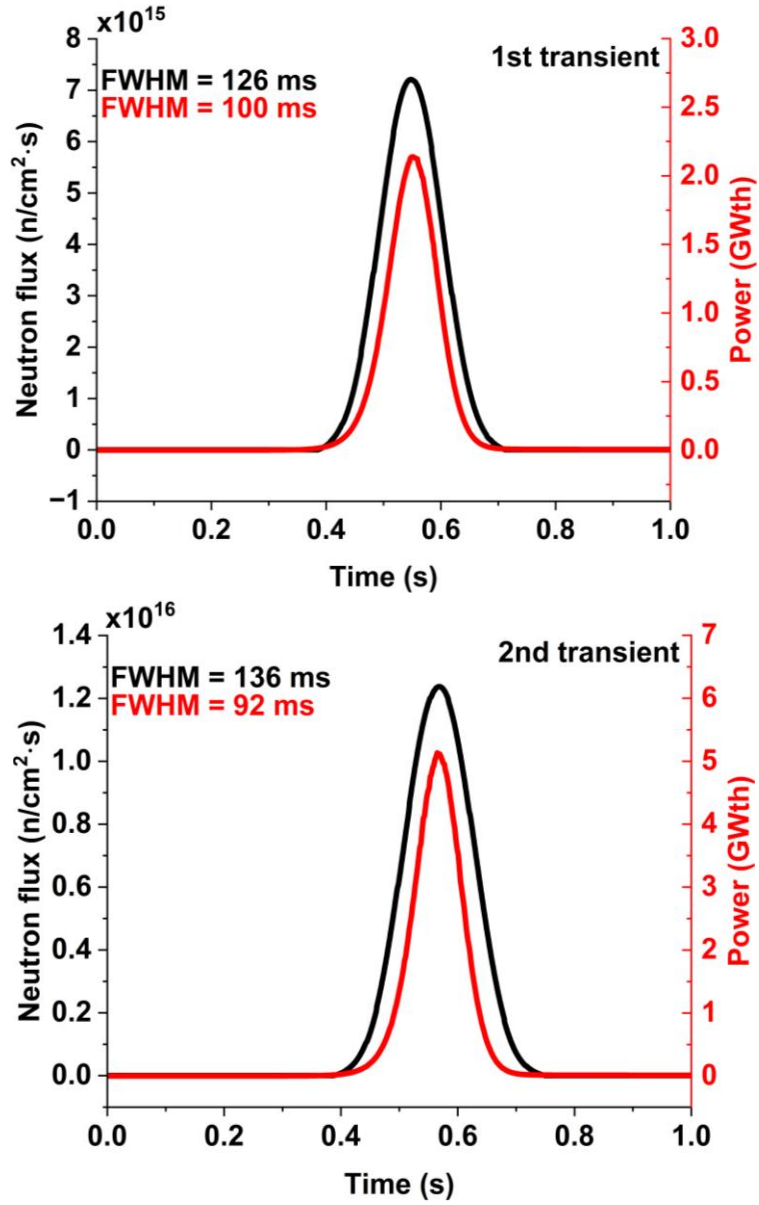


Fig. 4. 13. Reactor transient test results of neutron flux and reactor power. (a) When reactor power is 2.1 GWth, measured neutron flux is $7.2 \times 10^{15} \text{ n/cm}^2 \cdot \text{s}$ having FWHM of 126 ms. (b) When reactor power is 5.1 GWth, measured neutron flux is $1.24 \times 10^{16} \text{ n/cm}^2 \cdot \text{s}$ having FWHM of 136 ms.

between the obtained data and the calculated data for comparison at each thermal power, 2.1 GW and 5.1 GW, respectively. As aforementioned, during the detection process, fission reactions occur, which leads to a reduction in the number of neutron-reactive materials. As a result, the sensitivity of the MPFDs are degraded, which could be a contributing factor to the 38 % error observed in the results.

4.5 Discussion and Conclusion

4.5.1 Comparison of Count Rate

The calculated data for circuits with a constant dead time and ADTC can be calculated using equations (4.6) and (4.14) respectively. The dead time is specified as 3.36 μs and 0.8 μs , which correspond to the observed maximum and minimum values, respectively, obtained from the monostable circuit during the reactor transient test. Fig. 4.14 illustrates the calculation results.

The ideal count rate refers to the number of signals generated at the detector within 1 ms time window. For instance, if the ideal count rate is 650, then the actual count rate would be calculated as 204 (3.36 μs), 427 (0.8 μs) by using (4.6) in the conventional case. In contrast, ADTC can be calculated as 446 using (4.14). Consequently, the constant dead time circuit experiences a degradation in the count rate as the number of input signals increases, particularly with increasing dead time. In contrast, the ADTC circuit demonstrates a more linear response to the ideal count rate compared to the constant dead

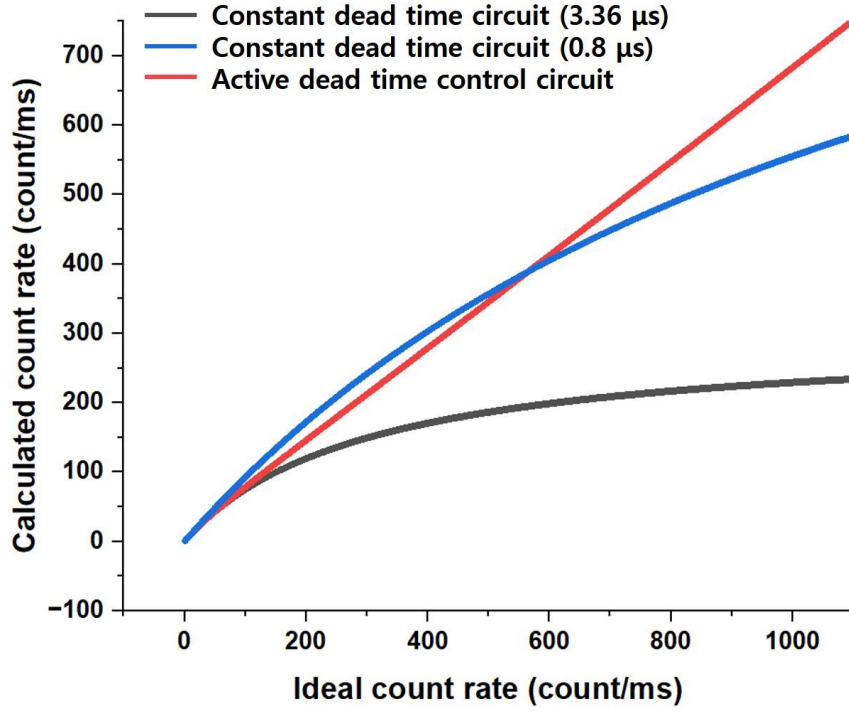


Fig. 4. 14. Comparing result of calculated count rate. Three cases are analyzed when the dead time is constant as 3.36 μ s and 0.8 μ s, and the dead time is actively controlled by the monostable.

time circuits. Therefore, the proposed preamplifier can compensate for the degradation of the count rate.

4.5.2 Power Consumption

In addition to its count rate compensation benefits, the ADTC also offers the advantage of reducing power dissipation. The power consumption during the charge time is proportional to the square of the voltage difference, as described in equation (4.3).

$$P = \frac{C}{2} \{V_M - (V_X - V_{DD})\}^2 = \frac{C}{2} \Delta V^2 \quad (4.15)$$

Section 4.4.3 introduced the conversion method for converting the count data to the neutron flux. In this section, comparisons of count rate and power consumption between the conventional reset circuit and the ADTC circuit are shown. The trigger circuit of the switch for the reset is usually designed using the inverter delay cell array [35]. The delay of the inverter delay cell is calculated as:

$$t_d = \sum_{j=1}^N t_{d,j} = 0.69 R_{eq} (C_{int} + C_{ext}) N. \quad (4.16)$$

where R_{eq} is an equivalent resistance of the inverter, C_{int} is an internal capacitance, C_{ext} is an external capacitance, and N is the number of inverter stages. To achieve the desired delay, either a large capacitance or a number of inverters is required since the discharge period is determined by the RC time constant. It becomes possible to simplify the modeling process for calculating the count rate and power dissipation, by assuming that the dead time of the monostable circuit remains constant while only the capacitance varies based on the dead time. Therefore, the capacitance is set to 9 pF and 2.25 pF, corresponding to the dead times of 3.36 μ s and 0.8 μ s, respectively. As the remaining charges in the capacitor of the monostable circuit decrease the voltage difference, the power dissipation is also reduced in the high radiation field. Fig. 4.15 compares the power consumption of

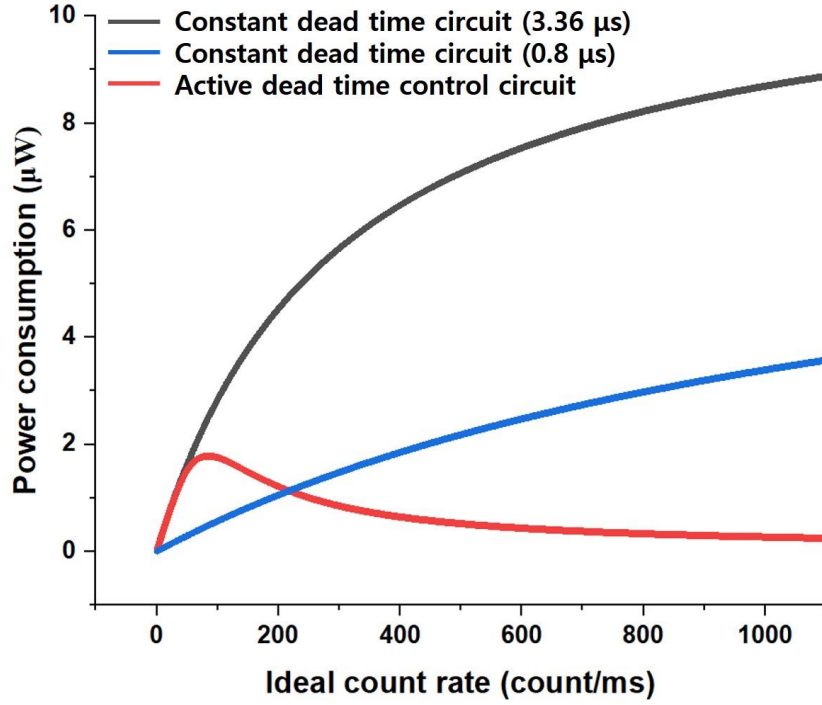


Fig. 4. 15. Comparing result of power consumption. Three cases are analyzed when the dead time is constant as 3.36 μs and 0.8 μs , and the dead time is actively controlled by the monostable.

the ADTC circuit and constant dead time circuits having 3.36 μs and 0.8 μs , respectively. Consequently, the ADTC circuit has the lowest power dissipation among the three cases after the ideal count rate of 200.

4.5.3 Conclusion

The MPFDs readout system was developed, including the preamplifier with self-reset, the data loggers, and the remote monitoring system. The proposed system can operate

in integration and single-event modes. The integration mode is merged with the conventional current and count modes for radiation detection, where the data logger for integration mode counts the number of saturated outputs of the CSA. On the other hand, the single event mode functions as an analog data logger, capturing and storing data every 1 ms. The monostable circuit is exploited for the self-reset of the preamplifier. The pulsewidth of the monostable output for the self-reset is chosen with sufficient margin to discharge the capacitor stably, regardless of the process variation during fabrication. Thus, the ADTC is introduced to compensate for the longer reset period considered as the dead time of the system. The measured data can be converted from the count rate to the neutron flux using the conversion method. The MPFDs readout system could track the reactor power level as the test result. The conversion results show that the neutron flux is measured as 7.2×10^{15} n/cm²·s with FWHM of 126 ms and 1.24×10^{16} n/cm²·s with FWHM of 136 ms at a thermal power of 2.1 and 5.1 GWth, respectively.

This technology is used to extend the measurement range of the count mode in neutron detectors. Typically, neutron detectors are designed to operate in different modes depending on the flux level: pulse count mode, AC current mode, and DC current mode [7]. By utilizing this technology, the reliability in the overlap region during the transition from pulse count mode to AC current mode can be enhanced. Furthermore, as most radiation detectors experience pile-up effects, applying the proposed technology can not only effectively mitigate pile-up issues but also resolve the count rate reduction problem that occurs during the reset process.

CHAPTER 5

Rad-Hard Time-to-Digital Converter for Time-Based Detectors

5.1 Background

Research on time-based detectors in radiation measurement systems has been widely pursued, with the most significant developments occurring in the field of high-energy physics. Particle physics laboratories, such as the European Organization for Nuclear Research (CERN), utilize time-based signal analysis to determine the position, time, energy, and momentum of high energy particles produced by proton collisions in particle accelerators. This technology has gradually expanded into applications such as positron emission tomography (PET) systems, Light Detection and Ranging (LiDAR) using Time-of-Flight (ToF), and all-digital phase-locked loops (ADPLLs). In these applications, time-to-digital converters (TDCs) are employed for precise time measurement.

In the field of high-energy physics, the momentum of muons is measured using the Compact Muon Solenoid (CMS) detector and the Monitored Drift Tube (MDT) of the AToroidal LHC Apparatus (ATLAS), both installed in the Large Hadron Collider (LHC) [152, 153]. Muons generate Electron-Ion Pairs, and the charges drift towards their respective electrodes. A TDC is used to measure the time difference between the signals generated due to the mobility difference [154]. The ATLAS and CMS detectors were also used in the 2013 discovery of the Higgs boson [155]. To observe the Higgs boson, a large amount of data and images were obtained using silicon pixel modules and analyzed

statistically. The silicon pixel, a reverse bias diode, interacts with high-energy particles to generate charge at the junction, which is then converted to a voltage signal by the preamplifier. Subsequently, the discriminator generates a pulse signal for periods exceeding a specific threshold voltage, and the TDC measures the pulse width, as illustrated in Fig. 5.1. This method is called Time Over Threshold (TOT) and is more efficient than voltage-domain signal processing [156].

The use of radiation in the medical field began with the discovery of radiation. Just three days after the discovery of X-rays, Ludlam proposed using X-rays for radiation therapy [157]. Since then, radiation therapy has expanded to include various treatments using other kinds of radiation, such as proton and heavy-ion therapy. Additionally, radiation-based cancer diagnostic techniques, such as medical imaging, have advanced significantly. Positron emission tomography (PET) is the most common technique, where a positron-emitting radioactive isotope is injected into the patient, and the 0.511 keV gamma rays emitted in opposite directions during positron annihilation are measured to determine the location of cancer [158]. The basic structure of PET is shown in Fig. 5.2. As depicted in Fig. 5.2 (a), the gamma rays generated by annihilation are emitted at 180 degrees, and the timestamps of signals from the coupled detectors are recorded using TDCs. The actual position is then determined through data processing [159].

In the event of a nuclear power plant accident or decommissioning, research is being conducted to accurately understand radiation distribution through radiation mapping technologies [160-162]. This technology is crucial for accurately determining the location

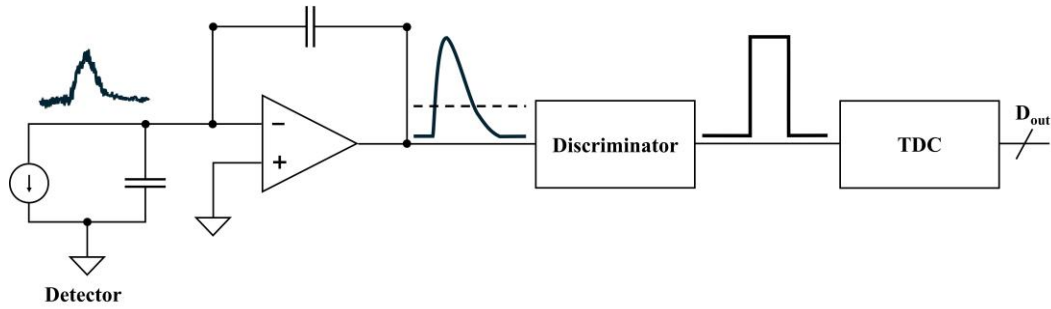


Fig. 5. 1. Block diagram of a silicon pixel detector. When charge-based signal is processed through preamplifier, a pulse is generated by threshold discriminator. This pulse is subsequently measured by Time-to-Digital Converter (TDC), enabling the determination of the time over threshold.

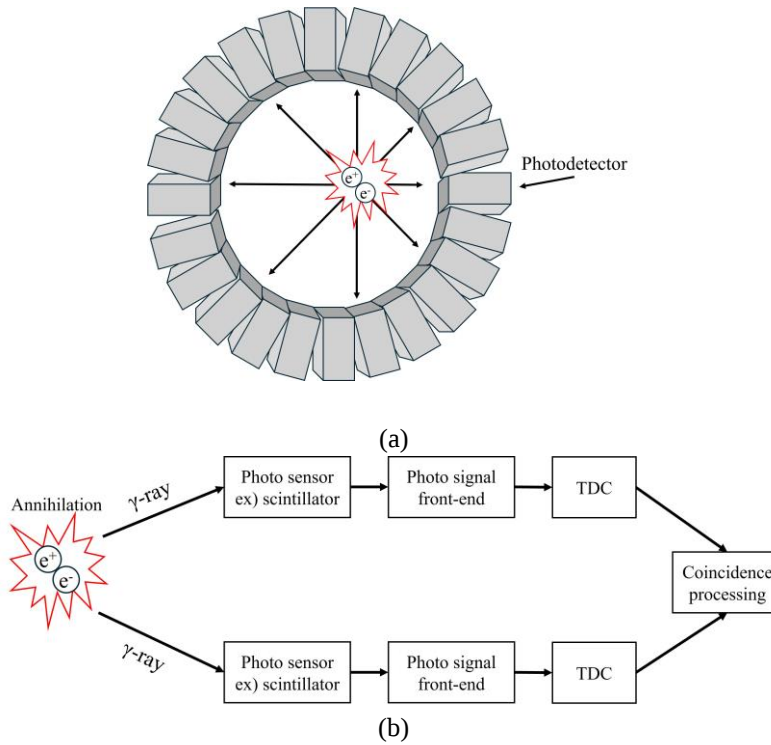


Fig. 5. 2. (a) illustration of a Positron Emission Tomography (PET) scanner and (b) block diagram of PET system. When gamma rays produced by electron-positron annihilation are emitted at a 180-degree angle, the time difference between their detection by two silicon pixel detectors is measured by Time-to-Digital Converter (TDC). The accumulated data from these measurements are then utilized to accurately determine the location of tumors within the body.

of radiation sources to prevent further damage. For radiation mapping, drones or nuclear emergency response robots are often employed, using simultaneous localization and mapping (SLAM) for 3-D mapping. The LiDAR system, which typically uses direct Time-of-Flight (dToF) technology, is widely used for 3D mapping [163]. Fig. 5.3 shows the dToF LiDAR system diagram. A TDC measures the time taken for light emitted from the light diode to return after hitting a target, thereby determining the height and distance.

These applications are deployed in high-radiation environments, necessitating advanced radiation hardening. For instance, the ATLAS detector at CERN requires a radiation tolerance exceeding 300 kGy [164], while the electronics utilized in the International Thermonuclear Experimental Reactor (ITER) should endure radiation doses surpassing 5 MGy [167]. In addition to these experimental facility requirements, in 2017, six years after the Fukushima Daiichi Nuclear Power Plant incident, an attempt was made to assess the reactor fuel condition using the Scorpion robot. However, the robot was exposed to radiation dose rate of 650 Gy/h near the Primary Containment Vessel (PCV) and consequently failed within two hours [165]. For effective three-dimensional mapping of accident sites using robots or drones, attributes such as compactability for navigating confined spaces, durability to withstand collisions with obstacles, high sensibility for detecting obstacles, and advanced mobility, including obstacle avoidance, are essential [166]. However, radiation shielding solutions using heavy materials such as lead or tungsten present significant limitations for these applications [166]. Therefore, enhancing the radiation tolerance of TDCs is crucial for reliable time-based signal processing in

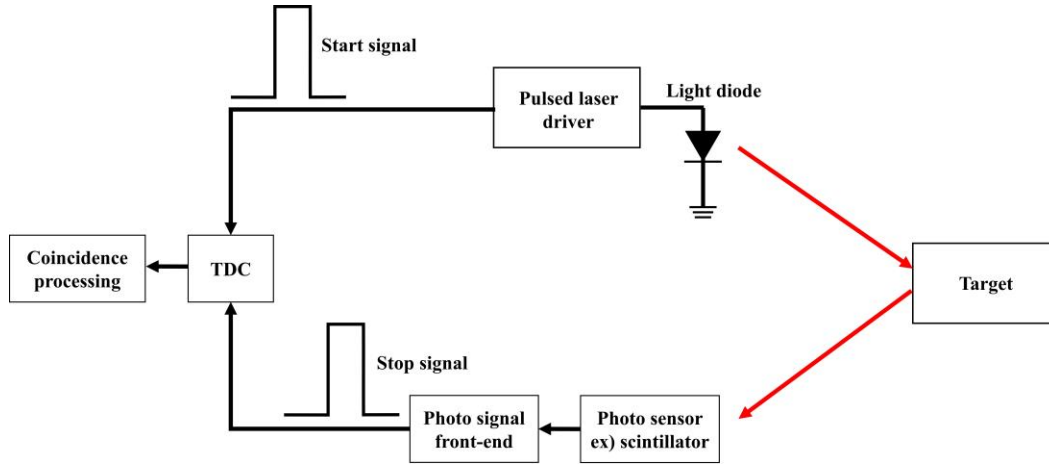


Fig. 5. 3. block diagram of dTOF LiDAR system. In this system, light is emitted from a light diode and travels towards a target. Upon collision with the target, the reflected light returns to the receiver. TDC measures the time interval between the emission and reception of the light pulse.

various radiation-prone environments. This chapter introduces radiation hardening techniques for TDCs used under these challenging conditions for medical imaging applications.

5.2 Rad-Hard Time-to-Digital Converter

Various types of TDCs have been developed, and this paper focuses on a two-step pipeline structure using a Time Amplifier (TA). The most commonly known TDC utilizes the delay of inverters, and to overcome the gate delay limitations of inverters, the Vernier Delay Line (VDL) was proposed [168]. However, this structure results in very high area consumption since the dynamic range and the number of delay cells increase proportionally. Additionally, when exposed to radiation, delay cell mismatch increases, leading to a degradation in linearity [169]. To alleviate the mismatch issue among inverters in VDL-

TDC, structures using Delay Locked Loops (DLL) or PLL were proposed [170]. However, these structures are more vulnerable to radiation, and exposure to radiation causes performance degradation in the circuits constituting the DLL and PLL, resulting in linearity degradation [171]. To overcome the limitations of VDL-TDC, a structure that replaces delay cells with a Ring Oscillator (RO) was proposed [172, 173]. By using a 2D Gated Ring Oscillator Vernier Delay Line (GRO-VDL), the dynamic range can be significantly improved through multiple laps without requiring many delay cells, yielding substantial benefits in terms of power consumption and area [172]. However, the layout becomes highly complex. Moreover, radiation can increase the mismatch between the time comparator and the GRO, potentially degrading linearity. The multiphase GRO-TDC structure activates the GRO upon the occurrence of a timing event and deactivates it upon receiving a stop signal, thereby enabling noise shaping [173]. However, in this configuration, it is necessary to preserve the phase even during intervals in which no input signal is present. This requirement causes a skew error attributed to leakage currents, and the resulting linearity degradation becomes more pronounced, particularly as leakage currents intensify under Total Ionizing Dose (TID) effects.

The TAs have become a crucial block in recent TDC designs [174 - 176]. TDCs used in time-based signal processing operate fundamentally based on the gate-delay of inverters. Various topologies have been proposed to improve time resolution below the gate delay. Recently, the predominant approach is the utilization of TAs which amplify the time difference between two inputs, allowing for a reduction in time resolution to below the gate

delay [177]. However, traditional TAs have limitation of linearity, restricting the dynamic range. To overcome the limitation, pulse-train TA (PTTA) has been proposed, demonstrating higher linearity [178]. However, when used in high radiation environments, the PTTA may encounter skew error issues. The TA output is altered due to skew error, leading to a degradation in the overall TDC linearity. This dissertation presents a study focused on alleviating the effects of radiation, particularly TID effects that increase leakage current, by utilizing a TA that incorporates a skew error mitigation technique.

5.2.1 Design of A-PTTA Circuit

The conventional PTTA is designed with simplicity, consisting of delay components, pulse generator, and OR gate as illustrated in Fig. 5.4 [178]. N pulses generated by the TA are input into the TDC, resulting in a total of N conversions. The TDC employs a ring oscillator, which measures the number of phase shifts each time a pulse is received to calculate the corresponding time. In this context, the delay of the delay circuits (τ_d) must be larger than the dynamic range of the TDC to prevent overlap with subsequent pulses. Consequently, when the incoming time difference is shorter than the delay of the delay circuit, an off-state time (T_{off}) occurs. During this off-state time, charge must be stored in the parasitic capacitors within the inverters of the ring oscillator. As shown in Fig. 5.5, It leads to two problems: skew error and the conversion rate. When the input time difference

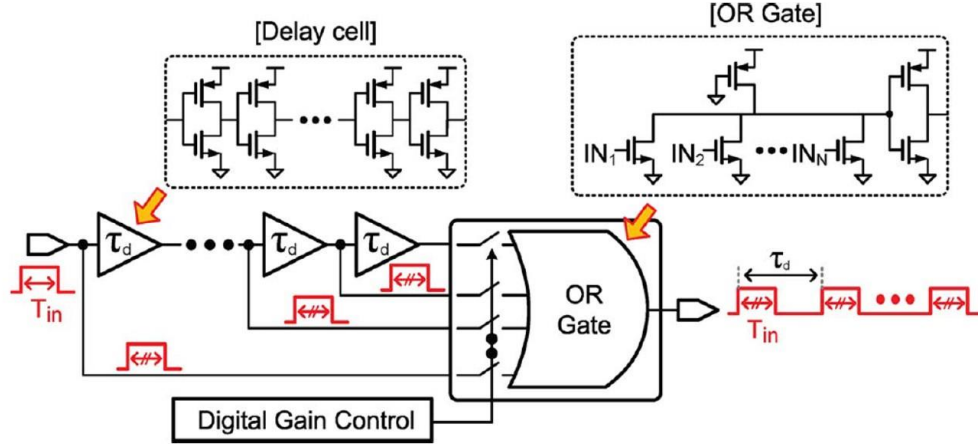


Fig. 5. 4. Traditional pulse-train time amplifier [170].

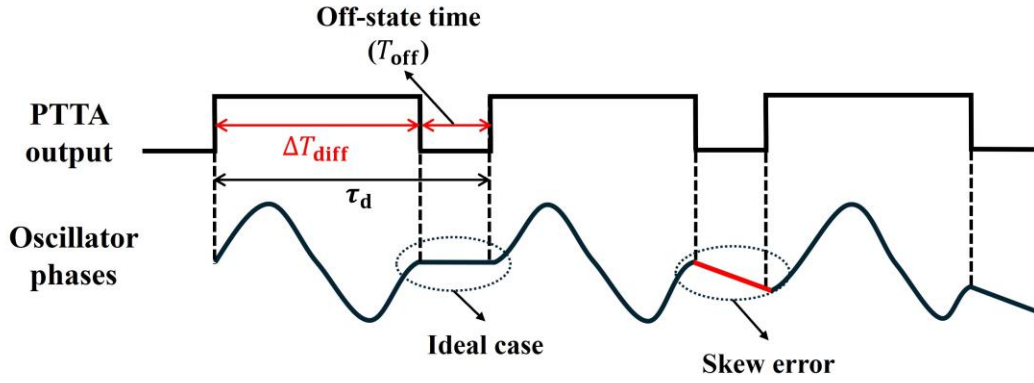


Fig. 5. 5. Timing diagram of gated ring oscillator TDC with PTTA. Long off-state time can lead to skew error.

(ΔT_{diff}) is significantly shorter than τ_d , off-state time increases according to (5.1), resulting in linearity degradation due to skew error.

$$T_{off} = \tau_d - \Delta T_{diff} \quad (5.1)$$

Moreover, in terms of the conversion rate, even when ΔT_{diff} is highly short, the same conversion time is required as when ΔT_{diff} is long.

In particular, the use of PTТА in radiation environments further exacerbates the impact of skew errors. As discussed in Chapter 2.2.1.2, prolonged radiation exposure of MOSFETs leads to cumulative damage, particularly the formation of leakage current paths due to charge accumulation in the field oxide region. This accumulation results in increased charge loss during off-state periods. Therefore, this article implemented an advanced pulse-train time amplifier (A-PTТА) which can automatically control the off-state time to mitigate skew error.

The A-PTТА consists of delay circuits, pulse generator, D-flipflops (DFFs), and control logic circuit as drawn in Fig. 5.6. The main idea is intentionally exploiting the overlap phenomenon. The τ_d is set to be shorter than that of the conventional PTТА with the same dynamic range. Consequently, the probability of overlap increases depending on ΔT_{diff} in A-PTТА. Three DFFs can provide the overlap code (O-code) whether overlap occurs between the first pulse and the next three output pulses. The spacing between delay cells is determined by the O-code. If Q[0] is high and the others are low, the delay cell spacing is set to 1. Thus, by skipping one delay cell at a time in the output, overlap is avoided, and the off-state time is minimized. Fig. 5.7 illustrates the timing diagram for the example. D[0] and D[1] overlap, while D[0] and D[2] do not. It means the second delay chain is chosen as shown in Table 5.1, resulting in the output of D[2] after D[0]. The TA

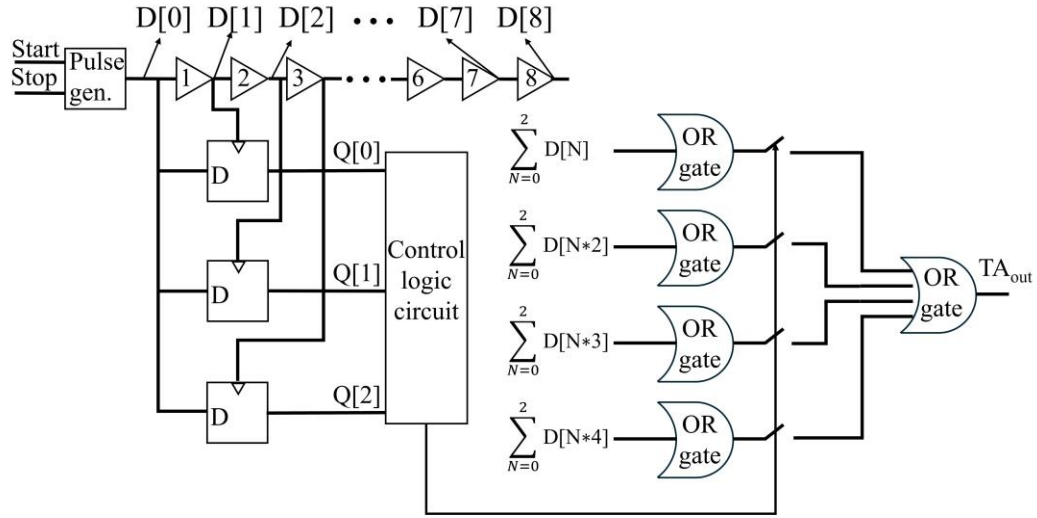


Fig. 5. 6. Block diagram of proposed A-PTTA. Inverter stage responsible for generating the output is determined by the O-code produced by the three DFFs.

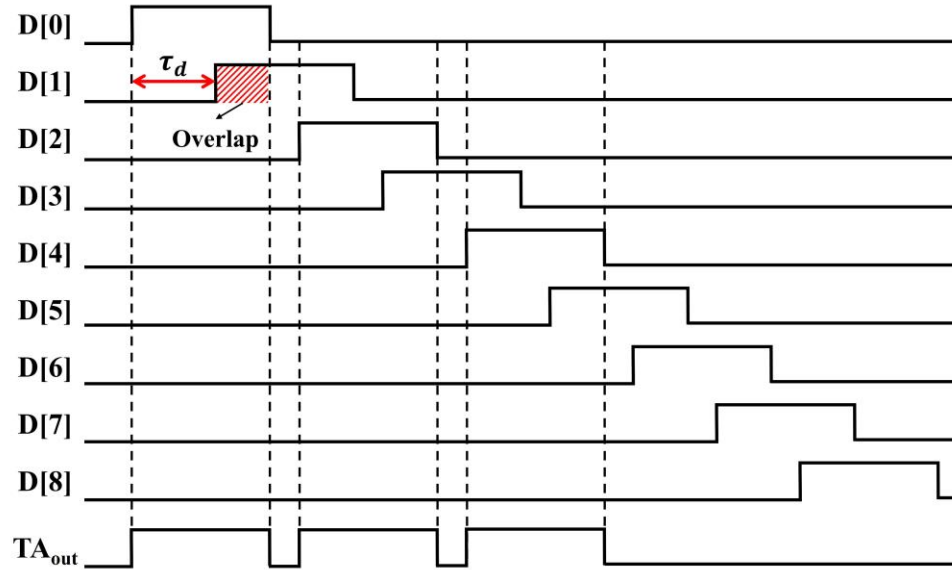


Fig. 5. 7. Timing diagram of proposed A-PTTA with gain of 3.

Table 5. 1
A-PTTA OUTPUT DELAY CHAIN BASED ON O-CODE

Q[0]	Q[1]	Q[2]	Delay chain of output
0	0	0	D[0]-D[1]-D[2]
1	0	0	D[0]-D[2]-D[4]
1	1	0	D[0]-D[3]-D[6]
1	1	1	D[0]-D[4]-D[8]

gain is set to 4, allowing the generation of pulses four times, denoted as D[0], D[2], D[4], and D[6].

5.2.2 Design of Rad-Hard Adaptive TDC

The proposed TDC was designed using a two-step topology for PET application. This two-step design employs a coarse-fine structure, enabling parallel operation, which offers advantages such as a high conversion [165]. The proposed design consists of four TDCs connected in series. Figure 5.8 illustrates the block diagram of the overall radiation-hardened adaptive TDC.

When a time difference is input, a 480 ps biased pulse is generated by the pulse generator within the A-PTTA. To prevent the input from being skipped due to the rapid operation of the counter (CNT), the time difference is biased by 480 ps. The biased time difference is then amplified three times by the A-PTTA and fed into the TDC module. The TDC comprises a ring oscillator and a CNT, which count the number of transients to measure time. The ring oscillator utilizes a three-stage current steering inverter structure,

achieving a resolution of 750 ps. The data measured by the ring oscillator is stored in a DFF, and simultaneously, an error detector operates to measure the residue time ($T_{residue}$). To improve the conversion rate, it operates in a pipeline TDC. Once the operation of the first fine TDC is complete, the second TDC activates, while both the coarse TDC and the first fine TDC are reset and remain in a standby state until the next signal arrives. Additionally, since the pipeline TDC structure is used, it is possible to select only the desired TDC for data acquisition. For example, using only the coarse TDC provides a resolution of 245.7 ps, using up to the first TDC provides 81.9 ps, using up to the second TDC provides 27.3 ps, and utilizing data from all TDCs achieves a resolution of 9.1 ps.

As shown in Figure 5.9, the error detector initiates operation from the point when the ring oscillator completes the conversion, measuring the time until the next two-phase transient occurs to determine the error time (T_{error}). Using the obtained data, $T_{residue}$ can be calculated as follows:

$$T_{residue} = T_{error} - T_{LSB}. \quad (5.2)$$

Where, T_{LSB} represents the resolution of the ring oscillator, which is 750 ps. The time difference generated by the error detector is input into the 1st fine TDC system. This process is then repeated two additional times, enabling operation up to the third TDC system. Subsequently, the data stored in the D flip-flops (DFFs) are output and processed post-simulation to calculate the final time difference.

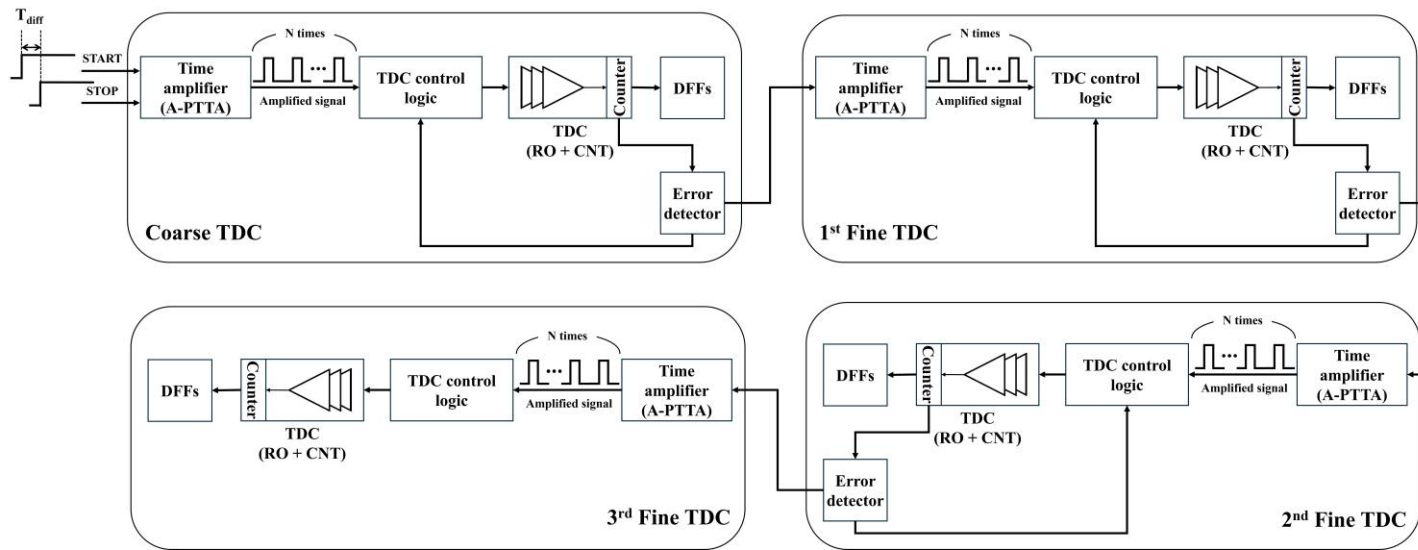


Fig. 5. 8. Block diagram of proposed TDC. It operates using pipeline architecture composed of four stages.

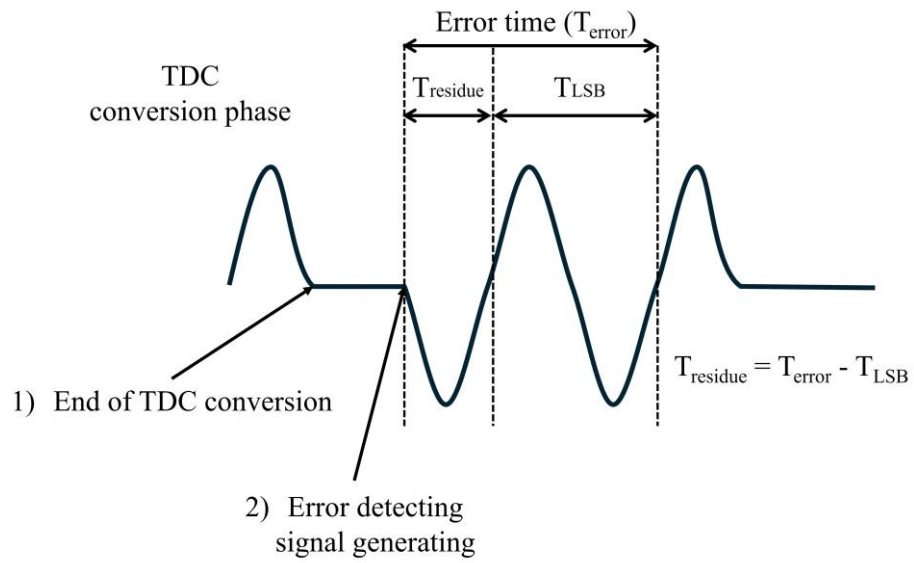


Fig. 5. 9. Operation principle of error time detector.

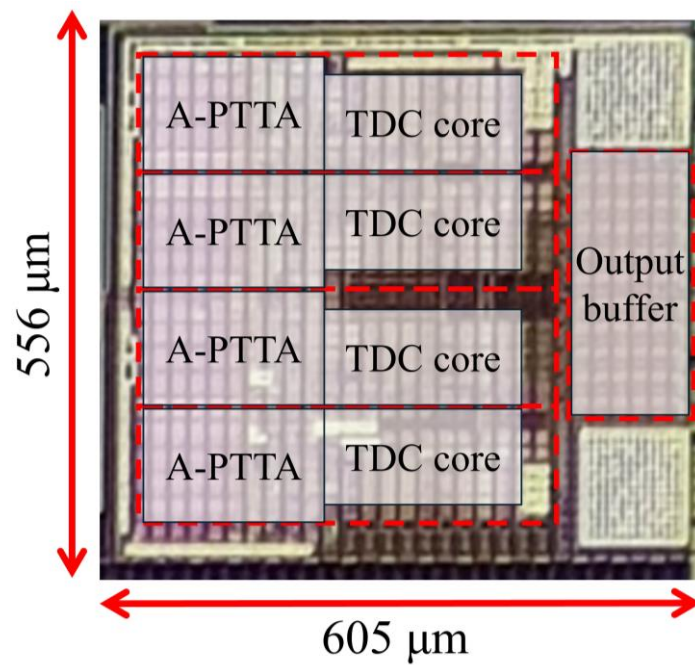


Fig. 5. 10. Die photograph of fabricated chip.

5.3 Chip Implementation Details

Figure 5.10 presents the layout of a two-step radiation-hardened adaptive TDC fabricated using a standard 180 nm CMOS process. The chip comprises four core TDCs and is designed with dimensions of $556 \times 605 \mu\text{m}^2$. For power distribution, a power mesh structure was implemented to ensure a stable and reliable voltage supply.

5.4 Simulation Results

The proposed circuit was verified through simulations conducted using electronic design automation (EDA). Fig. 5.11 shows the output when the input signal of the proposed PTТА is swept from 0 to 5 ns at 10 ps intervals. The simulation results indicate a slope of 3.0026, demonstrating very high linearity. Fig. 5.12 illustrates the output of the TA when time differences of 1 ns and 3 ns are applied both conventional and proposed. In all of TA cases, a biased pulse width of 480 ps was observed at the output. The simulation results show that when an input time difference of 1 ns is applied, the conventional PTТА takes a total of 13.55 ns to complete the output of three pulses, whereas the proposed PTТА achieves this in 7.785 ns, resulting in an improvement of approximately 43%. Additionally, with an input time difference of 3 ns, the conventional PTТА takes 15.55 ns, while the proposed PTТА takes 12.8 ns, resulting in an 18% improvement. This indicates that the off-state time of the proposed PTТА was effectively controlled, enabling faster operation and mitigating skew errors caused by leakage current. Especially, it was found to be more

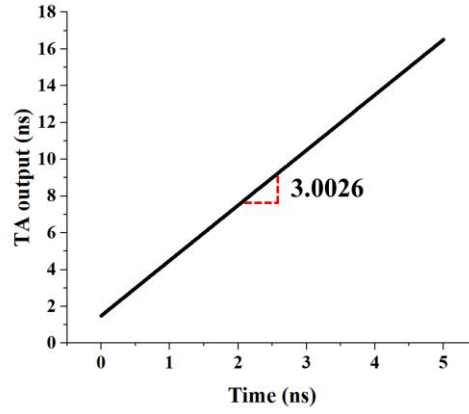


Fig. 5. 11. Graph of output versus input time for a TA with a gain of 3.

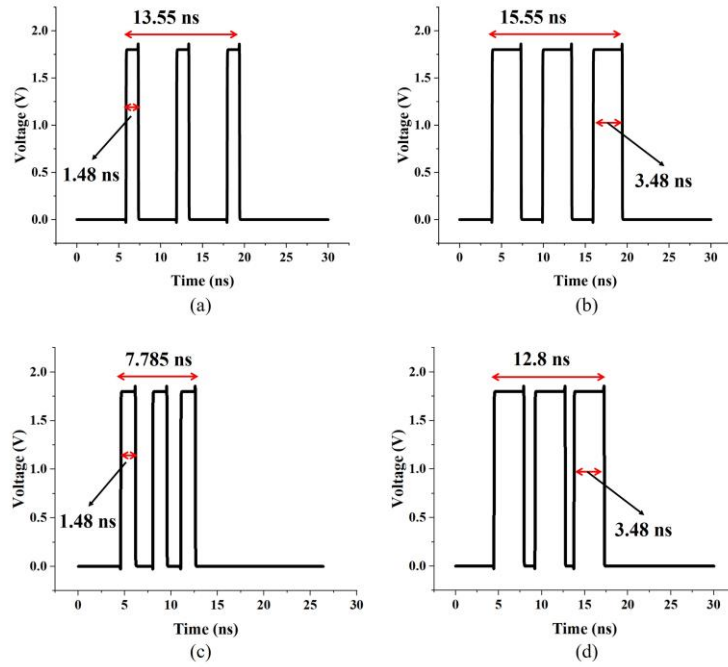


Fig. 5. 12. Comparison of input time differences of 1 ns and 3 ns for both conventional and proposed time amplifiers. For the conventional time amplifier, input time difference of 1 ns requires 13.55 ns to amplify the input time (a), whereas input time difference of 3 ns requires 15.55 ns (b). In comparison, the proposed time amplifier takes 7.785 ns (c) and 12.8 ns (d), respectively. Thus, improvements of approximately 43% and 18% are achieved in each case.

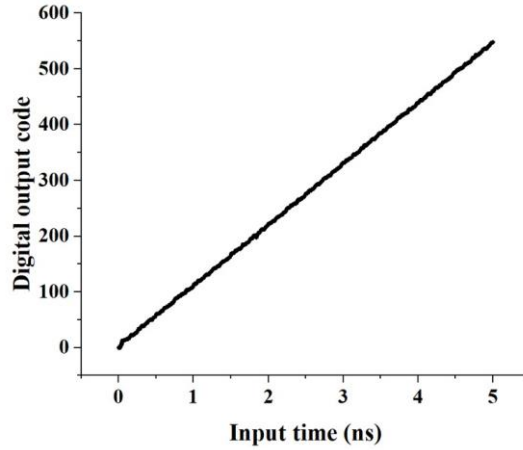


Fig. 5. 13. Graph of 9-bit TDC output as a function of input time.

effective when the input time difference was shorter.

Fig. 5.13 presents the simulation verification results of the 9-bit radiation-hardened TDC with a dynamic range of 5 ns and a maximum operating frequency of 200 MHz. The simulations were performed after extracting parasitic components. Fig. 5.14 and Fig. 5.15 show the INL and DNL curves, respectively. When used as a 7.5-bit TDC, the LSB was 27.3 ps, with DNL measured at [-0.37, 1.63] LSB and INL at [-0.75, 2.55] LSB as shown in Fig. 5.14. For the 9-bit TDC configuration, the LSB was 9.1 ps. Simulation results showed that the DNL was [-4.1, 5.9] LSB, and the INL was [-4.2, 7.5] LSB as depicted in Fig. 5.15. Therefore, a trade-off between linearity and resolution was observed. This trade-off arises due to the accumulation of skew errors during the off-state time of TA and kickback noise resulting from switching operations, which increases as the number of TDC stages increases.

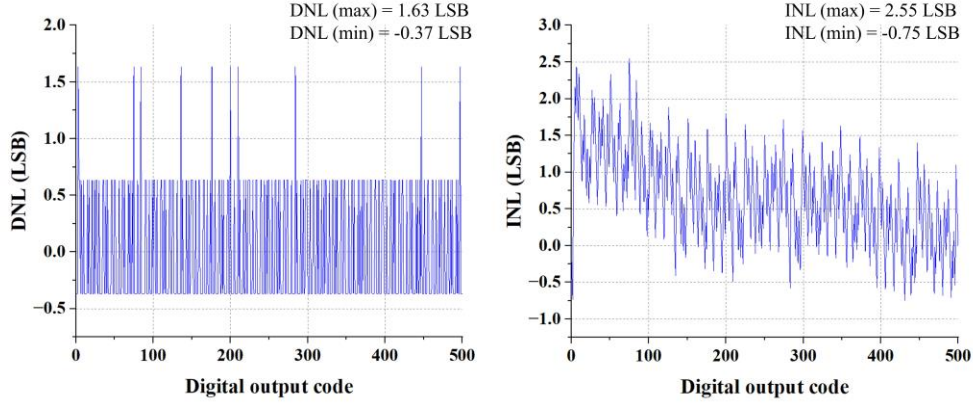


Fig. 5. 14. DNL and INL graphs for the 7.5-bit TDC configuration. The DNL is measured between -0.37 and 1.63 LSB, while the INL is measured between -0.75 and 2.55 LSB.

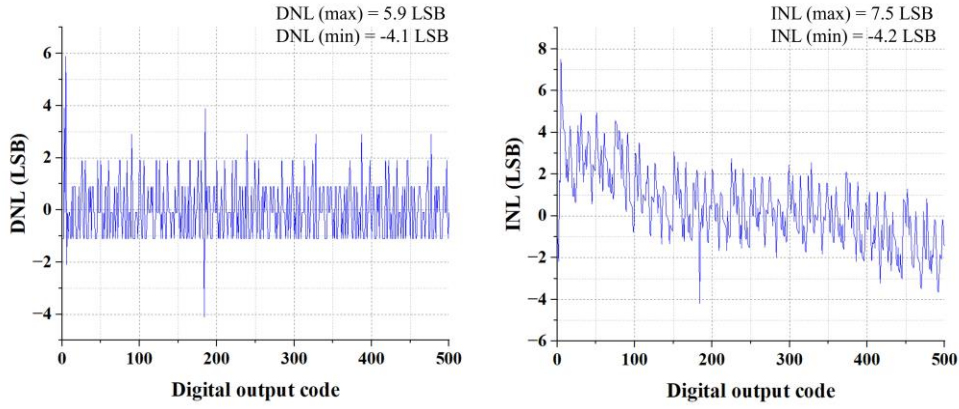


Fig. 5. 15. DNL and INL graphs for the 9-bit TDC configuration. The DNL is measured between -4.1 and 5.9 LSB, while the INL is measured between -4.2 and 7.5 LSB.

To evaluate the radiation tolerance of the proposed RHBD TDC, simulations were performed using a simplified TID model, as illustrated in Figure 5.16. The proposed TDC architecture exhibits significant linearity degradation due to skew errors induced by leakage currents. To address this issue, ideal current sources were connected to the NMOS transistors to mimic a leakage current path. The leakage current was set to increase

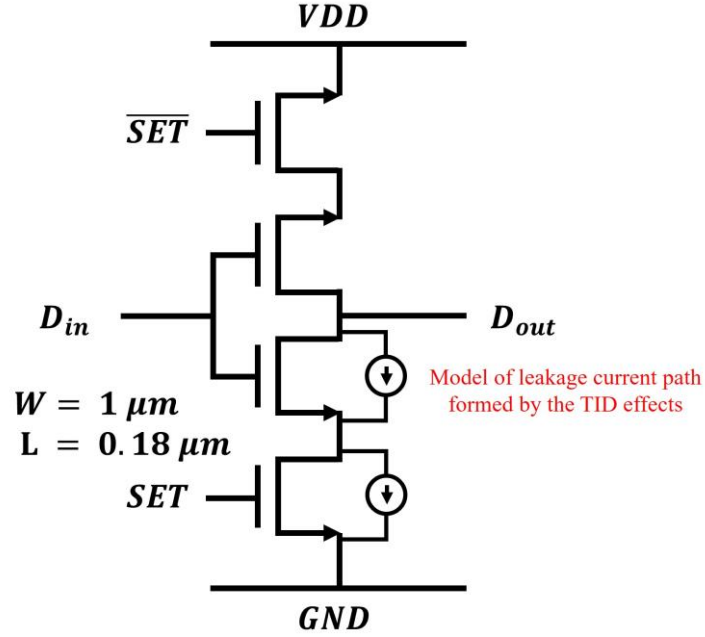


Fig. 5. 16. Schematic of leakage current model. Ideal current source is connected between the source and drain of the NMOS transistor, establishing leakage current path. Leakage current increases linearly with the number of NMOS fingers. Each unit NMOS transistor is configured with W/L ratio of 1/0.18.

linearly with the number of NMOS fingers. Thus, the current source was configured to supply 1 μA per unit NMOS transistor. Each unit NMOS transistor has a width-to-length (W/L) ratio of 1/0.18. This method enables a preliminary evaluation of the performance differences between circuits utilizing the proposed PTTA and conventional designs in terms of linearity.

As illustrated in Fig. 5.17, the conventional TDC exhibits a significant degradation in output code linearity compared to the proposed radiation-hardened TDC. This degradation in linearity is observed as depicted in Fig. 5.18, where the counter capturing the rising edge is ideally expected to count two times. However, due to leakage currents,

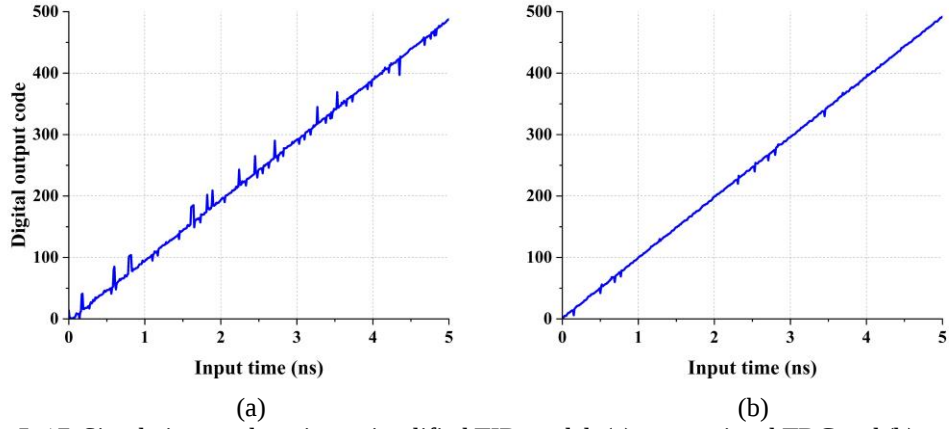


Fig. 5.17. Simulation results using a simplified TID model: (a) conventional TDC and (b) proposed RHBD TDC.

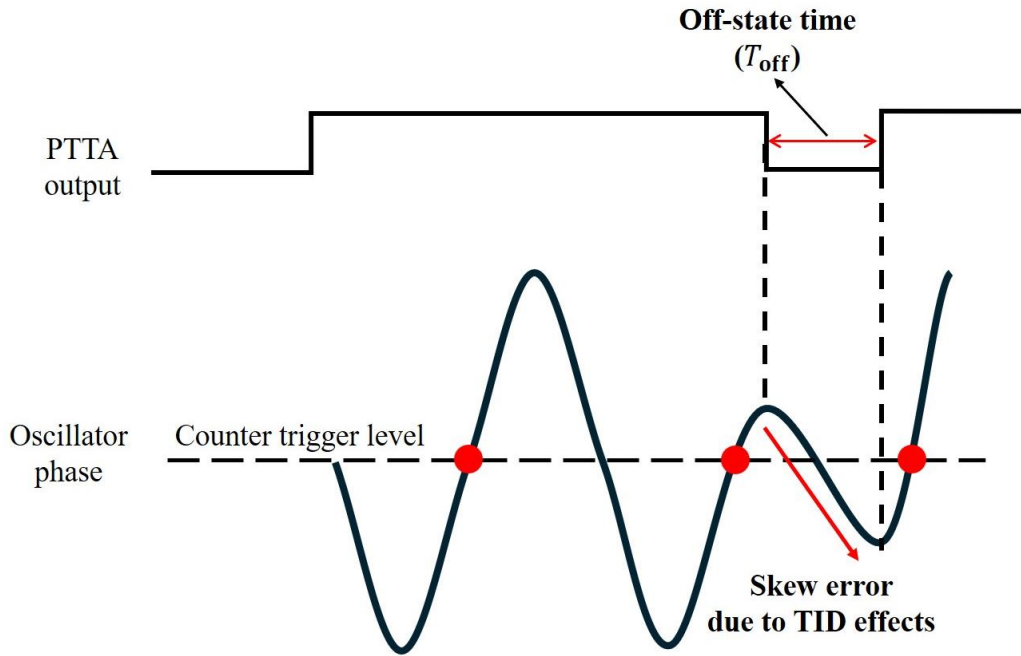


Fig. 5.18. Timing diagram of gated ring oscillator in conventional TDC with PTTA. Long off-state time can lead to skew error.

the counter erroneously triggers three times, resulting in output codes that exceed the

intended values. This indicates that radiation-induced TID effects can significantly affect the reliability of conventional TDCs. In contrast, although a degradation in the linearity of the proposed radiation-hardened TDC is observed, its impact is minimized compared to conventional TDCs.

Fig. 5.19 illustrates the INL and DNL curves of both TDCs. The DNL and INL for the conventional TDC are presented in Fig. 5.19 (a) and (b), with measured values showing a DNL range of $[-37, 29]$ LSB and an INL range of $[-30, 26]$ LSB. In contrast, the proposed RHBD TDC exhibited a DNL range of $[-9, 13]$ LSB and an INL range of $[-8.8, 5.6]$ LSB, as depicted in Fig. 5.19 (c) and (d). These results indicate that the proposed RHBD TDC achieves significantly improved linearity compared to the conventional TDC, with a 67% reduction in DNL_{p-p} and a 74% reduction in INL_{p-p} under radiation conditions. Therefore, this approach can effectively mitigate leakage-induced skew errors, ensuring more stable performance.

Table 5.2 compares the proposed TDC with other TDCs used in various applications. The TDC presented in this dissertation is designed for use in extreme radiation environments, with a target application focused on medical imaging. [178] first introduced the PTTA and developed a two-step TDC architecture for an All-Digital Phase Locked Loop (ADPLL). [159], [179], and [180] focus on TDCs used in medical imaging, and when compared to these designs, the proposed TDC achieves an improvement in resolution, enabling more accurate coincidence timing information. Although a trade-off in linearity is observed, the 7.5-bit proposed TDC retains comparable linearity performance. [167]

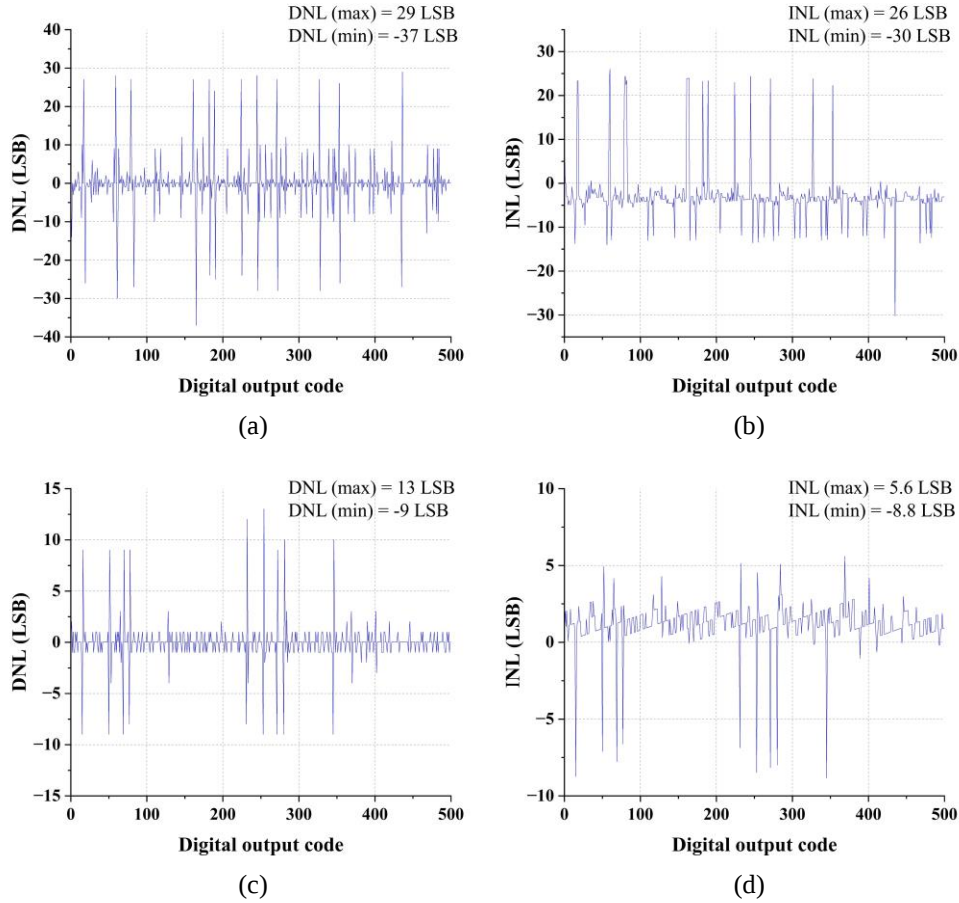


Fig. 5. 19. DNL and INL graphs for the conventional and proposed TDCs using the simplified TID model. For the conventional TDC, the DNL is measured between -37 and 29 LSB (a), while the INL is measured between -30 and 26 LSB (b). For the proposed RHBD TDC, the DNL is measured between -9 and 13 LSB (c), and the INL is measured between -8.8 and 5.6 LSB (d).

presents a radiation-hardened TDC designed for extreme radiation environments, specifically to meet the requirements of ITER, including exposure to radiation doses up to 5 MGy. The study showed continued operation with only a 1-bit reduction in Effective Number of Bits (ENOB). This robustness is attributed to the use of a relaxation oscillator instead of a ring oscillator, which provides better radiation stability. The observed 1 bit

Table 5. 2
COMPARISON RESULTS OF PROPOSED TDC

	This work	JSSC'13 [178]	JSSC' 14 [159]	JSSC'19 [179]	JSSC' 20 [180]	TNS' 12 [167]
Architecture	Two-step Pipeline	Two-step	GRO	GRO	VDL	Sigma-delta
Radiation Hardening	O	X	X	X	X	O
Technology (nm)	180	65	130	40	350	130
Fs (MS/s)	12.5	200	5	N/A	10	5 – 50
Bits (bit)	7.5 / 9	7	12	12	7	11
Resolution (ps)	27.3 (7.5 b) / 9.1 (9 b)	3.75	64.5	33 – 120	78	6
DNL (LSB)	1.63 (7.5 b) / 5.9 (9 b)	0.9	0.81	0.5	0.04	N/A
INL (LSB)	2.55 (7.5 b) / 7.5 (9 b)	2.3	3.9	3.5	0.58	N/A

degradation is likely due to a decrease in the relaxation oscillator's frequency under radiation exposure. Additionally, oversampling TDCs are not suitable for single-shot applications such as medical imaging applications.

5.5 Conclusion

In this chapter, I presented the TDC architecture utilizing a time amplifier that can be used in various radiation environments. The demand for time-based detectors across different radiation industries has been growing, prompting ongoing research into enhancing the radiation-hardening performance of TDCs, such as in space, nuclear power plants, high-energy particle physics, and medical imaging applications. The TDC proposed in this

dissertation was designed specifically for medical applications, featuring an advanced pulse-train time amplifier to address the skew error issues found in conventional pulse-train time amplifiers. The proposed rad-hard adaptive TDC was designed using a four-stage, two-step pipeline architecture, allowing input data to be measured with resolutions of 27.3 ps and 9.1 ps.

To verify the operation of the designed circuit under radiation environments, simulations were performed using a simplified TID model. Simulation results showed improvements of 67% in DNL_{p-p} and 74% in INL_{p-p} compared to the baseline TDC. The results showed significant improvements in linearity compared to the baseline TDC. Future work will include validation experiments in real radiation environments.

CHAPTER 6

Conclusion

With the discovery of radiation in 1896, radiation application technologies have become integral to various aspects of human life, extending beyond particle accelerators, nuclear power plants, and nuclear fusion reactors to encompass medical imaging, cancer treatment, the space industry, and military applications. In the 1960s, the effects of radiation on electronic components used in these applications were observed, prompting active research into radiation-hardened circuits. Since radiation can induce threshold voltage shifts and increase leakage currents in MOSFETs, Radiation-Hardened-by-Design (RHBD) techniques have become essential requirements to mitigate these adverse effects.

This dissertation begins with a brief background on the discovery of radiation and its impact on semiconductors. It then presents solutions to minimize the radiation effects on radiation detector circuit systems used in various environments.

Chapter 2 provides a concise history of radiation discovery and its effects, along with the background on how radiation impacts semiconductor devices.

Chapter 3 introduces a self-compensation technique for mitigating Total Ionizing Dose (TID) effects in Charge-Sensitive Amplifiers (CSAs) essential for general-purpose radiation detectors. This technique was successfully tested and helps detect and compensate for radiation-induced degradation in CSA outputs. Additionally, the RHBD CSA can be applied not only to radiation detectors but also to any sensor readout system that generates charge-based signals.

Chapter 4 addresses the pile-up phenomenon in CSAs used for measuring neutron flux in reactors by employing the Active Dead Time Control (ADTC) technique. This technique dynamically determines the reset period based on the input signal rate, enabling accurate radiation measurements in both high and low radiation fields. Through this research, neutron flux was successfully measured at the Transient Reactor Test (TREAT) facility at Idaho National Laboratory (INL).

Chapter 5 presents the research findings on radiation-hardening Time-to-Digital Converters (TDCs), which are key components in time-based signal detectors used in radiation environments. An advanced topology was proposed to address the skew error increase caused by radiation in the commonly used time amplifiers (TAs) in TDCs. A 9-bit radiation-hard adaptive TDC was designed, achieving post-simulation results of Differential Non-Linearity (DNL) ranging from -0.5 LSB to +1.5 LSB and Integral Non-Linearity (INL) ranging from -1.8 LSB to +3.5 LSB. To verify the TDC operation in a radiation environment, a simplified TID model was applied to the TDC. The verification results showed that the conventional TDC exhibited a DNL ranging from -37 LSB to +29 LSB and an INL ranging from -30 LSB to +26 LSB. In contrast, the proposed TDC shows a DNL ranging from -9 LSB to +13 LSB and an INL ranging from -8.8 LSB to +5.6 LSB, indicating higher hardness in radiation environments.

Future research will focus on integrating the radiation-hardening techniques presented in Chapter 3 with the ADTC technique from Chapter 4, aiming to compensate for performance degradation in high-radiation fields while enabling more stable self-

resetting through ADTC. Additionally, future efforts will explore the development of radiation-hardened analog-to-digital converters, digital-to-analog converters, and power management circuits, further advancing the capabilities of these integrated systems. This work will extend beyond the development of individual components to the integration of designed chips into cohesive systems for applications such as satellites, planetary orbit probes, high-energy physics laboratories, and nuclear power plants.

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ABSTRACT (In Korean)

방사선 계측 시스템에서 사용되는 적응형 내방사선 ASICs 설계 기법

최근 우주 탐사, 군사 시스템, 의료 영상, 원자력발전소, 입자 물리학 등 많은 응용 분야에서 집적회로 수요가 크게 증가하고 있다. 이러한 분야에서 사용되는 회로들은 방사선의 영향을 받아 성능 저하가 발생한다. 특히 방사선에 장기간 노출될 경우 Total Ionizing Dose (TID) effects 가 발생하면서 문턱전압 변화, 누설 전류 증가, 그리고 노이즈 증가 등의 문제가 발생할 수 있다. 본 학위논문에서는 세 가지 주요 연구를 통해 회로 설계 수준에서 TID 영향을 최소화하는 Radiation-Hardened-by-Design (RHBD) 기법을 제안한다.

먼저 범용성 방사선 계측기를 위한 RHBD 전치증폭기가 binary current source 를 사용해 설계되었다. 제안하는 전치증폭기는 TID effects 를 완화하기 위한 자가 보상 기술이 이용되었으며, 이를 통해 방사선에 의한 성능 저하를 감지하고 피드백 루프를 통해 보상할 수 있다. 이는 다양한 종류의 방사선 계측기에 사용되는 charge-sensitive 전치증폭기의 신뢰성을 향상시킬 수 있다.

두번째로, Micro-Pocket Fission Detector (MPFD)의 신호를 판독하는 시스템이 개발되었다. 원자로 내부에서 실시간 중성자 속을 측정하기 위해 사용되는 MPFD 가 개발되었다. MPFD 의 빠른 신호로 인해 pile-up 현상이 발생하면서 전치증폭기가 포화되는 문제가 발생하므로, 자가 초기화를 위한 Active Dead Time Control (ADTC) 기법이 도입되었다. 이 기법은 입력되는 signal rate 에 따라서 초기화되는 주기를 능동적으로 조정함으로써, 높은 방사선

환경이든 낮은 방사선 환경이든 정확한 방사선 측정이 가능하도록 한다. 이 기술은 Idaho National Laboratory 의 Transient Reactor Test (TREAT) 시설에서 성공적으로 검증되었다.

마지막으로, RHBD 시간-디지털 변환기가 소개된다. Two-step 구조를 기반으로 한 적응형 시간-디지털 변환기가 표준 180 nm CMOS 공정을 활용해 설계되었다. Pulse train time amplifier 의 방사선 영향으로 인한 skew error 증가를 완화하기 위해 능동적으로 주기를 조정하는 advanced pulse train time amplifier 가 제안되었다. 이를 이용하여 시간-디지털 변환기가 개발되었으며, 전체 시스템의 검증이 시뮬레이션을 통해 이루어졌다. 방사선 영향 검증을 위해 간소화된 TID 모델이 사용되었다. 검증 결과 선형성 측면에서 최대 74 % 개선된 것으로 조사되었다.

본 연구에서 제안된 다양한 RHBD 기법들은 방사선 환경에서 발생하는 TID 효과를 효율적으로 완화하여 극한 환경에서도 안정적인 회로 동작이 가능함을 보여준다. 이러한 설계 기술은 우주, 군사, 의료, 원자력 등 높은 방사선이 존재하는 분야에서 적용될 수 있으며, 이를 통해 다양한 응용 시스템에서 요구되는 회로의 신뢰성과 안정성을 크게 향상시킬 수 있을 것으로 기대된다.

Keywords : 내방사선 회로, 총 이온화 선량 효과, 단일 사건 효과, 전하 민감형 증폭기, 초소형 핵분열 계측기, 능동형 불감시간 조절, 시간-디지털 변환기