Integrated Silicon Photonic Transmitters with Simultaneous Thermal and Linearity Calibration

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A Dissertation
Submitted to the Department of Electrical and Electronic Engineering and the Committee on Graduate School of Yonsei University in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy

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December 2025

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Abstract

Integrated Silicon Photonic Transmitters with Simultaneous Thermal and Linearity Calibration

This dissertation presents the design and experimental demonstration of integrated silicon photonic transmitters that enable scalable optical input and output for next-generation high-performance computing and artificial intelligence systems. The proposed architectures address the fundamental thermal instability and nonlinear transfer characteristics of micro-ring modulators (MRMs), which are among the primary challenges in achieving energy-efficient and high-speed optical interconnects.

The first prototype implements a 32-Gb/s single-channel silicon MRM transmitter with an on-chip code-based temperature calibration and locking algorithm. The controller identifies the heater bias that maximizes optical modulation amplitude and maintains this point through a low-bandwidth dithering feedback loop. By employing DC-balanced calibration codes and low-speed optical monitoring, the system achieves autonomous resonance alignment without external digital signal processing or optical feedback circuits. Experimental results verify stable operation across ambient temperature variations from 20 °C to 30 °C while maintaining open eye diagrams and consistent optical output power.

Building on this foundation, the second prototype extends the concept to a 224-Gb/s four-channel wavelength-division-multiplexed transmitter employing PAM-4 signaling. A dual-objective calibration algorithm is introduced to simultaneously optimize optical modulation amplitude and relative-level mismatch by coordinating thermal tuning in the

photonic domain and digital weighting in the electronic driver. The integrated controller achieves balanced PAM-4 eye openings and robust thermal locking across all wavelength channels, demonstrating scalability and repeatability in multi-channel operation.

While the demonstrated systems achieve competitive energy efficiency and stable operation, the work also identifies hardware-level bottlenecks that limit further performance scaling. The low modulation efficiency of current MRMs requires the driver to generate nearly full-swing output voltage, which increases capacitive loading and constrains the overall electrical bandwidth, thereby becoming a bottleneck to developing even higher data rates. Future research directions include improving MRM modulation efficiency, developing high-speed driver circuits capable of operating beyond nominal voltage, and enhancing heater efficiency and calibration speed through digitized feedback architectures.

The results of this dissertation establish a practical and scalable framework for self-calibrating silicon photonic transmitters that integrate thermal stability, linearity control, and wavelength management within a unified on-chip system. These techniques provide a foundation for future co-packaged optical I/O solutions capable of meeting the bandwidth, energy, and reliability requirements of next-generation computing platforms.

Keywords: silicon (Si) photonics, micro-ring modulator (MRM), optical transmitter, source-series termination (SST), thermal calibration, PAM-4 signaling, wavelength-division multiplexing (WDM), optical interconnect, high-speed driver, high-performance computing (HPC), artificial intelligence (AI) systems.

CHAPTER 1 Introduction

1.1 MOTIVATION

In recent years, the rapid expansion of artificial intelligence (AI), high-performance computing (HPC), and cloud-scale data analytics has driven an unprecedented surge in data throughput requirements. Modern computing systems, particularly those deploying large-scale AI models, demand not only vast computational resources but also immense data movement capabilities. This has exposed fundamental limitations in current interconnect technologies, both at the chip and system levels.

1.1.1 Bandwidth Bottlenecks and Insertion Loss Scaling

As system bandwidth targets have escalated beyond 100 Gb/s per lane, traditional electrical interconnects are approaching their physical limits. In copper-based links, insertion loss increases rapidly with distance and frequency, making high-speed transmission over long distances increasingly impractical.

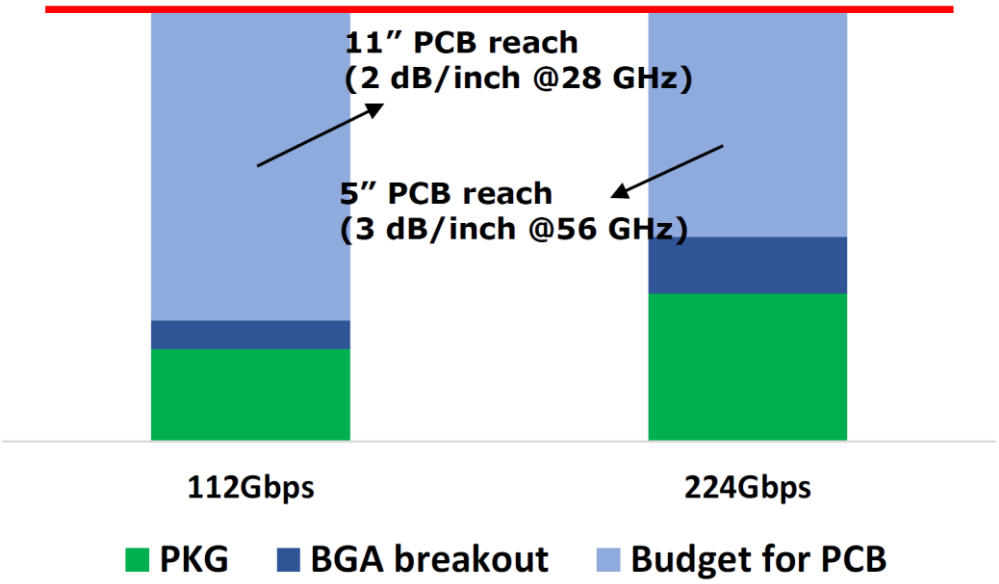


Fig. 1-1. 30 dB chip-to-chip loss budget [1]

As illustrated in Fig. 1-1, a channel operating at 112 Gb/s (28 GHz) may tolerate up to 11 inches of PCB trace assuming 2 dB/inch attenuation, while a 224 Gb/s (56 GHz) channel is limited to just 5 inches due to increased loss of approximately 3 dB/inch. [1] This sharply reduced reach highlights how even moderate distances on a PCB can exceed the insertion loss budget, necessitating aggressive equalization or signal regeneration.

These constraints are especially problematic in hyperscale data centers, where rack-to-rack and switch-to-server links often span multiple meters. To preserve signal integrity under such conditions, systems must rely on power-hungry digital signal processing (DSP) for equalization and forward error correction (FEC). As a result, the power consumption and thermal footprint of electrical I/O scale disproportionately with bandwidth, undermining the energy efficiency and scalability of next-generation networked systems.

1.1.2 Interconnect Latency Challenges in Large-Scale AI Systems

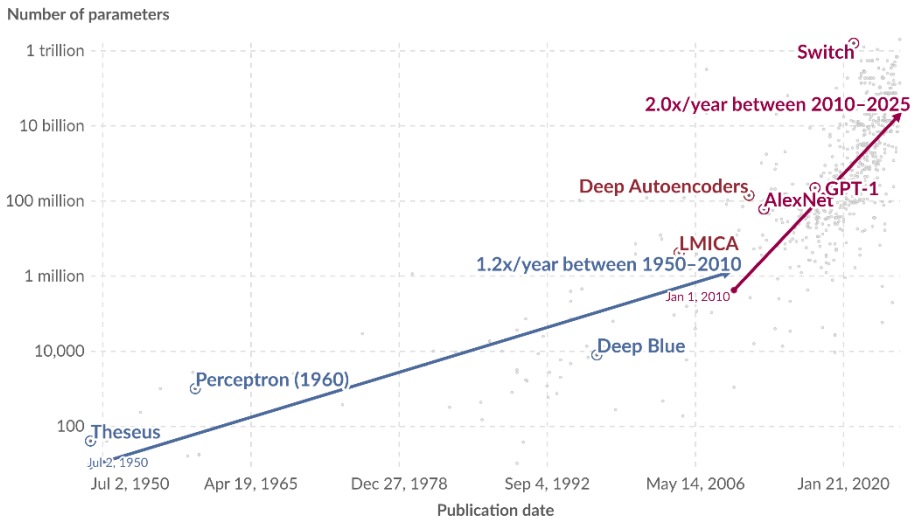


Fig. 1-2. Exponential growth of parameters in notable AI systems [2]

As shown in Fig. 1-2, the number of parameters in state-of-the-art AI models has been growing exponentially, approximately doubling each year since 2010. This rapid growth has resulted in unprecedented computational demands and a corresponding increase in data movement between devices during both training and inference. As a consequence, interconnect performance has become a key bottleneck, not only in terms of bandwidth but also in terms of latency.

In latency-sensitive workloads such as large-scale AI model training and HPC, the cost of excessive signal conditioning, including channel equalization and FEC, can outweigh its benefits. DSP blocks used for these purposes can introduce multi-nanosecond delays, which accumulate across multi-hop networks topologies and degrade end-to-end

performance.

Moreover, modern AI models are often too large to fit within a single accelerator and must therefore be trained in parallel across multiple devices. As a result, inter-device communication becomes a major bottleneck. According to [3], interconnect overhead could account for as much as 40 to 75 percent of total runtime in future training workloads. Inference tasks are similarly impacted, as frequent data transfers between compute and memory units lead to increased latency and energy consumption. As noted in [4], deploying full-scale conversational AI services at the scale of a major search engine could require capital expenditures on the order of $100 billion, driven largely by interconnect infrastructure.

1.1.3 Silicon Photonics and the Rise of Optical Interconnects

To overcome these constraints, the industry is rapidly adopting optical interconnects based on silicon photonics. Optical links inherently offer superior bandwidth-distance products, lower loss, and better energy efficiency compared to copper. Silicon photonics enables dense integration of lasers, modulators, and photodetectors into CMOS-compatible platforms, allowing optical engines to be co-packaged with switch ASICs and network interfaces. A representative example of this trend is NVIDIA's adoption of silicon photonics in its next-generation data center switches, such as the Quantum-X and Spectrum-X series. These platforms incorporate micro-ring based optical transceivers co-packaged with the switch ASIC, aiming to reduce SerDes power consumption, eliminate the need for pluggable optics, and support higher port densities. This shift toward co-

packaged optics is motivated by the need to scale interconnect bandwidth while improving overall system energy efficiency and reliability.

While CPO is currently being applied to network switches, research into extending optical interconnects to chiplet and intra-package domains is ongoing. As silicon photonics matures in reliability and integration, its role in solving both long-reach and short-reach I/O bottlenecks is expected to grow. Ultimately, optical communication offers a path to decouple bandwidth scaling from the physical and thermal constraints of electrical links.

1.1.4 Challenges in Silicon Photonic Interconnects

However, despite these advantages, silicon photonics also exhibits certain limitations compared with conventional electronics. In particular, some wavelength-selective or resonant optical components are inherently more sensitive to temperature variations due to the thermo-optic effect of silicon, which can cause fluctuations in optical characteristics and performance drift over time. In addition, the nonlinear transfer characteristics observed in many optical modulators tend to reduce overall signal linearity, especially for multi-level modulation formats such as PAM-4 [5]–[8]. These factors necessitate additional on-chip calibration and control circuitry to maintain stable and linear operation, which is an important consideration for realizing practical large-scale optical interfaces [9]–[12].

1.2 RESEARCH SCOPE AND OBJECTIVES

This thesis aims to address the challenges outlined earlier by designing high-throughput optical interconnects that leverage advanced modulation and multiplexing techniques. The objective is to maximize per-fiber and per-channel data rates while ensuring signal integrity and energy efficiency. By exploring hybrid electrical-optical transmitter designs and photonic integration strategies, this work seeks to demonstrate practical architectures capable of sustaining the data throughput demands of next-generation computing systems.

The rest of this thesis is organized as follows: Chapter 2 provides background on silicon photonic devices, transmitter architectures, and thermal control techniques. Chapter 3 presents the design and evaluation of a 1-channel optical transmitter integrating CMOS drivers and MRM. Chapter 4 extends the architecture to a 4-channel WDM system with thermal and linearity calibration. Chapter 5 concludes the dissertation and discusses directions for future research.

CHAPTER 2 Background

This chapter reviews the building blocks relevant to a high-throughput, pin-efficient silicon-photonics transmitter. Section 2.1 surveys the three modulators most commonly used in silicon photonics: Mach–Zehnder, electro-absorption, and micro-ring. Section 2.2 summarizes driver architectures and what they imply for level accuracy and bandwidth. Section 2.3 collects signaling facts that are specific to NRZ and PAM-4. Section 2.4 explains why micro-ring nonlinearity and bias sensitivity matter in practice. Section 2.5 describes heater-based bias acquisition and lock algorithms that make rings practical. Section 2.6 discusses WDM scaling, channel spacing, and stability.

2.1 PHOTONIC MODULATORS: FUNDAMENTALS AND COMPARATIVE PERSPECTIVE

In optical fiber links the carrier can be driven by direct modulation or by external modulation: direct modulation varies the laser injection current so that the output power follows the laser rate dynamics, while external modulation keeps a continuous-wave source stable and imprints data in a separate device. Direct modulation is economical for short reach, but the usable bandwidth is set by the relaxation resonance and parasitic, the generated chirp interacts with fiber dispersion, and efficient on-silicon lasers are still difficult to integrate at high yield. External modulation separates roles: the laser supplies stable optical power, the modulator and driver supply electro-optic bandwidth, linearity,

and bias control. One laser or a comb can feed multiple modulators for wavelength-division multiplexing. For these reasons silicon-photonics transmitters generally adopt external modulators. Three device classes dominate practical silicon platforms: Mach–Zehnder modulators, electro-absorption modulators, and micro-ring modulators.

2.1.1 Mach-Zehnder modulators (MZMs)

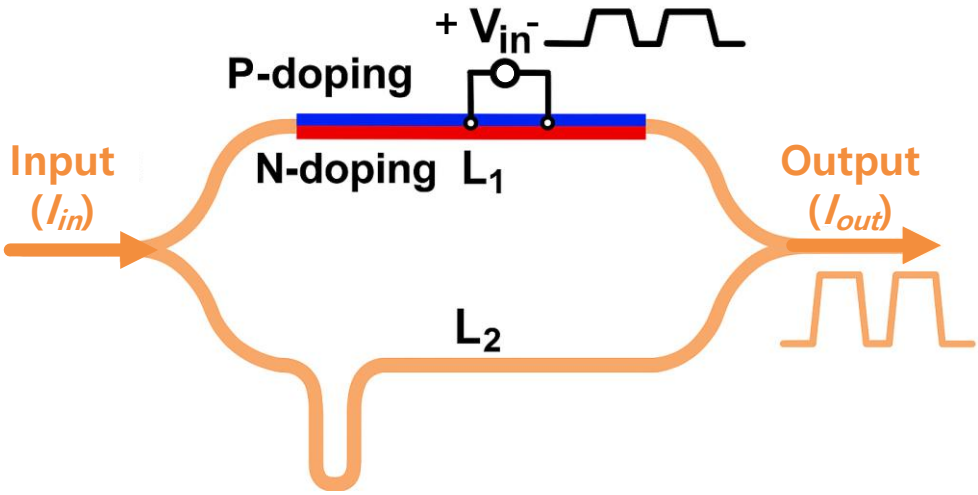


Fig. 2-1. Mach-Zehnder Modulator (MZM) conceptual layout

Fig. 2-1 shows a canonical silicon MZM. A splitter divides the input field into two arms, each arm carries an electrically driven depletion-type PN phase shifter, and a combiner converts phase difference into intensity at the output. The optical path is long

enough to accommodate electrodes and bends but otherwise simple. The strength of the MZM comes from its interferometric transfer: the optics are passive and do not need wavelength locking, yet a small electrical phase change causes a predictable intensity change at the combiner [13], [14].

The normalized intensity transfer is well approximated by a cosine-squared relation. Writing $\Delta\phi = \phi_1 - \phi_2$ for the arm phase difference and ϕ_b for a static bias with arm-loss imbalance captured by $0 < \rho \leq 1,$, the transmission can be written as:

$$T_{MZM}(V) = \frac{1}{2}[1 + \rho\cos(\Delta\phi(V) + \phi_b)] \tag{2.1}$$

which reduces to the familiar cosine-squared form when ρ=1\rho=1ρ=1. For push–pull drive we use the linear phase–voltage law

$$\Delta\phi(V) = \frac{\pi}{V_\pi}V \tag{2.2}$$

where V_π is the half-wave voltage of the phase shifter. Biasing near quadrature is standard: choose $\phi_b = \pi/2$ and define the origin of V so that $\Delta\phi(0) = 0$. Around that point the first two derivatives are

$$\left.\frac{dT}{dV}\right|_Q = \frac{\rho}{2}\frac{\pi}{V_\pi}, \qquad \left.\frac{d^2T}{dV^2}\right|_Q = 0 \tag{2.3}$$

which formalizes the broad quasi-linear region seen in Fig. 2-2: electrical steps map to nearly uniform optical steps and curvature is minimal. For two electrical levels V_H and V_L, the optical modulation amplitude is

$$\mathrm{OMA} = P_{\mathrm{in}}\left[T_{\mathrm{MZM}}(V_H) - T_{\mathrm{MZM}}(V_L)\right] \tag{2.4}$$

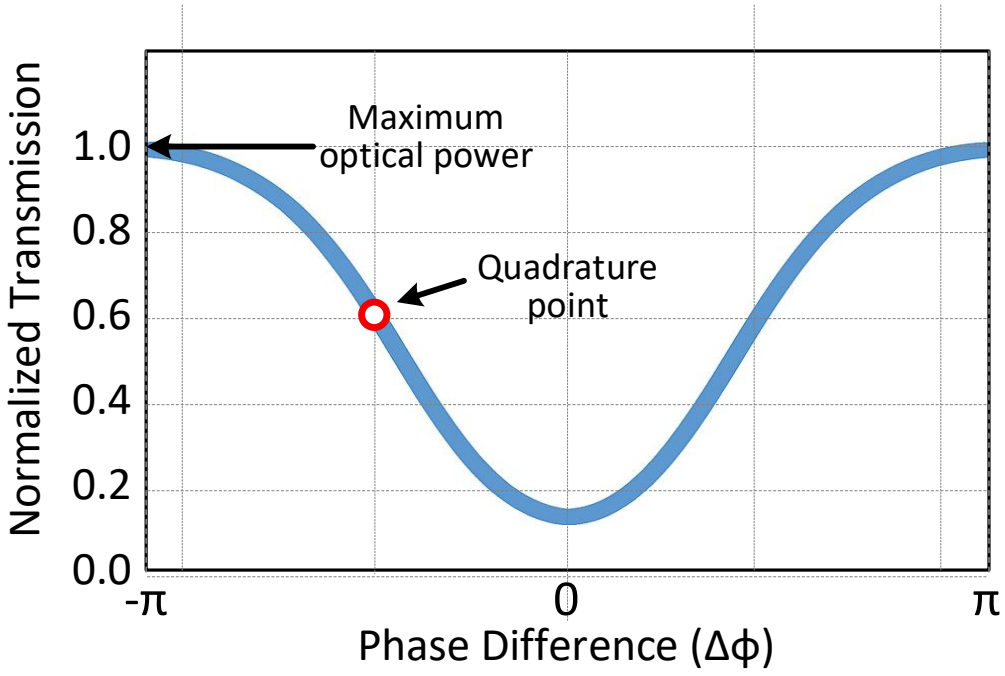


Fig. 2-2. MZM normalized transfer versus phase difference

and, for balanced arms, the extinction ratio expressed via ρ is

$$\mathrm{ER}_{\mathrm{dB}} = 10\log_{10}\left(\frac{1+\rho}{1-\rho}\right)^{2} \tag{2.5}$$

Electro-optic bandwidth is extended with traveling-wave electrodes by matching RF and optical velocities and by providing proper termination. In practice the baud-rate ceiling is then set by RF attenuation, velocity mismatch, and package parasitic rather than by the optical transfer near quadrature. Because an MZM has no intrinsic wavelength selectivity, WDM is realized with external multiplexers and demultiplexers. This keeps wavelength control simple but adds insertion loss and isolation requirements as channel count grows.

2.1.2 Electro-Absorption Modulators (EAMs)

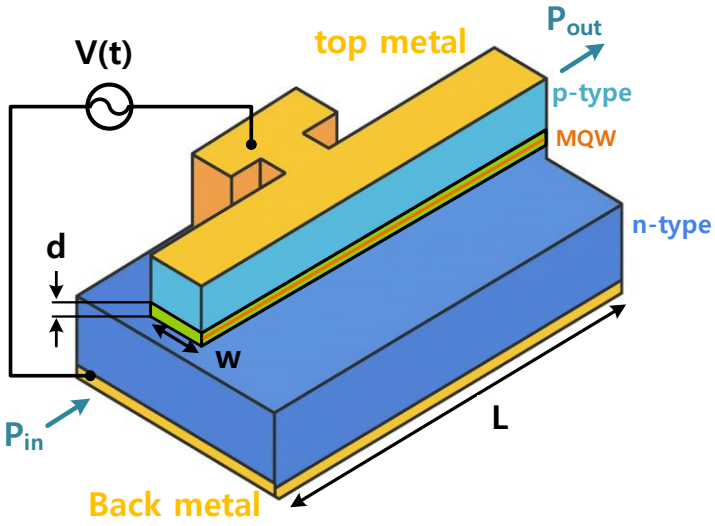


Fig. 2-3. Electro-Absorption Modulator (EAM) conceptual layout

Fig. 2-3 depicts a lumped EAM. The waveguide passes through an active absorption region contacted by top and bottom electrodes. In silicon photonics, germanium or GeSi quantum-well stacks enable operation in the O- or C-band through the Franz–Keldysh or quantum-confined Stark effect. The physical device is short and compact, routing is straightforward, and small-signal bandwidth is typically set by RC rather than by the intrinsic electro-absorption dynamics [16]–[19]. Transmission follows Beer–Lambert with a bias-dependent absorption coefficient:

$$T_{EAM}(V) = e^{-\alpha(V)L} = e^{-(\alpha_0 + \Delta\alpha(V))L} \tag{2.6}$$

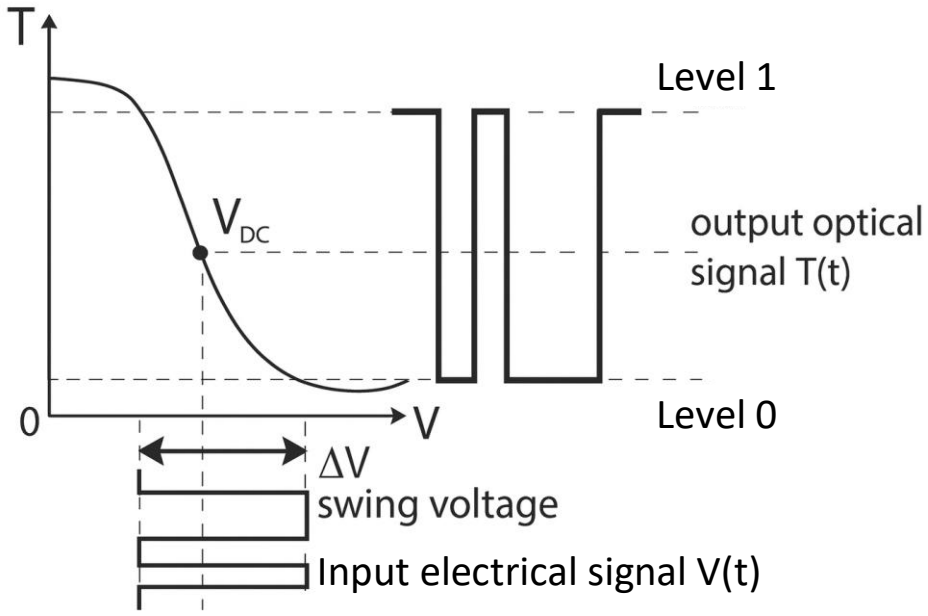


Fig. 2-4. Conceptual EAM transmission versus bias voltage

where L is the active length. Around an operating bias V_0 the slope and curvature are

$$\left.\frac{\partial T}{\partial V}\right|_{V_0} = -L\alpha_V' T_{\mathrm{EAM}}(V_0), \qquad \left.\frac{\partial^2 T}{\partial V^2}\right|_{V_0} = T_{\mathrm{EAM}}(V_0)\left[(L\alpha_V')^2 - L\alpha_{VV}''\right] \tag{2.7}$$

with $\alpha_V' = d\alpha/dV$ and $\alpha_{VV}'' = d^2\alpha/dV^2$. Fig. 2-4 sketches the resulting transmission-versus-bias curve: a practical operating window exists where the voltage-to-transmission conversion is approximately linear. Outside that window the optical steps become uneven and the equalization burden rises. The optical modulation amplitude (OMA) between V_H and V_L reads

$$\mathrm{OMA} = P_{\mathrm{in}}[e^{-\alpha(V_H)L} - e^{-\alpha(V_L)L}], \tag{2.8}$$

and the small-signal bandwidth for lumped operation is

$$f_{3dB} \approx \frac{1}{2\pi R_{\text{eq}} C_{\text{tot}}}, \qquad C_{tot} \simeq \varepsilon \frac{A}{d} + C_{\text{pad}} + C_{\text{routing}}. \tag{2.9}$$

EAMs do not require resonance locking and can be driven simply, but the static insertion loss consumes link margin and the finite linearity window limits multi-level headroom. As with MZMs, WDM relies on external multiplexers whose loss stacks with modulator loss as channel count increases. The qualitative view is that EAMs are attractive when compactness and simple drive are paramount and when the link budget can tolerate static loss. Bias should be chosen so that the intended voltage swing remains inside the gentle part of the transmission curve, with periodic checks if temperature or material dispersion shift that window.

2.1.3 Micro-Ring Modulators (MRMs)

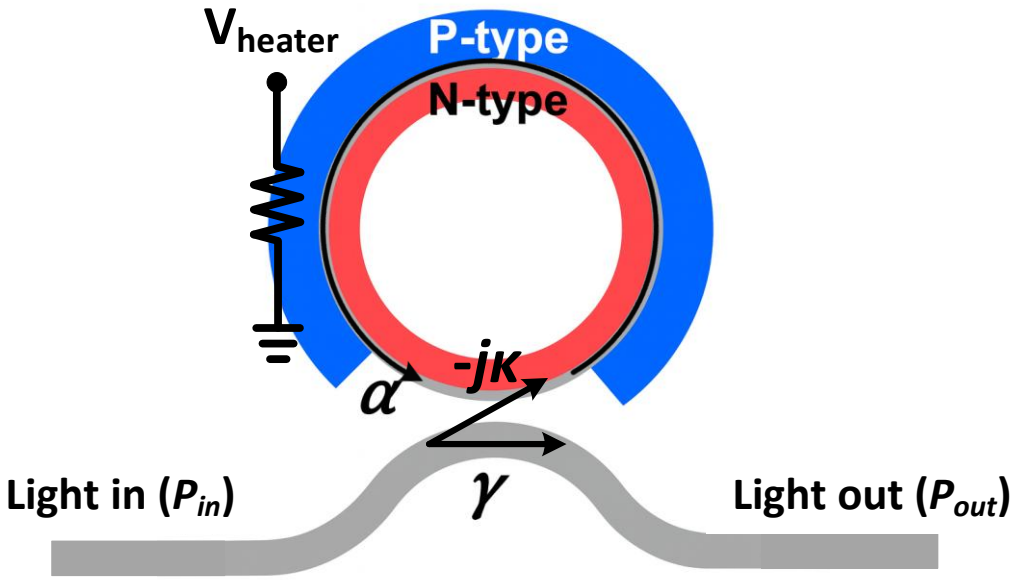


Fig. 2-5. Micro Ring Modulator (MRM) conceptual layout

Micro-ring modulators (MRMs) are widely used in silicon photonics for their compact size, low power consumption, and intrinsic compatibility with wavelength-division multiplexing. These modulators are based on optical resonance and offer highly efficient modulation within a small footprint.

Figure 2-5 shows the basic structure of an MRM. It consists of a ring-shaped waveguide side-coupled to a straight bus waveguide. An integrated heater is commonly included for coarse thermal tuning. The resonance condition is determined by the round-trip optical phase shift, given by

$$\theta = \beta L = \frac{\omega n_{eff} L}{c} \tag{2.10}$$

where L is the ring perimeter, n_{eff} is the effective refractive index, ω is the optical angular frequency, and c is the speed of light. The essential characteristics of a micro-ring modulator can be captured by a small set of parameters. The self-coupling and cross-coupling coefficients, r and κ, satisfy the energy conservation condition $r^2 + \kappa^2 = 1$. The intrinsic round-trip amplitude transmission is given by $a = e^{-\alpha_i L/2}$, where α_i is the waveguide loss coefficient. These first-order parameters are sufficient to describe the fundamental resonance behavior of the device, as demonstrated in earlier studies [20]–[23].

The complex optical transmission through the all-pass configuration of the MRM is described by

$$T_{through}(\omega) = \left| \frac{r - ae^{-j\theta}}{1 - rae^{-j\theta}} \right|^2 \tag{2.11}$$

As shown in Figure 2-6, the resonance manifests as a Lorentzian-shaped transmission dip. When the wavelength of the input light matches the resonance condition, strong optical interference occurs, and most of the light couples into the ring. This effect is used to modulate the output intensity by shifting the resonance with an applied voltage.

The tuning is typically achieved by embedding a PN junction in the ring waveguide. Applying a voltage changes the carrier concentration through the plasma dispersion effect, which in turn modifies the effective index and shifts the resonance wavelength. Modulation is performed near the slope of the resonance curve, where small voltage changes cause significant changes in transmitted optical power. This high sensitivity enables efficient binary modulation. In systems that employ multi-level formats such as PAM-4, however, more careful control is required. PAM-4 relies on four distinct optical levels, and any deviation from linearity in the transmission response can cause the level spacing to become

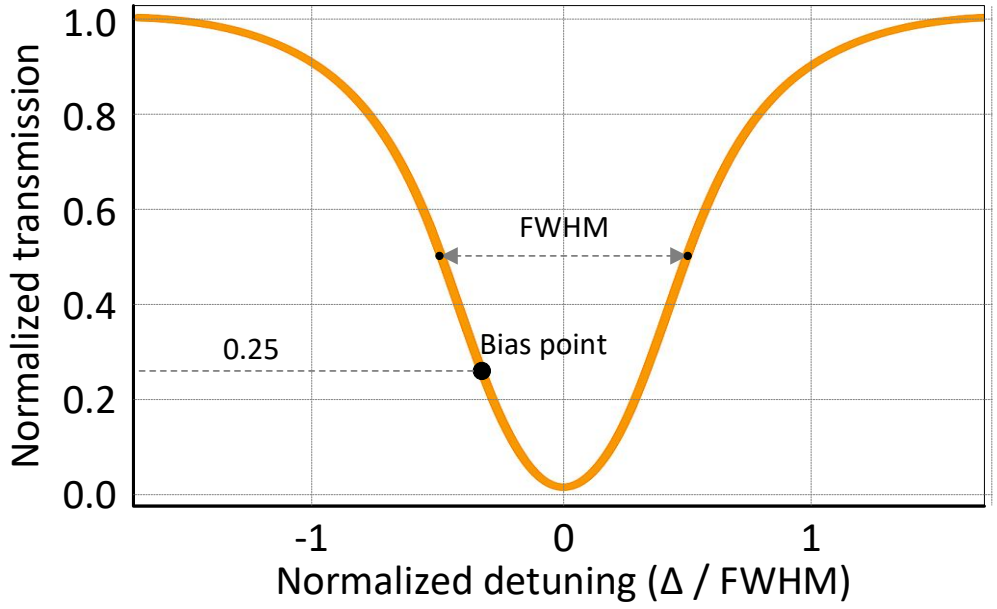


Fig. 2-6. MRM transmission versus normalized detuning.

uneven. This distortion, referred to as relative level mismatch, can degrade signal quality and reduce the noise margin. The curvature of the resonance curve is the primary source of this nonlinearity. If the modulation swing is too wide, it spans regions where the slope is no longer constant, resulting in unequal level steps.

To avoid this issue, the MRM must operate within a region of the resonance curve that is approximately linear. While higher-order mathematical models can quantify curvature-induced distortion, in most practical cases it is sufficient to limit the voltage swing and carefully bias the device. This ensures the modulated levels remain uniformly spaced, allowing PAM-4 and other multi-level signals to maintain their integrity.

Another important aspect of MRM operation is the coupling regime. At resonance, the through-port transmission simplifies to

$$T_{resonance} = \left| \frac{r - a}{1 - ra} \right|^2 \tag{2.12}$$

This expression shows how the balance between coupling and internal loss defines the device's extinction ratio and insertion loss. When $r = a$, the device is critically coupled and the transmission at resonance ideally drops to zero. This maximizes extinction and enables high-contrast modulation. If $r > a$, the ring is under-coupled, which results in higher insertion loss but lower extinction. Conversely, over-coupled rings with $r < a$ introduce phase distortions and reduce eye diagram clarity. The choice of coupling condition depends on system requirements and trade-offs between loss, modulation depth, and spectral shape. One practical challenge in using MRMs is their sensitivity to temperature. Because silicon has a strong thermo-optic coefficient, small variations in ambient temperature can shift the resonance wavelength by several picometers. This is enough to move the operating point away from the desired bias and degrade performance. To address this, most MRM-based systems include integrated heaters and thermal feedback control to stabilize the resonance. In some designs, closed-loop tracking circuits are used to maintain optimal biasing during operation.

In summary, micro-ring modulators provide a compact and efficient solution for optical modulation in integrated photonic systems. Their resonance-based behavior allows for precise control of the output signal, though it also introduces sensitivity to temperature and nonlinearity in certain operating regions. These limitations can be effectively managed through bias control, thermal tuning, and careful modulation design, enabling MRMs to serve as a core component in high-speed, high-density optical communication systems.

2.1.4 Summary

MZMs supply a broad quasi-linear transfer and simple biasing at the cost of area and drive energy. EAMs are compact and easy to drive but impose insertion loss and a finite linearity window that requires careful swing selection. MRMs are compact, efficient, and intrinsically wavelength-selective, so a single array naturally maps to many WDM channels. The remainder of this dissertation therefore adopts the micro-ring modulator as the primary device for achieving high aggregate rate and pin efficiency, and it addresses the associated bias acquisition, lock, and linearity management in the transmitter circuits and control algorithms that follow.

2.2 DRIVER ARCHITECTURES

High-speed silicon-photonics transmitters place the electrical driver in front of an optical device that appears either as a predominantly capacitive junction or as a distributed impedance-controlled line. The driver determines the available electrical swing, the usable electrical bandwidth into that load, and how accurately a weighted sum of input data slices forms the intended PAM-4 voltage levels at the modulator node. Those electrical levels then set the optical levels produced by the device. Because the systems of interest here use micro-ring modulators with PAM-4, the discussion focuses on drivers that interface with capacitive loads and compares voltage-mode and current-mode logic (CML) stages commonly used in broadband links.

2.2.1 Current-mode logic drivers

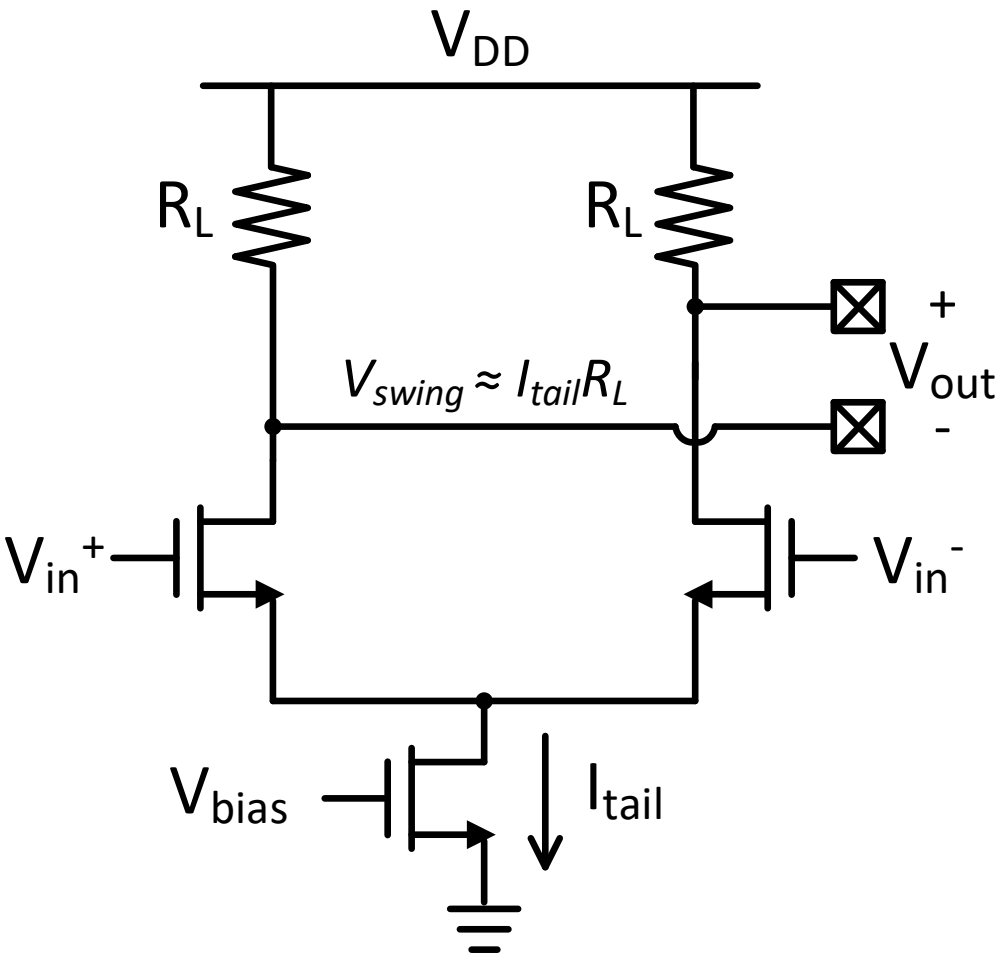


Fig. 2-7. Basic structure of current-mode logic drivers

Fig. 2-7 shows the canonical current-mode logic output stage used in high-speed transmitters. A differential pair steers an approximately constant tail current between two branches that terminate in resistive loads tied to V_{DD} . The differential inputs V_{in}^{+} and V_{in}^{-} control the transistors M1 and M2. The drains form the outputs V_{out}^{+} and V_{out}^{-} across R_L. A tail NMOS biased by V_{bias} sets the tail current I_{tail}. With this topology the single-ended voltage swing follows

$$V_{swing} \approx I_{tail} R_L \tag{2.13}$$

and the average output power is well approximated by

$$P_{avg} \approx V_{DD} I_{tail} \tag{2.14}$$

The upper electrical bandwidth is governed by the load resistance and the total capacitance at each output node. A first-order estimate is

$$f_{3dB} \approx \frac{1}{2\pi R_L C_{tot}} \tag{2.15}$$

This structure provides wide bandwidth, clean edges, and a controlled output impedance that mates naturally to 50-ohm environments and long electrical runs. These properties suit traveling-wave Mach–Zehnder modulators and board-level interconnects [24]–[27]. For micro-ring links the drawbacks are the swing bound set by voltage headroom at advanced nodes and the static power that follows from a nearly constant tail current [28].

2.2.2 Voltage-mode drivers with source-series termination

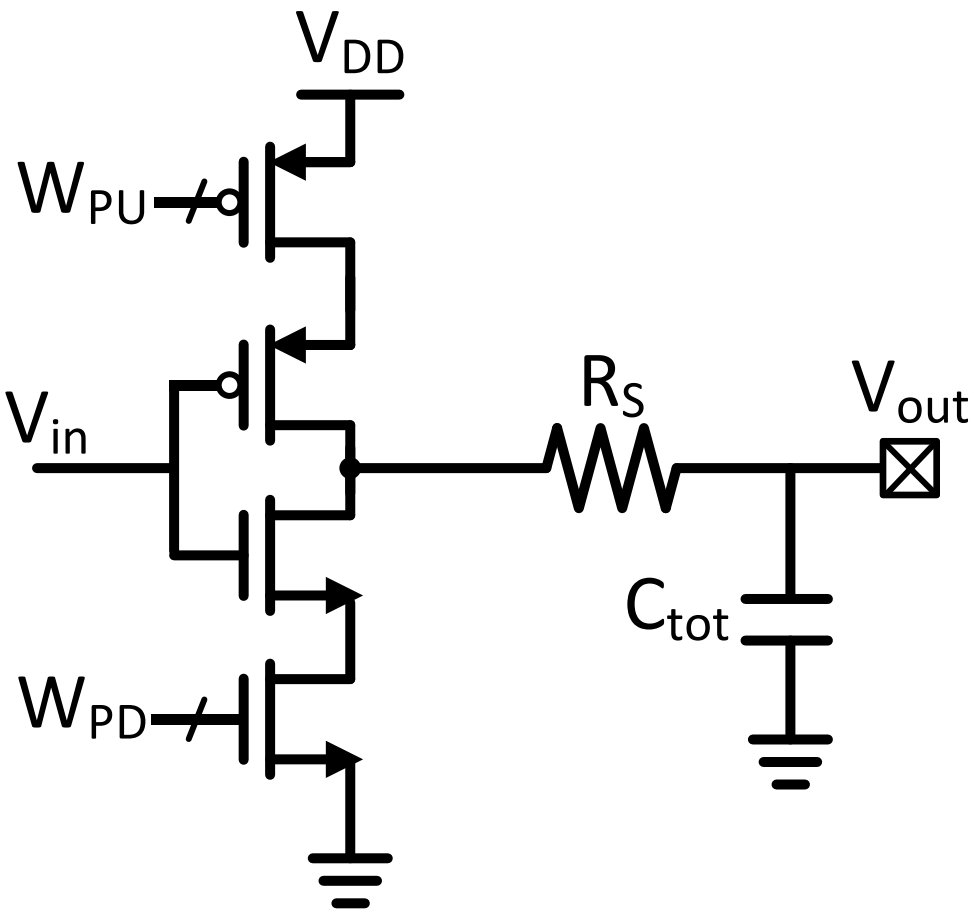


Fig. 2-8. Basic structure of voltage mode driver with source-series termination (SST)

Fig. 2-8 shows the source-series termination style used for capacitive silicon-

photonics modulators. A CMOS inverter drives the modulator node V_{out} through a defined series resistor R_S. The inverter output V_{drv} and R_S act as a Thevenin source into the electrical load C_{tot}, which includes the modulator junction and short local routing. The motivation for SST in PAM-4 with micro-ring modulators is twofold: it improves the accuracy with which the weighted sum of input slices produces the intended steady-state levels at the capacitive node, and it makes the small-signal bandwidth more uniform across levels [29]–[34].

Without series termination the bandwidth depends on the output level because the driver's effective source resistance changes with transistor operating region. Near the outer PAM-4 levels one device is in the linear region with a small on-resistance and the opposite device is off, so the incremental source resistance is low and edges are fast. Around the inner levels both devices conduct and operate closer to saturation. The small-signal output conductance adds as

$$g_{ds,tot}(V_{out}) = g_{ds,n}(V_{out}) + g_{ds,p}(V_{out}) \tag{2.16}$$

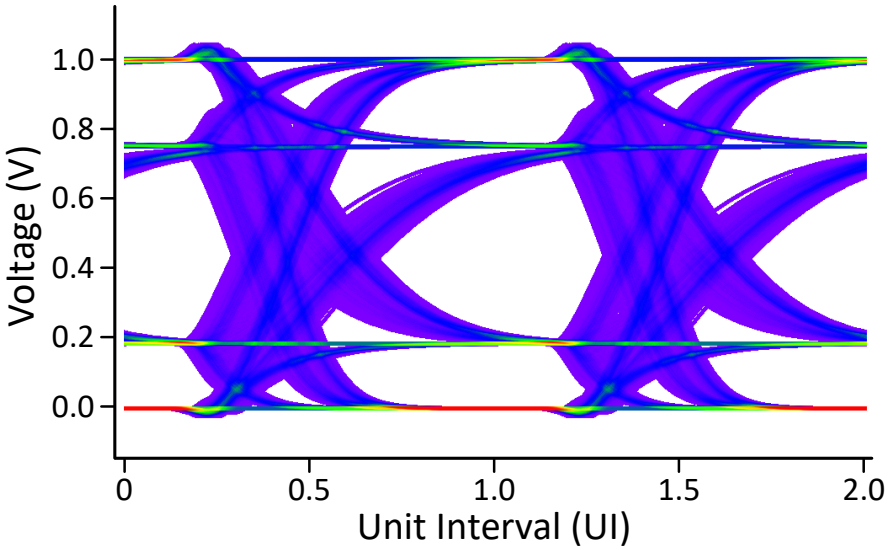
and the effective resistance

$$R_{out}(V_{out}) = \frac{1}{g_{ds,tot}(V_{out})} \tag{2.17}$$

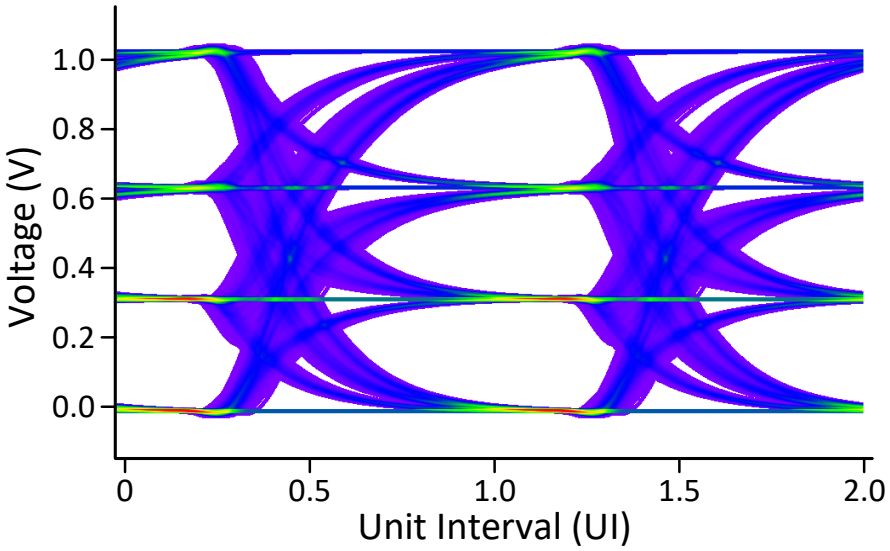
becomes larger near the mid-levels (level 1, level 2) than near the rails (level 0, level 3). The instantaneous time constant and bandwidth follow the Equation (2.27)

$$\tau(V_{out}) = R_{out}(V_{out})C_{tot}, \qquad f_{3dB}(V_{out}) = \frac{1}{2\pi\tau(V_{out})} \tag{2.18}$$

As a results, transitions that cross the inner decision thresholds spend more time near the mid-levels and the inner eyes compress even when the static level spacing is nominally correct.



(a)



(b)

Fig. 2-9. PAM-4 eye diagrams of a 10 GS/s voltage-mode ring driver: (a) without source-series resistor, (b) with source-series termination

With SST a defined series resistor R_S dominates the charging path during transitions. Most of the dynamic voltage drop appears across R_S, so the instantaneous V_{DS} of the MOS pair remains small and both transistors behave as on-resistances. The total output resistance is

$$R_{\text{out,tot}} = R_S + (R_{\text{on,n}} \parallel R_{\text{on,p}}) \tag{2.19}$$

which approaches R_S when $R_S \gg R_{\text{on,n}} \parallel R_{\text{on,p}}$. The capacitor current and transition law reduce to

$$i_C = C_{\text{tot}} \frac{dV_{\text{out}}}{dt} = \frac{V_{\text{drv}} - V_{\text{out}}}{R_S + (R_{\text{on,n}} \parallel R_{\text{on,p}})} \approx \frac{V_{\text{drv}} - V_{\text{out}}}{R_S} \tag{2.20}$$

and the time constant is nearly level-independent, $\tau \approx R_S C_{\text{tot}}$ and $f_{3dB} \approx 1/(2\pi R_S C_{\text{tot}})$. Fig. 2-9 contrasts the PAM-4 eye of a voltage-mode output driving a capacitive ring with and without a source-series resistor. Under the same 10-GS/s symbol rate and swing, Fig. 2-9(a) illustrates that without the series resistor, the effective source resistance becomes level-dependent, leading to slower mid-level transitions and compressed inner eyes.
Fig. 2-9(b) adds a series resistor that dominates the source impedance, so the transition time is set mainly by $R_S C_{\text{tot}}$ and is nearly independent of level. The crossings tighten and the inner and outer openings become more uniform, which reduces deterministic ISI and improves threshold placement and the level separation mismatch ration (RLM).

In an SST stage the series resistor and the MOS on-resistance form a divider during transitions. The device only sees a fraction of the total voltage swing, so when R_S is large compared with the composite on-resistance the instantaneous V_{DS} on the transistors stays small. The pull-up and pull-down devices then operate in the linear region and the effective source impedance during a transition is set mostly by R_S. The charging time constant is therefore almost independent of the PAM-4 level and bandwidth linearity improves. At

steady state the load is capacitive, so there is no dc drop across R_S. The final level is set by the weighted-sum code and the mapping is more reproducible because the source impedance is dominated by a known resistor rather than by device variation, which helps dc linearity at the sampling instant. The trade-off is controlled by the ratio of R_{on} to R_S. A larger R_S flattens level-to-level variation but reduces absolute bandwidth because the pole scales with $R_S C_{tot}$. Reducing R_{on} achieves the same linearity with less bandwidth penalty but requires upsizing the output devices, which increases gate and diffusion capacitances, raises predriver load and energy, and can add to C_{tot} through larger junctions and routing. In practice R_S is chosen large enough to suppress level dependence over PVT and the output devices are sized only as much as needed to meet swing and reliability limits.

2.2.3 Comparison of CML and VM-SST drivers

This section contrasts CML drivers and voltage-mode source-series-terminated (VM-SST) drivers for micro-ring PAM-4 links and explains the choice adopted in this work. From a load-matching perspective the two styles target different regimes. CML presents a controlled output impedance and delivers wide electrical bandwidth into transmission-line environments, which suits traveling-wave phase shifters and long electrical runs as in Fig. 2-1. A micro-ring modulator is instead a predominantly capacitive load located very close to the driver. In that case VM-SST behaves as a near-ideal Thevenin source into a first-order pole set by $R_S C_{tot}$, so the energy goes primarily into charging the junction capacitance rather than into a termination network. This difference is central for short, capacitive PIC links.

Swing and optical modulation amplitude follow directly from the output stage. In CML the single-ended swing is set by $I_{tail}R_L$ and is bounded by headroom at advanced nodes and by the need to maintain a low output impedance. VM-SST can approach rail-to-rail at the modulator node, which helps micro-rings whose required voltage swing increases once process spread and bias offsets are included. The higher usable swing reduces the burden on bias placement and relaxes the required electro-optic efficiency of the device.

Power scales differently as well. CML consumes static power on the order of $V_{DD}I_{tail}$ regardless of data activity, which grows linearly with the number of WDM channels. VM-SST is dominated by dynamic switching, roughly proportional to $C_{tot}V_{swing}^2$ and the baud rate, so idle or low-activity periods cost little and the absence of far-end terminations avoids continuous dissipation.

Linearity and eye uniformity are the deciding factors for PAM-4 on rings. A bare voltage-mode stage shows level-dependent bandwidth because the effective source resistance varies with operating point, which shrinks the inner eyes. Adding the series resistor fixes this. As shown in Fig. 2-9, R_S forces most of the transition drop to appear across a known element, keeps the MOS devices in the linear region with small V_{DS}, and makes the time constant nearly independent of the PAM-4 level. The same dominance of R_S also stabilizes the code-to-level mapping at the sampling instant. CML can produce clean edges into resistive loads, but when the optical load is capacitive it either requires dissipative terminations or it sees a level-dependent RC through device output resistance, so the eye uniformity advantage shifts to VM-SST in the ring case.

There are practical trade-offs. A larger R_S improves level-to-level uniformity yet lowers absolute electrical bandwidth since the pole is $1/(2\pi R_S C_{tot})$ Reducing the driver on-resistance achieves the same uniformity without sacrificing bandwidth, but upsizing devices raises gate and capacitances, increases pre-driver effort and energy, and can add to

C_{tot} through larger junctions and routing. CML offers stable common-mode and good supply-bounce immunity, while VM-SST requires careful local decoupling and short routing to keep the single dominant pole well defined. For dense WDM arrays the replication cost matters. VM-SST reuses standard CMOS logic slices and one series resistor per lane, while CML adds bias generation and static current per lane, which compounds thermal load near the PIC.

Table 2-1
Comparison of CML and VM-SST Drivers

Category	**CML Driver**	**VM-SST Driver**
Target Load	Long-reach, 50-Ω TL	Capacitive MRM
Output Swing	Limited (I_{tail} R_L)	Near Rail-to-rail
Power type	Static power	Dynamic power
PAM-4 Suitability	Swing–Limited	Good Linearity
Scalability	Static current per lane	Easy replication

Table 2-1 summarizes the key differences between CML and VM-SST drivers, showing why VM-SST is better suited for capacitive micro-ring PAM-4 transmitters. For short-reach, capacitive micro-ring PAM-4 links the VM-SST approach provides higher usable swing, lower static power, and better level-independent transition behavior once R_S is chosen appropriately. CML remains the right choice when controlled impedance over distance is mandatory, for example with traveling-wave modulators. Given the target

architecture in this thesis, the subsequent chapters adopt VM-SST as the baseline driver and focus on sizing R_S and the output devices to balance bandwidth, power, and level accuracy.

2.3 PAM-4: ADVANCED SIGNALING SCHEMES

2.3.1 PAM-4 fundamentals and link-level implications

High-throughput optical links can raise information rate by pushing the symbol rate or by placing more bits on each symbol. Wavelength-division multiplexing (WDM) increases parallelism across carriers [35]–[40]. Within a single lane the choice is between binary signaling such as non-return-to-zero (NRZ) and multi-level formats such as four-level pulse amplitude modulation (PAM-4) [41]. Given a fixed analog bandwidth at the electrical driver and the modulator, PAM-4 delivers two bits per symbol where NRZ carries one bit per symbol. The gross bit rate therefore doubles at the same symbol rate. This gain comes with a cost in noise margin, level linearity, and jitter sensitivity.

In a linear additive noise model, PAM-4 reduces the vertical eye height for each decision by roughly a factor of three at a given peak-to-peak swing. The four levels cluster at quarter-steps between the rails, so the minimum distance between adjacent decision thresholds is small. Any error source that projects into amplitude, such as thermal noise or residual inter-symbol interference, consumes a larger fraction of that distance than it would for NRZ. The receiver must also place and hold three decision thresholds rather than one, which introduces threshold placement error as an additional sensitivity. These effects explain why PAM-4 generally requires stronger calibration and tighter component tolerances than NRZ for the same target error rate.

Timing effects become more visible with multi-level signals. For a given unit-interval

(UI) the same absolute jitter consumes a larger fraction of eye width when the inner symbol transitions slow down near the mid-levels. This mechanism is particularly relevant in capacitive links where the effective electrical time constant depends on the instantaneous output level. Without conditioning, the inner eyes of PAM-4 compress even when the static level mapping is accurate. Section 2.2 showed that source-series termination (SST) reduces this dependence by forcing most of the dynamic voltage drop to appear across a known resistor. The transition then follows a nearly level-independent first-order law and the inner and outer eyes open more uniformly.

Equalization strategies for short-reach silicon photonics tend to be modest because the electrical path between driver and modulator is short and the optical device often dominates the link response. Pre-emphasis in the driver can help where the single first-order pole limits edge speed. In PAM-4 systems pre-emphasis must be short in duration so that the settled level is still defined by the weighted sum of slices. Long tails would convert to level-dependent overshoot and create vertical noise at the sampler. Decision-feedback equalization (DFE) is less attractive at the optical receiver when the dominant distortion is amplitude compression in the modulator rather than dispersive inter-symbol interference in a long channel.

Forward error correction closes residual gaps by converting a small pre-FEC error rate to a much smaller post-FEC error rate at tolerable overhead. It adds latency and power and it does not repair deterministic eye distortion that reduces the distance between decision thresholds. For short-reach WDM arrays used with micro-rings the most effective path is to maximize the quality of the analog waveform at the transmitter, then apply a light FEC to cover the remaining random errors. That approach preserves low end-to-end latency while maintaining the throughput benefit of PAM-4 at the symbol rates of interest.

2.3.2 Thermometer encoding for PAM-4 drivers

PAM-4 drivers can be built with two weighted branches controlled by the most significant bit (MSB) and the least significant bit (LSB), or with a segmented structure that enables a monotonic set of equal-weight slices. In a conventional binary-coded design, transitions like 10 to 01 require the two branches to toggle in opposite directions at nearly the same instant. Any finite skew between those edges can momentarily turn both branches on or both off, which injects a spurious pulse and degrades the eye through glitch energy and extra jitter.

Thermometer encoding avoids that hazard by mapping the two-bit word to a three-slice unary code in which each higher level enables one additional segment while the already enabled segments remain on. Only one slice changes state between adjacent PAM-4 levels. The output slew is monotonic and the driver is not exposed to opposite-direction switching. The result is a cleaner waveform with fewer glitches and less inter-symbol interference that originates in the driver [29], [42], [43].

A minimal mapping that supports four output levels uses three equal slices T_C, T_B, and T_A. The enabled set grows as the level increases as shown below.

Table 2-2

Two-bit to three-slice thermometer mapping for PAM-4

Decimal	**Binary**		**Thermometer**		
	MSB	LSB	T_A	T_B	T_C
0	0	0	0	0	0
1	0	1	1	0	0
2	1	0	1	1	0
3	1	1	1	1	1

This mapping corresponds to the thermometer table commonly used in PAM-4 drivers and ensures single-sided, monotonic updates between adjacent levels.

From a link-level standpoint, thermometer encoding also helps preserve PAM-4 level spacing because each increment ideally adds the same contribution to the output amplitude. That uniformity improves the RLM metric defined by IEEE 802.3 for PAM signaling. In practice the slices are only approximately identical, so residual mismatch among segments can still compress one eye relative to the others. Even so, thermometer encoding removes the dominant binary-glitch mechanism and leaves a primarily static matching problem that can be trimmed or lightly pre-distorted in the driver.

2.3.3 Summary

PAM-4 increases spectral efficiency within a fixed analog bandwidth, which supports energy and pin efficiency in dense WDM systems. The cost is reduced eye height and greater sensitivity to amplitude error, nonlinearity, and timing uncertainty. Thermometer encoding improves transmitter behavior by eliminating binary-coding glitches and keeping level steps monotonic. Section 2.4 turns to the device side and explains how the micro-ring transfer curve affects level spacing and why bias placement and hold are required.

2.4 NONLINEARITY IN MICRO RING MODULATORS

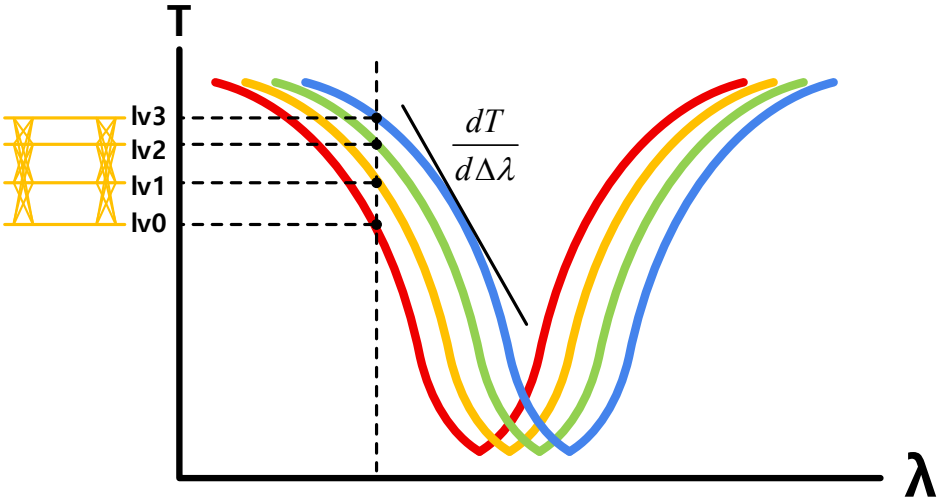


Fig. 2-10. Illustration of PAM-4 level placement on the static resonance curve of the micro-ring modulator

A silicon micro-ring modulator converts voltage to intensity through resonance detuning. The depletion-mode junction in the ring changes the effective index, which shifts the resonance wavelength. The optical transmission versus detuning is a resonant curve with finite linewidth. The electrical-to-optical mapping can be written in a compact form

$$I_{\text{out}}(V) = T(\Delta\lambda(V))P_{\text{in}} \tag{2.21}$$

where P_{in} is the MRM input power, $T(\cdot)$ is the ring transmission around the operating port, and $\Delta\lambda(V)$ is the voltage-induced resonance shift. The small-signal gain that links electrical swing to optical swing is the product of a device term and a photonic term

$$\frac{dI_{\text{out}}}{dV} = \frac{dT}{d\Delta\lambda}\frac{d\Delta\lambda}{dV}P_{\text{in}} \tag{2.22}$$

Only a narrow bias window yields an approximately constant slope. Away from that window the curvature of the resonance makes the mapping from voltage to intensity nonlinear.

As illustrated in Fig. 2-10, the four PAM-4 levels must be placed on this curved transfer function, and their relative spacing depends directly on the local slope $dT/d\Delta\lambda$. If the levels span too much of the resonance, the inner and outer steps become unequal because the slope varies with detuning. The eye openings then become nonuniform even when the electrical driver forms perfect voltage steps. In practice the modulator must be biased so that the usable four-level set sits on a part of the curve with near-constant slope. That requirement competes with other constraints such as insertion loss and extinction ratio. For a given optical carrier, bias drift of tens of picometers moves the working point enough to change the slope and therefore the level separation. Temperature variation is the dominant source of such drift in silicon photonics. This is why bias acquisition and hold are necessary even in a static link.

Dynamic effects add another layer. The ring has a finite photon lifetime and the junction presents an electrical capacitance that is driven by the output stage. The combined electro-optic bandwidth is the minimum of the electrical pole and the optical pole. If the electrical pole is dominant, the SST approach from Section 2.2 yields uniform transition speed and the dynamic nonlinearity is modest. If the optical pole is dominant, the ring's own dynamics shape the waveform. A step in voltage maps to a detuning step, and the cavity responds by gradually approaching the new operating point with a characteristic time constant. That response creates a memory that is independent of the driver and can be interpreted as low-pass filtering of the ideal PAM-4 pulse train. In both cases the

fundamental nonlinearity stems from the static resonance curve that converts detuning to intensity and the solution begins with careful bias placement.

Process variation and fabrication tolerances shift the resonance and change the coupling condition between the ring and its bus. Those shifts alter the depth and width of the resonance and therefore change the available slope at a given laser wavelength. Arrays of rings intended for WDM amplify this issue because each device must be biased to the correct working point while sharing a thermal environment. The practical outcome is that open-loop placement of the bias is not sufficient. A closed-loop method is needed to acquire the bias and to hold it in the presence of drift and crosstalk.

For the summary of Chapter 2.4: it is enough to record two facts. First, ring nonlinearity is the principal reason why PAM-4 level spacing is difficult to maintain over time without calibration. Second, the combined electro-optic bandwidth and the driver architecture determine whether the dynamic response exacerbates that nonlinearity or whether it remains a static bias-placement problem. The following sections build on these points when describing thermal calibration and multi-channel integration.

2.5 WAVELENGTH-DIVISION MULTIPLEXING

Wavelength-division multiplexing (WDM) is spectral parallelism. Multiple optical carriers share one fiber and each lane uses a distinct wavelength that is combined and separated by wavelength-selective elements on the chip. In silicon photonics the common choices are ring-based filters and arrayed waveguide gratings. A ring modulator fits a per-channel architecture because the same resonant element both selects the wavelength and applies the modulation [44], [45].

Channel spacing is the separation between adjacent lanes, expressed in frequency or wavelength. The spacing is chosen larger than the filter linewidth so that leakage from neighbors remains small and so that there is guard margin for drift and process spread. Wider spacing reduces crosstalk and simplifies bias hold at the cost of a larger occupied spectrum. Tighter spacing improves spectral efficiency and integration density but makes the array more sensitive to temperature variation and device mismatch. Around 1550 nm a change of about 1-nm corresponds to roughly 125-GHz [46].

In ring-based plans the free spectral range sets how often the resonance pattern repeats. The occupied WDM band should fit well within one free spectral range so that higher order repeats do not overlap the channel plan. A simple way to think about it is that the free spectral range should exceed the product of channel count and spacing with some extra guard.

Laser planning follows two basic patterns. Multiple lasers provide carriers on an external grid and each channel couples one of those carriers into its ring. This simplifies per-channel alignment but increases laser count. A single laser can be split on chip and each ring is thermally tuned to a unique resonance. This reduces hardware but increases the

tuning burden because the rings must be pulled to their assigned wavelengths and then held there. In both cases the laser and the ring need to remain aligned inside the chosen guard band during operation.

Thermal interaction is the dominant coupling mechanism in dense arrays. Heater power on one ring can conduct through the substrate and shift the resonance of a neighbor by a small but meaningful amount. Placing drivers close to the photonics reduces electrical loss yet adds local heat. Layout spacing, heater placement, and low-bandwidth bias loops are therefore part of the WDM design space. Electrical crosstalk across short on-package runs is usually modest, although common supplies and routing can couple noise if decoupling is insufficient.

The loaded quality factor (Q_L) connects static and dynamic behavior. A higher quality factor increases the local slope and extinction and reduces carrier leakage, which is helpful for optical modulation amplitude and eye height. The trade-off is a narrower optical bandwidth and greater sensitivity to drift. A lower quality factor relaxes bandwidth limits and eases alignment but reduces the available slope per volt. For PAM-4 a moderate quality factor is often preferred so that per-lane slope remains adequate while the optical bandwidth stays compatible with the symbol rate and with the simple first-order electrical pole set by the driver and the modulator capacitance. In practice the design loop is iterative. One first measures or conservatively estimates the filter linewidth and the expected drift envelope, then sets a spacing and guard that keep each lane on the high-slope portion of its own response while suppressing leakage from neighbors. The free spectral range is chosen comfortably larger than the occupied band. The laser plan is picked with awareness of tuning power and hold stability. Thermal layout and slow bias control close the loop. With these elements in place, WDM raises throughput and pin efficiency by sharing a fiber while preserving per-lane waveform quality.

Table 2-2 summarizes current WDM channel grids and representative wavelength sets used in recent standards. At the standard level, DWDM fixed and flexible grids are defined by ITU-T G.694.1. The DWDM frequency grid is anchored at 193.1 THz and supports fixed spacings from 12.5 GHz to 100 GHz, and a flexible grid with 12.5 GHz granularity via frequency slots and slot widths. CWDM grids are defined by ITU-T G.694.2 with 20 nm spacing over nominal center wavelengths from 1271 nm to 1611 nm. Short-reach Ethernet optics use both: LAN-WDM around 1310 nm with closely spaced lines for 100GBASE-LR4, and CWDM4 for 400GBASE-FR4.

Table 2-3

WDM channel grids in current standards

Category / Use	Standard	Anchor	Channel Spacing
DWDM (fixed grid)	ITU-T G.694.1 (latest, 2020 edition)	193.1 THz	100 GHz, 50 GHz, 25 GHz, 12.5 GHz (and integer multiples)
DWDM (flexible / elastic grid)	ITU-T G.694.1 (Edition 3)	193.1 THz	Minimum slot width of 12.5 GHz
CWDM	ITU-T G.694.2 (2003)	O- to L-band	20 nm spacing
LAN WDM / IEEE for 100G LR4	IEEE 802.3	~1310 nm band	~ 4–5 nm spacing
CWDM4 for 400G FR4	IEEE 802.3cu / CWDM4 MSA	~1310 nm band	~ 20 nm spacing

2.6 Summary and Design implications for the Transmitter Architecture

The discussions in Chapter 2 highlight the key device- and link-level challenges associated with silicon micro-ring modulators, including their static nonlinearity, narrow bias window, and strong thermal sensitivity. These characteristics imply that a practical transmitter must incorporate both a high-bandwidth driver optimized for capacitive loading and a calibration mechanism capable of maintaining the correct optical operating point in the presence of drift.

Chapter 3 focuses on developing such a transmitter architecture in a single-channel setting, integrating an SST-based electrical driver with a bit-pattern-assisted thermal calibration algorithm. This single-channel implementation provides a controlled environment to validate the calibration and driver concepts introduced in Chapter 2, and forms the foundation for the multi-channel extensions discussed later in the dissertation.

CHAPTER 3 Design of a 32-Gb/s Silicon Micro-ring Transmitter with Code-Based Thermal Calibration

This chapter presents the design, implementation, and experimental validation of a single-channel silicon photonic transmitter that integrates a MRM with a compact, code-based temperature calibration algorithm. The work aims to address the inherent sensitivity of MRMs to thermal variation, which can significantly degrade modulation performance in high-speed optical interconnects. To achieve stable operation without relying on external feedback or signal processing units, the proposed transmitter leverages a hybrid integration of a silicon photonic integrated circuit (PIC) and a CMOS electronic integrated circuit (EIC), with all calibration logic implemented on-chip. The chapter begins with an overview of the system architecture, followed by a review of existing thermal calibration techniques and their limitations. It then introduces the proposed calibration method based on deterministic data patterns and low-bandwidth monitoring, and concludes with measurement results that verify the effectiveness and robustness of the approach. The work in this chapter serves as a foundational building block for the multi-channel extension discussed in Chapter 4.

3.1 OVERVIEW OF THE TRANSMITTER ARCHITECTURE

The hybrid silicon photonic transmitter integrates both photonic and electronic building blocks to enable high-speed, thermally stable optical modulation. As illustrated in Fig. 3.1, the system consists of a photonic integrated circuit (PIC) that includes the optical devices, and an EIC that incorporates high-speed data generation, driver circuitry, and a fully integrated temperature calibration controller. The two chips are co-packaged using wire bonding to enable compact and low-loss integration.

On the photonic side, the PIC features a MRM with a metal heater placed above the ring structure for thermal tuning. The MRM is side-coupled to a silicon waveguide that routes input light from an external C-band tunable laser. The modulated optical signal is primarily delivered through the through port of the MRM. However, at resonance, a significant portion of the optical power is coupled into the ring and exits through the drop port. The combined output power from the through and drop ports remains approximately constant, assuming negligible propagation loss. An integrated germanium photodetector (PD) is connected to the drop port to monitor the resonance condition, enabling feedback for temperature calibration and locking.

The EIC consists of two main subsystems: a high-speed data generation path and a temperature control loop. The data generation path consists of a PRBS31 generator, a chain of retimers and multiplexers, and a voltage-mode driver with a $2V_{pp}$ output swing AC-coupled to the MRM. A detailed description of these sub-blocks is provided in Section 3.2. A CMOS clock divider and CML-to-CMOS converter generate the appropriate clock signals, while a digitally controlled delay line (DCDL) and associated circuits, such as the duty cycle corrector (DCC) and quadrature error corrector (QEC), ensure timing alignment

across the transmitter chain. The driver structure consists of an 8:4 and 4:1 serialization stage followed by differential amplifiers and pull-up/down biasing networks, optimized for capacitive loading from the MRM.

The upper portion of the EIC is dedicated to temperature calibration and locking. The monitor PD signal is filtered by a low-pass filter (LPF) to remove high-speed components and then digitized using an 8-bit successive approximation register (SAR) analog-to-digital converter (ADC). The resulting digital value is processed by a finite state machine (FSM) inside the thermal controller, which selects among different pre-defined 4-bit calibration patterns to evaluate the modulator's response. Based on the measured average powers, the controller determines the optimal heater code and updates the output of a 10-bit digital-to-analog converter (DAC) that supplies the heater voltage V_{heater}. This feedback loop enables both one-time calibration and continuous resonance locking through periodic dithering.

The integration of both temperature control and data modulation within a single transmitter platform allows autonomous resonance tuning without relying on external DSP or real-time optical analysis. This architectural approach achieves high signal integrity across a wide temperature range, and serves as a foundation for scalable WDM implementations described in the following Chapter 4.

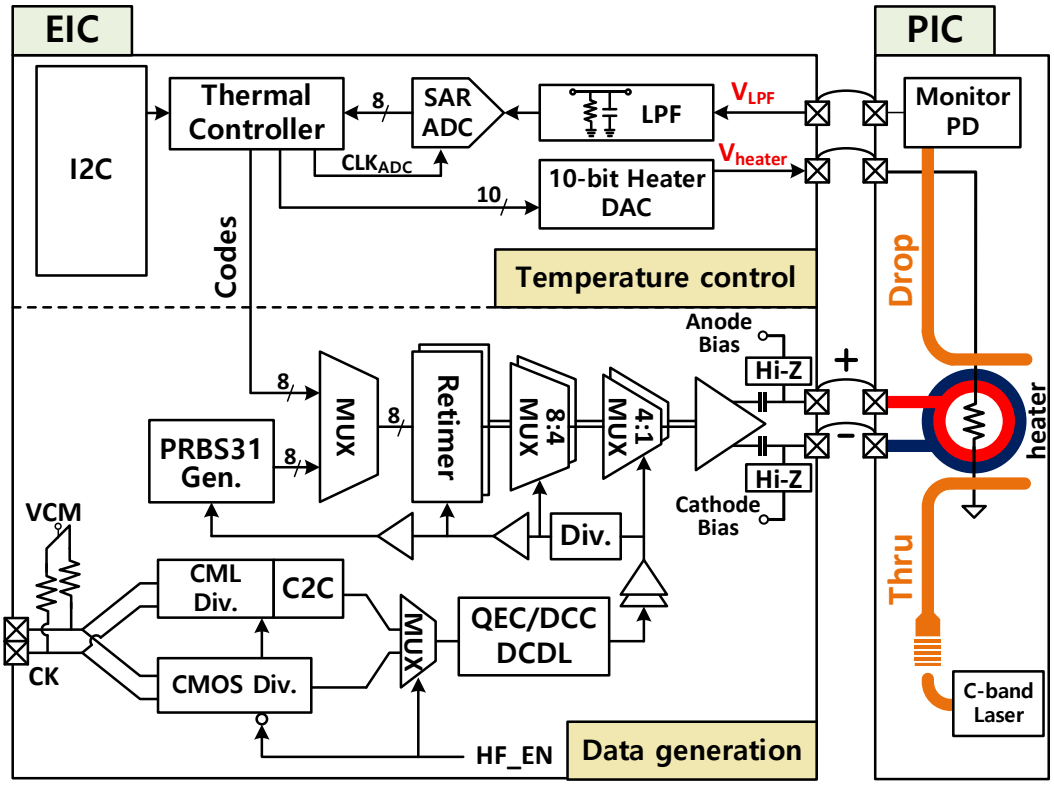


Fig. 3-1. Top block diagram for the hybrid Si MRM transmitter with temperature controller [47].

3.2 IMPLEMENTATION OF TX BUILDING BLOCKS

The proposed hybrid silicon photonic transmitter integrates both high-speed data modulation and autonomous thermal control circuitry within a single system. This section describes the internal functional blocks, particularly those implemented in the CMOS IC, which are responsible for clock conditioning, data generation and serialization, optical modulation, and closed-loop resonance control.

3.2.1 Clock Distribution and Conditioning

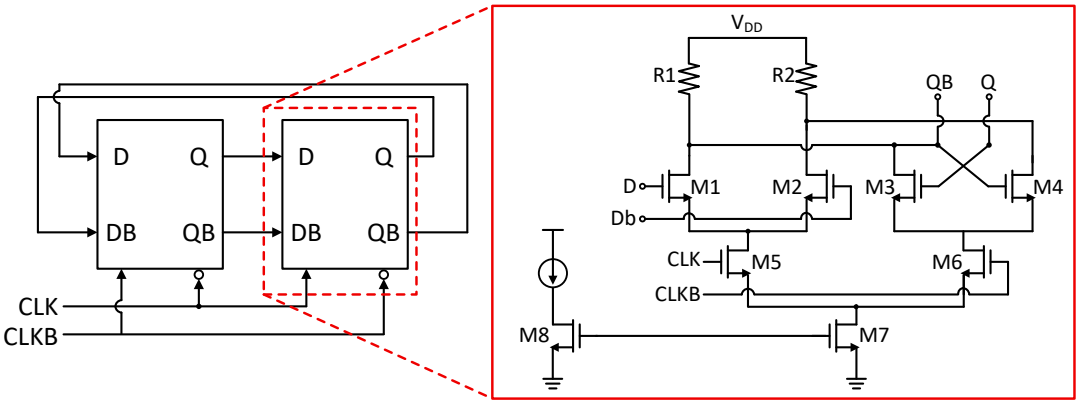


Fig. 3-2. CML frequency divider and its internal latch implementation.

The high-speed frequency divider used in this design is implemented using CML flip-flops to ensure proper functionality at clock frequencies above 2 GHz. As illustrated in Fig. 3.2, the divider consists of a cascade of D flip-flops, each implemented with a differential latch circuit. The internal structure of the latch comprises a pair of NMOS differential input transistors (M1 and M2), resistive loads (R1 and R2), and cross-coupled NMOS transistors (M3 and M4) to retain logic state during clock transitions.

Clocking is achieved using complementary clock signals (CLK and CLKB), which gate the tail-switch transistors (M5 and M6) that control the current flow through the latch. A constant bias current is supplied by M8, with an additional tail transistor M7 ensuring common-mode stability.

This CML implementation provides robust high-speed performance with minimal jitter and reduced sensitivity to supply variation, making it suitable for multi-gigahertz operation. The latch topology also minimizes signal swing, thereby enabling high-speed operation with low dynamic power consumption.

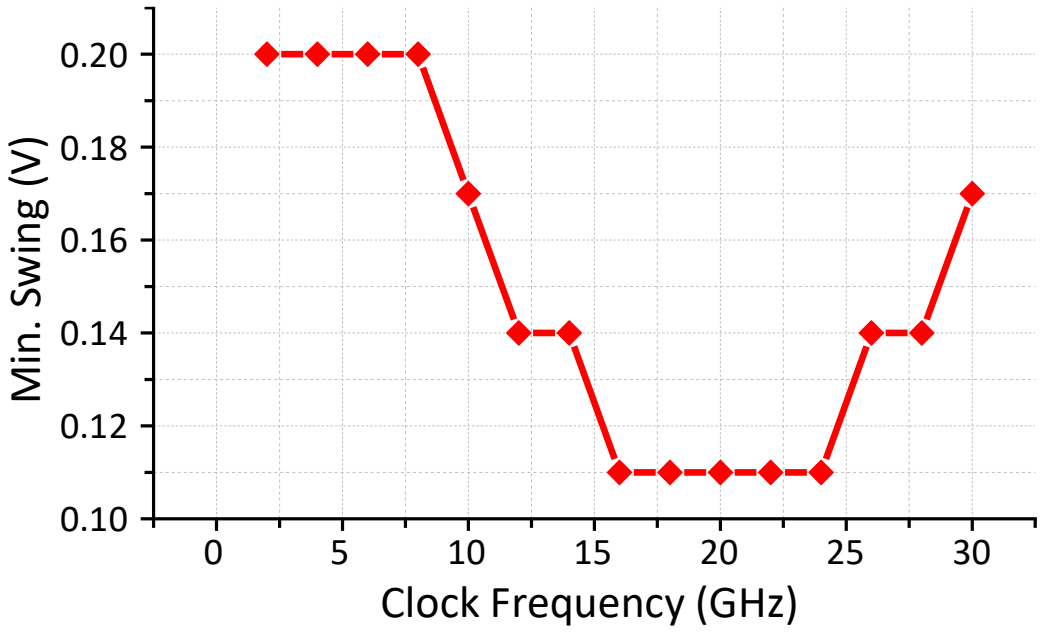


Fig. 3-3. Simulated minimum differential input swing required for the CML divider versus input clock frequency.

Fig. 3.3 presents the simulated minimum differential input swing required for the CML divider to operate reliably across a wide range of input frequencies. The divider exhibits robust sensitivity down to ~110 mV_{pp} in the frequency range of 15–25 GHz, where the circuit operates in its optimal region. Below 10 GHz, the required swing increases significantly, reaching ~200 mV_{pp} at 5 GHz, indicating reduced sensitivity and degraded latch regeneration due to insufficient gain and bandwidth.

These results confirm the practical frequency range in which the CML divider operates with sufficient margin and justify the use of an input clock ≥8 GHz in the actual transmitter system. To ensure proper logic functionality and minimize signal degradation, the system employs an external clock amplitude of at least 200 mVpp, which provides sufficient margin across the entire operating frequency range.

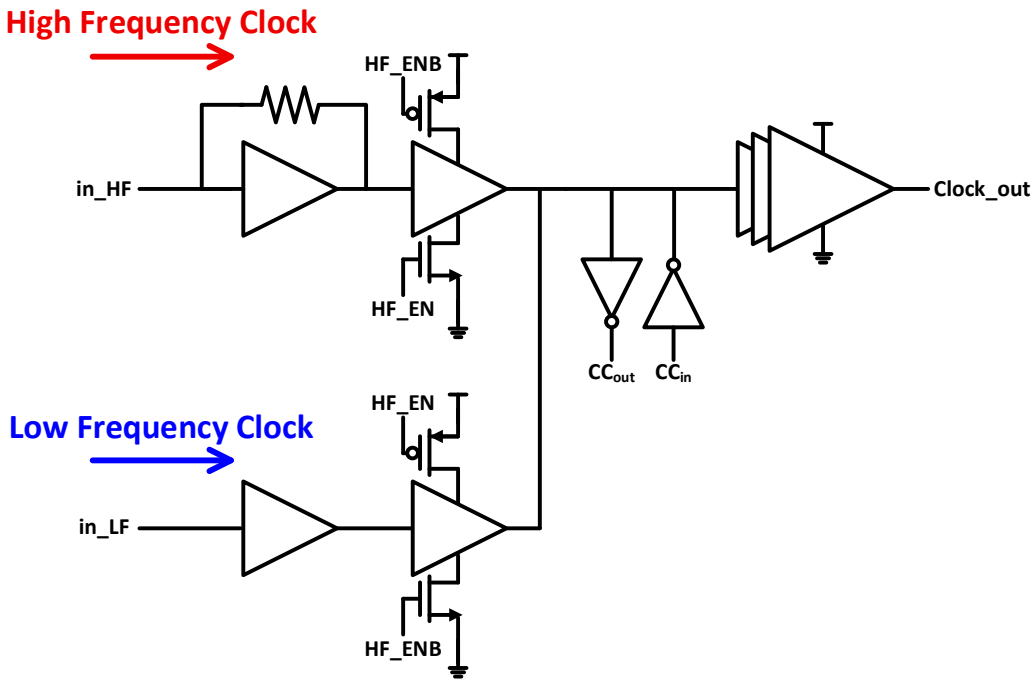
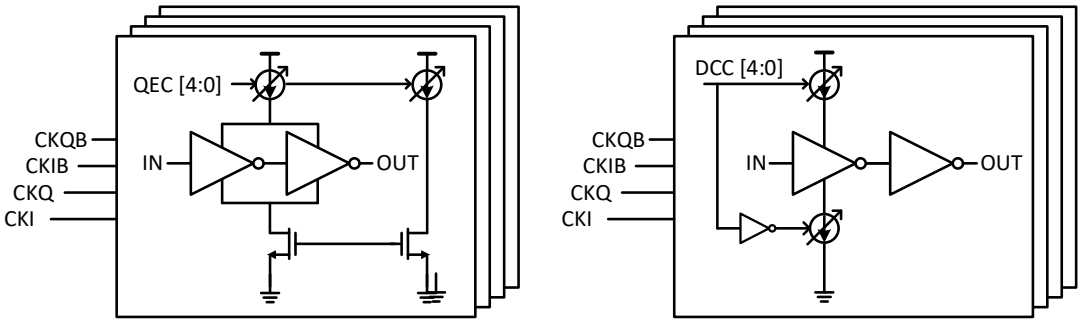


Fig. 3-4. Block diagram of the dual-path (CMOS / CML) clock selector

To accommodate a wide range of input clock frequencies, the proposed transmitter employs two distinct clock divider paths: a CMOS divider for low-frequency operation and a CML divider for high-speed operation. As shown in Fig. 3.4, the outputs of these two dividers are connected to a tri-state buffer-based clock selection circuit, which allows switching between the two domains depending on the operational mode.

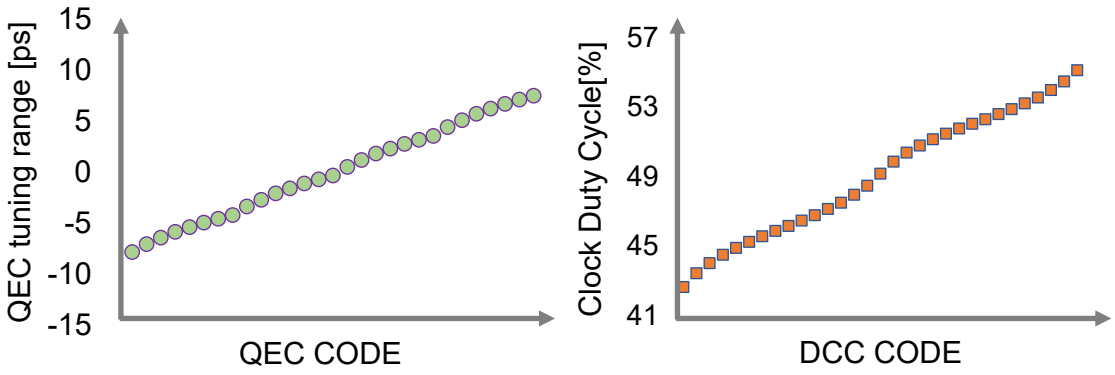
The selection is governed by two complementary control signals, HF_EN and HF_ENB, which enable only one clock path at a time while placing the other in a high-impedance state. This ensures that there is no contention at the shared output node and minimizes signal distortion or glitches during mode transitions. The selected clock signal is then routed through labeled nodes (CC_{in}, CC_{out}) that interface with the complementary phase divider chain. These nodes are not standalone inverter blocks but represent the

interconnection points between the two divider outputs and the shared clock distribution network. This structure ensures that clock phases remain synchronized between the two divider domains and helps maintain signal integrity when switching between operating modes.



(a) (b)

Fig. 3-5. Schematic of the digitally controlled (a) quadrature error corrector (QEC) and (b) duty cycle corrector (DCC) blocks.



(a) (b)

Fig. 3-6. Post-layout simulation results showing the tuning range and resolution of (a) the QEC and (b) the DCC circuits.

To ensure reliable high-speed serialization and robust timing calibration, the proposed transmitter includes two building blocks in its clock path: the duty cycle corrector (DCC) and the quadrature error corrector (QEC), as illustrated in Fig. 3.5. These blocks enable fine-tuned control over the clock waveform, correcting duty cycle imbalances and aligning quadrature-phase clocks used in the serializer and output driver.

While conceptually similar to conventional delay tuning circuits that utilize capacitor banks, the DCC and QEC in this design adopt a digitally controlled delay mechanism based on MOS switch arrays. Each control bit (DCC[4:0] or QEC[4:0]) enables a set of MOS transistors connected to either the pull-up or pull-down paths of an inverter stage. The number of activated transistors determines the on-resistance r_{on}, which modulates the delay through the inverter's RC characteristics. In this structure, the delay is tuned by adjusting resistance rather than capacitance, resulting in similar control over signal edge timing.

This method offers several practical advantages. It enables compact, fully digital control without requiring analog bias voltages or large metal capacitors, making it particularly well-suited for integration in high-speed digital environments. Moreover, the granularity of delay tuning can be finely controlled by the bit resolution of the digital code, and the symmetric nature of the design ensures consistent tuning behavior across PVT variations.

As shown in Fig. 3.6, post-layout simulation results verify that both the DCC and QEC modules achieve sufficient tuning range and resolution for robust clock calibration. The DCC adjusts the relative timing of the rising and falling clock edges to correct duty cycle distortion at the serializer input, achieving a tunable range from approximately 41% to 57% across its 5-bit control code. The QEC fine-tunes the phase skew between CKI and CKQ, offering a phase adjustment range of approximately ±7.5 ps with fine step granularity, ensuring proper quadrature alignment across clock domains.

3.2.2 Data Generation and Serialization Path

The high-speed data path is responsible for converting low-rate parallel data into a fully serialized differential output capable of modulating the silicon photonic MRM. The path initiates with a PRBS-31 generator designed to emulate the transmitted random data using a linear feedback shift register (LFSR) architecture. This generator operates at one-eighth of the full line rate, corresponding to 4 Gb/s, and delivers 8-bit wide parallel outputs synchronized to a divided version of the system clock derived from the 8 GHz input reference.

Immediately following the PRBS block is a pattern selector that provides the capability to switch between random PRBS data and fixed and repeated 4-bit deterministic patterns such as ‘1110’, ‘0001’, and ‘1100’. These calibration patterns are used specifically during the thermal tuning and optical monitoring stages, as discussed later. As depicted in Fig. 3.1, this selection is dynamically configured by the system-level controller described in Section 3.3, allowing seamless transition between data modulation and calibration without requiring physical reconfiguration of hardware. This flexibility enables the transmitter to operate in multiple modes, including normal data transmission and heater calibration, by using the same physical data path.

The selected 8-bit data is routed to a retiming circuit that ensures proper synchronization with the multi-phase clock signals used in the serialization stages. This retimer compensates for any clock skew that may have been introduced by the PRBS generator or pattern selector, thereby maintaining phase alignment with the high-speed serializer clock domain.

The retimed data is then processed through a two-stage serialization architecture. The

first serialization stage performs 8:4 multiplexing using conventional digital logic. To maximize the setup and hold timing margins at the multiplexer input, each of the 8 data bits is sampled by a dedicated retiming flip-flop clocked with a 90° phase-shifted version of the serialization clock. This technique enables fine-grained alignment of each data bit with respect to its respective clock edge, significantly improving timing robustness prior to serialization.

The final stage of the serializer chain employs a 4:1 multiplexer that combines four parallel data lines (D0–D3) into a single high-speed output stream operating at 32 Gb/s. As illustrated in Fig. 3-7, the multiplexer adopts a two-level NAND gate tree architecture, where the first stage selects between D0/D1 and D2/D3 to generate intermediate outputs D01 and D23, and the second stage combines them into D0123. Each NAND gate is clocked by overlapping multi-phase clocks ($C4_I/C4_Q/C4_{IB}/C4_{QB}$) to ensure correct timing alignment during high-speed switching.

A critical design challenge in this architecture arises from the intrinsic structure of the NAND gates. As shown in Fig. 3-8(a), each two-input NAND gate consists of a standard CMOS logic configuration with one PMOS in the pull-up and two stacked NMOS transistors in the pull-down path per input. Since all six transistors are driven in parallel, the gate exhibits roughly three times the input capacitance compared to a simple inverter, significantly limiting its switching speed at high frequencies. This large gate capacitance not only reduces transition sharpness but also prevents the gate from directly driving the following logic stage without degradation in eye opening.

To mitigate this bandwidth limitation, feedback equalizers are inserted at the output nodes of the NAND gates, specifically at D02, D13, and D0123. As illustrated in Fig. 3-8(b), each equalizer consists of an inverter with a feedback connection from its output to input. During transitions, the input and output momentarily oppose each other, creating a

fighting condition that prevents the output from fully swinging rail-to-rail. This controlled contention effectively enhances the rising and falling edge slopes, thereby increasing bandwidth and reducing inter-symbol interference (ISI).

Since this structure inherently consumes static current, each equalizer is equipped with a power-gating switch as shown in Fig.3-8(b), allowing it to be disabled during low-speed operation or calibration modes where high bandwidth is unnecessary. This selective activation mechanism improves overall energy efficiency without sacrificing high-speed performance when needed.

Fig. 3-9 shows the post-layout simulation results at 40 Gb/s. In Fig. 3-9(a), the NAND-based 4:1 MUX exhibits slow transitions and a reduced eye opening due to the large effective input capacitance of the stacked devices. In Fig. 3-8(b), enabling the feedback equalizer sharpens the edges and notably improves the eye opening, demonstrating its effectiveness in restoring high-speed signal integrity at the target data rate.

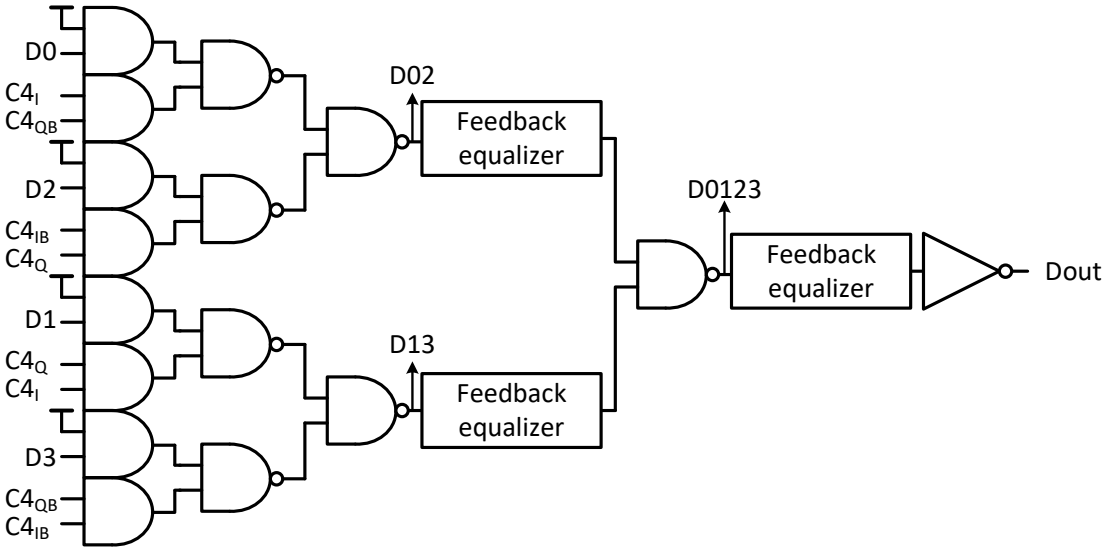
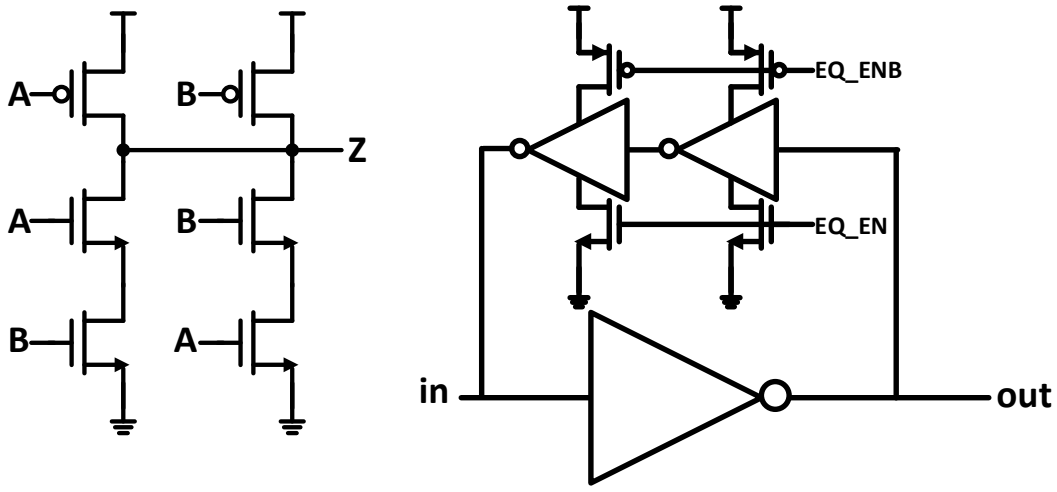
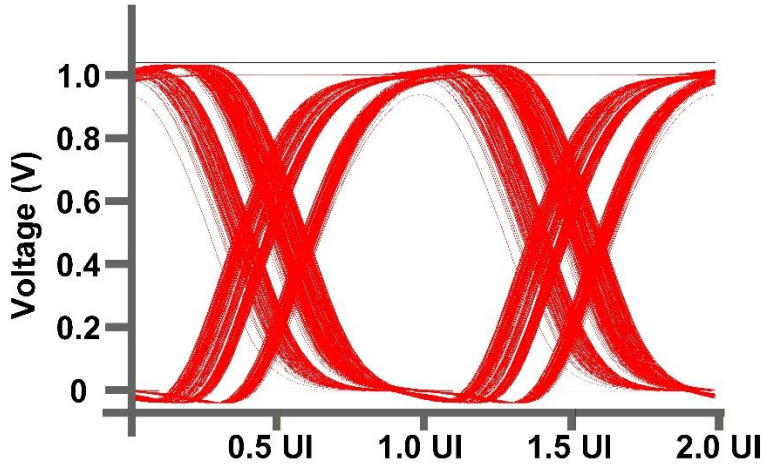


Fig. 3-7. Overall schematic of the 4:1 multiplexer using NAND gate tree structure with integrated feedback equalization.

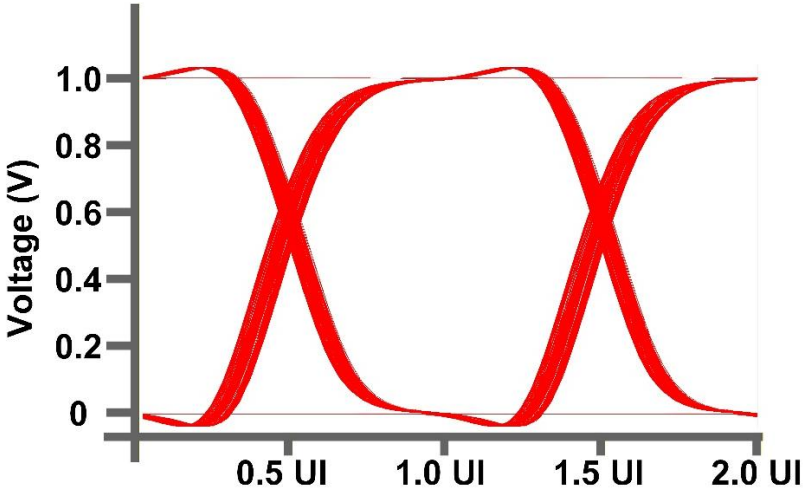


(a) (b)

Fig. 3-8. (a) Two-input NAND gate schematic (b) Schematic of the feedback equalizer



(a)



(b)

Fig. 3-9. Eye diagrams of the 4:1 MUX output: (a) without feedback equalization, (b) with feedback equalization.

3.2.3 Driver Structure and Output Network Configuration

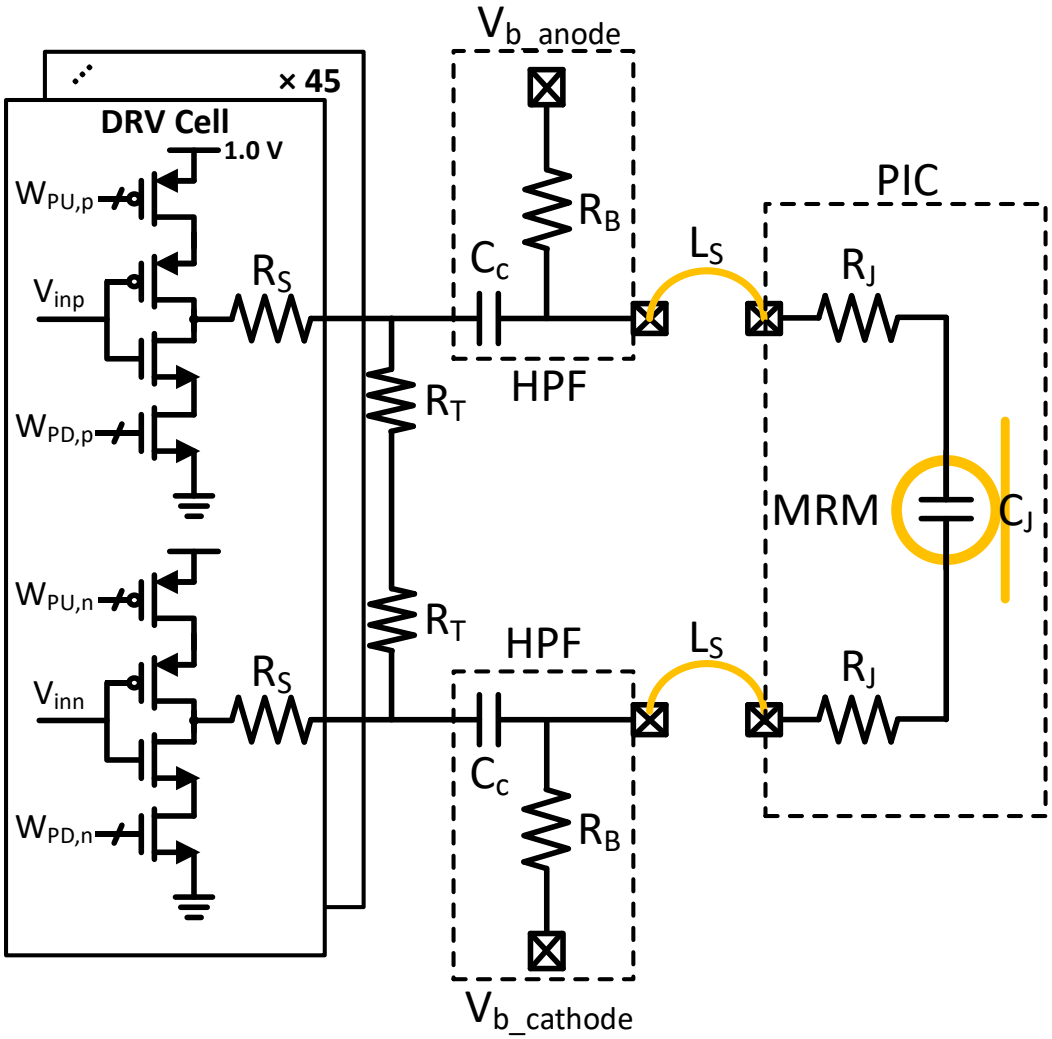


Fig. 3-10. Schematic of the output driver and passive network connecting the electrical IC to the photonic MRM, including AC-coupling.

Table 3-1

Passive component values used in the driver and output network

Component	Value	Purpose
R_S	400 Ω	Source series resistor
R_T	50 Ω	Termination resistor
C_C	1 pF	AC coupled capacitor
R_B	780 kΩ	Biasing resistor
L_S	650 pH	Bond wire inductor
R_J	1.1 Ω	Junction resistor
C_J	10 fF	Junction capacitor

The differential voltage-mode driver adopts a source-series terminated topology, where a resistor R_S is included in each output branch to enhance output linearity. The driver utilizes stacked PMOS and NMOS transistors to deliver a full $2V_{pp}$ differential swing, sufficient for depletion-mode modulation of the silicon MRM. This stacked structure allows for programmable output strength by enabling selective activation of the upper and lower transistors, supporting high-speed operation while maintaining symmetrical transitions.

The output of the driver is AC-coupled to the MRM through coupling capacitors C_C, and biased via large-valued resistors R_B connected to an external or on-chip common-mode voltage source V_{b_anode} and $V_{b\_cathode}$. The combination of C_C and R_B forms a high-pass filter that blocks low-frequency components, isolates DC offsets between the driver and the modulator, and ensures that the signal is properly centered around the desired bias point. To avoid degradation of low-frequency content and long-term baseline drift, R_B is selected to ensure a corner frequency well below the operating data rate. The criteria

for selecting the appropriate R_B will be discussed in detail in Section 3.3.

To further improve bandwidth, a termination resistor R_T is connected across the differential outputs. During differential signaling, the center point of R_T acts as an AC virtual ground, effectively reducing the output impedance of the driver. This reduction in impedance decreases the RC time constant of the driver output node, which helps extend the bandwidth and improve high-frequency signal integrity. However, because R_T forms a shunt path, a portion of the differential swing is lost across it. As a result, the voltage delivered to the modulator is reduced. This trade-off requires careful co-design of R_T and R_S to balance signal amplitude and bandwidth, while also accounting for the modulation characteristics of the micro-ring modulator. In particular, when the optical bandwidth of the modulator is inherently limited, further increasing the electrical bandwidth of the driver offers little benefit. On the other hand, if the modulator exhibits low modulation efficiency, preserving a higher voltage swing at the input becomes more critical to achieve sufficient optical modulation depth. The overall driver output network, including the SST structure, coupling elements, biasing resistors, and termination, is illustrated in Fig. 3-10, and the associated passive component values are summarized in Table 3-1. The output stage is implemented as a three-segment structure, with each segment containing 15 slices (2^4–1 levels), providing a total of 45 slices for programmable drive strength.

Fig. 3-11 illustrates the top-level layout of the hybrid Si MRM transmitter. The layout integrates the PRBS generator, clocking blocks, digital control logic, thermometer encoder, high-speed 4:1 multiplexer, and the differential SST driver, together with the passive AC-coupling and biasing network that interfaces the electrical IC with the silicon micro-ring modulator. Fig. 3-12 shows the post-layout 32-Gb/s, $2V_{pp}$ NRZ eye diagram of the transmitter. It shows that the driver, coupling network, and MRM interface maintain sufficient bandwidth and signal integrity under full parasitic extraction.

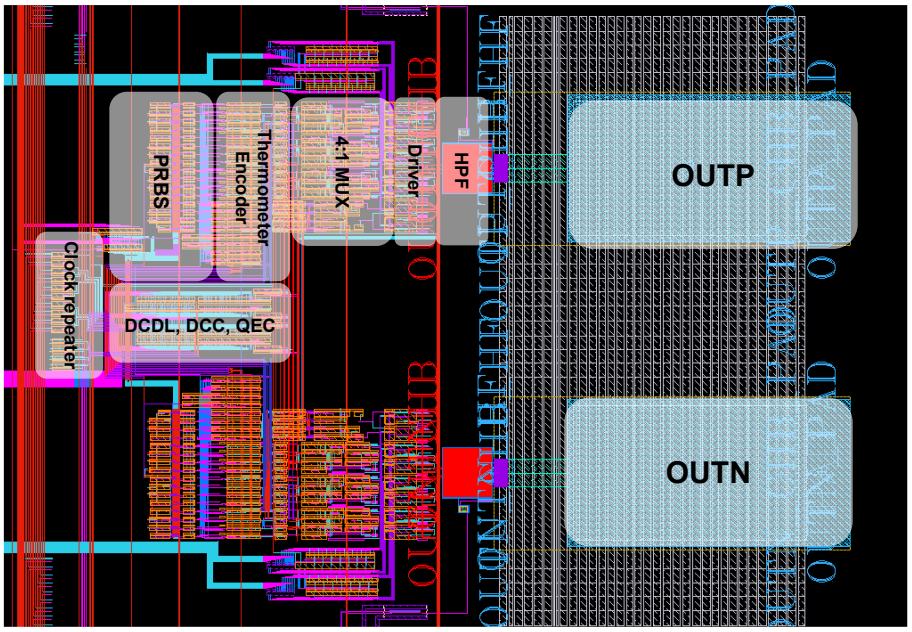


Fig. 3-11. Top-level layout of the hybrid Si MRM transmitter

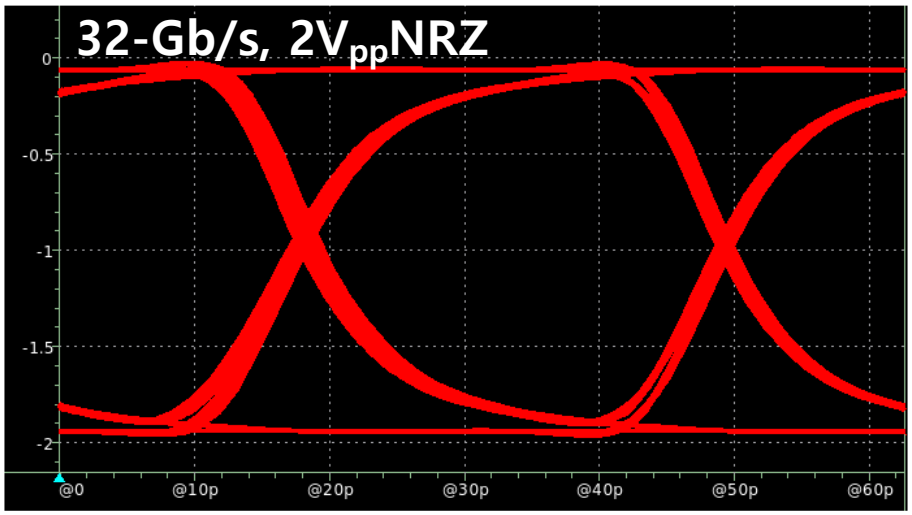


Fig. 3-12. Post-layout eye diagram of the 32-Gb/s Si MRM transmitter

3.2.4 Controller Interface Circuits

To support closed-loop thermal tuning of the MRM, a control interface is required within the control path. Specifically, this interface is responsible for delivering the appropriate heater voltage to the on-chip heater and for digitizing the optical feedback signal used in resonance tracking. While the detailed finite-state machine logic and thermal control algorithms are discussed later in Section 3.3, this section focuses on the interface circuitry, consisting of an on-chip 10-bit digital-to-analog converter (DAC) and an 8-bit successive approximation register (SAR) analog-to-digital converter (ADC).

As shown in Fig. 3-13, the DAC adopts a conventional R-2R ladder structure followed by an op-amp with negative feedback, converting a 10-bit digital control word into an accurate analog voltage. This heater voltage is used to supply the integrated heater through a resistive driver path, enabling precise wavelength control of the MRM. Due to the high thermal sensitivity of MRMs, where a small change in temperature results in substantial resonance wavelength shift, precise voltage resolution is critical. The 10-bit DAC provides sufficiently fine control steps to ensure accurate and repeatable heater tuning.

The SAR ADC, illustrated in Fig. 3-14, is used to digitize the low-frequency monitor signal obtained from the photodetector (PD) output. The architecture includes a sample-and-hold block, a switched-capacitor comparator network, and asynchronous logic to manage the conversion process. The ADC samples the monitor signal obtained from the integrated photodetector, which reflects the average optical output of the microring modulator. This digitalized value is then passed to the control logic to assist in thermal calibration and feedback locking.

Together, these interface blocks form the electrical bridge between the analog

photonic domain and the digital control logic. The DAC supplies the photonic heater, while the ADC senses the modulated optical signal, enabling real-time feedback and adaptation. While the closed-loop control logic determines the feedback behavior, the precision and robustness of the interface circuits, namely the ADC and DAC, play an equally critical role in defining the overall control fidelity. Any nonlinearity, quantization error, or noise in these circuits directly limits the accuracy of thermal tuning and resonance locking in the photonic front-end.

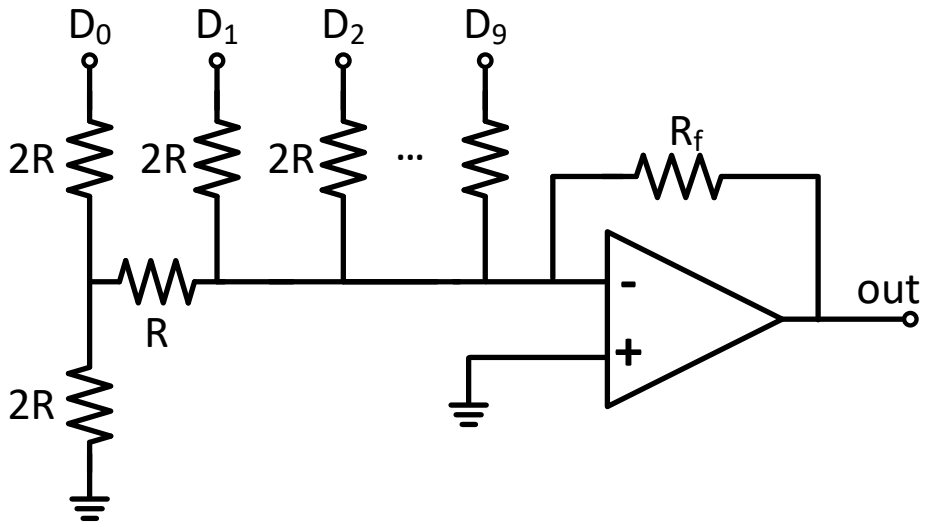


Fig. 3-13. 10-bit R-2R DAC with op-amp feedback for heater voltage.

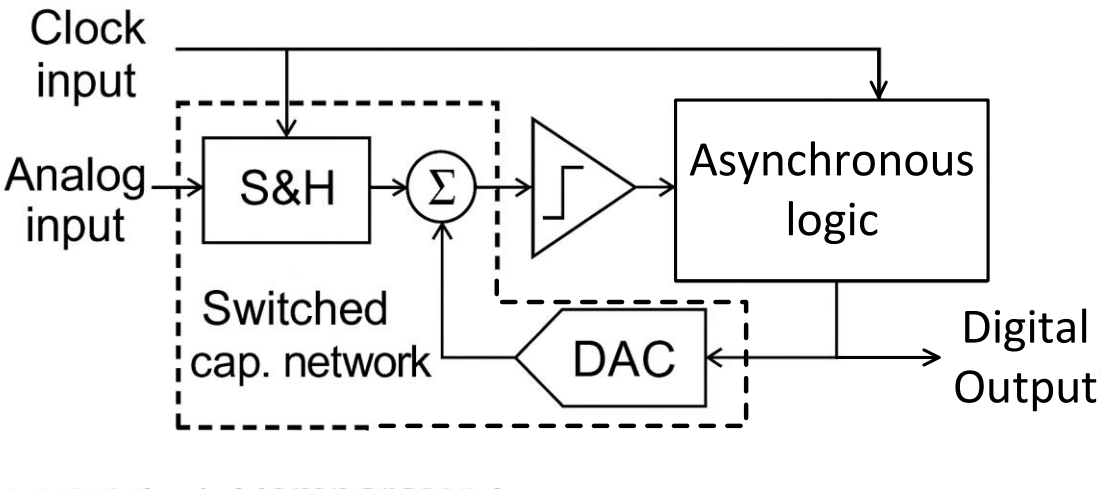


Fig. 3-14. 8-bit SAR ADC based on switched-capacitor architecture for monitoring photodetector output.

3.3 TEMPERATURE CONTROL ALGORITHM

As discussed in the preceding sections, MRMs are highly sensitive to temperature due to the thermo-optic effect of silicon. Even small variations in temperature can cause a significant shift in the resonance wavelength, leading to degraded OMA, reduced eye opening, and ultimately higher bit error rates. This sensitivity arises not only from ambient temperature changes, but also from self-heating by high-speed CMOS drivers and chip-to-chip process variations. The impact of thermal instability becomes even more critical in multi-channel WDM systems, where narrow channel spacing amplifies the effects of resonance drift, resulting in potential channel overlap and inter-channel crosstalk.

This chapter introduces a fully integrated temperature control algorithm designed to autonomously align and maintain the optimal modulation condition of the MRM. In this context, the optimal modulation condition refers to the specific detuning point at which the modulator achieves its maximum OMA, determined by a corresponding heater voltage. The algorithm eliminates the need for external digital signal processing or off-chip optical monitoring by relying solely on compact, low-speed electrical circuitry and digital logic for both initial calibration and continuous locking. Its simplicity and low overhead make it well suited for highly integrated, power-efficient optical transmitter architectures.

The structure of this section is as follows. Section 3.3.1 reviews major temperature control strategies reported in previous studies, including approaches based on average insertion loss, bit-level statistics, and direct OMA monitoring. The trade-offs among these methods are discussed in terms of implementation complexity, locking precision, and system scalability. Section 3.3.2 introduces the proposed code-based temperature control algorithm, which identifies the optimal operating point by sweeping the heater DAC and

analyzing the optical response under a set of predefined calibration patterns, referred to as codes. Once the optimal DAC setting is identified, the system enters a closed-loop mode where small dithering steps are applied to maintain resonance alignment over time. Section 3.3.3 describes the on-chip controller architecture and its gate-level implementation, including the finite-state-machine design, ADC/DAC interfaces, and behavioral co-simulation results that verify the complete calibration and locking sequence under realistic thermal conditions.

While the algorithm is verified in this chapter for a single modulator, the challenges of maintaining resonance stability become significantly more complex when extended to multi-channel WDM systems. These scalability issues will be further explored in Chapter 4.

3.3.1 Previous Temperature Control Algorithms

Numerous temperature control techniques have been proposed in prior studies to address the resonance instability of MRMs. These approaches vary in terms of sensing methodology, control architecture, and implementation overhead. This section reviews three representative schemes: temperature-sensor-based tracking [48], bit-statistics-based estimation [49], and insertion-loss monitoring [50]–[52]. Their trade-offs in tracking accuracy, hardware complexity, and scalability are compared, along with a discussion of the advantages offered by the proposed method.

A representative method is introduced in [48], where a temperature sensor-based feedback scheme is implemented in a monolithic silicon photonic transmitter. The system performs an initial calibration by sweeping the heater DAC while monitoring the OMA through an integrated photodetector. The heater value that yields the highest OMA is stored as the optimal operating point. During normal operation, an on-chip temperature sensor (typically PTAT-based) monitors the local thermal environment, and the system adjusts the heater DAC based on deviations from the calibrated reference. While this approach simplifies runtime operation by avoiding continuous optical monitoring, it inherently assumes a stable relationship between chip temperature and optical resonance. As a result, the control loop cannot compensate for laser wavelength drift or localized thermal effects from high-speed driver circuits, both of which often dominate in dense integration scenarios. Moreover, scaling this scheme to multi-channel WDM systems would require duplicating temperature sensors per modulator, leading to limited scalability.

In contrast, [49] presents a bit-statistics-based temperature stabilization technique that estimates detuning through statistical analysis of transmitted data. When the MRM is

slightly detuned from the laser wavelength, the resulting eye asymmetry causes a shift in the average voltage level observed at the receiver. By comparing the expected and observed bit distribution, such as the ratio of logical ‘1’s to ‘0’s in a DC-balanced pattern, the system infers both the degree and direction of detuning. A digital feedback loop then adjusts the heater DAC to restore the expected balance. Unlike [48], this method can partially compensate for laser drift and does not require explicit temperature sensors. However, its effectiveness relies on the ability to extract sufficient statistical information from the transmitted data over time, which can be challenging when the bitstream is highly skewed or varies unpredictably over short windows. While the method can theoretically operate under random or biased data conditions, estimation accuracy degrades under severely skewed payloads or short sampling windows. Additionally, its feedback loop relies on low-pass filtering of digital bit counts, which leads to limited responsiveness not only during calibration but also during payload transmission. This delayed response makes the system vulnerable to fast thermal transients or abrupt wavelength shifts.

The work in [50]–[52] takes a different approach by using insertion loss ratio monitoring through dual photodetectors placed at the input and output of the MRM. The system computes the ratio of output to input optical power, and a bang-bang controller adjusts the heater DAC accordingly. This technique inherently compensates for both temperature-induced detuning and laser wavelength variation, since it directly measures the optical response. It also operates continuously during normal data transmission and is agnostic to the transmitted bit pattern. However, the requirement for two photodetectors and transimpedance amplifiers (TIAs), along with analog signal conditioning circuits, significantly increases power and area overhead. Furthermore, as the control is based on insertion loss rather than direct modulation depth, it assumes that a fixed transmission level, such as the −6 dB point, represents optimal modulation. However, due to ring-to-ring

variations in Q-factor, coupling strength, and asymmetries, this point often deviates from the actual OMA peak. As a result, the system is likely to lock to a sub-optimal detuning point, which limits modulation efficiency.

A summary of the key characteristics of these techniques is presented in Table 3.1. While each approach offers trade-offs between complexity, tracking accuracy, and integration cost, none fully satisfy the requirements for precise, low-power, and scalable resonance stabilization. In particular, existing methods either rely on indirect sensing mechanisms that may drift over time [48], suffer from slow convergence due to statistical averaging [49], or require considerable analog overhead while potentially locking to sub-optimal detuning points due to indirect estimation of the modulation depth [50]–[52].

The proposed algorithm addresses these limitations by using a code-based calibration and a lightweight electrical feedback loop that directly identifies and maintains the optimal modulation point without relying on external monitoring or complex analog circuitry. The overall structure and operation are detailed in the following section 3.3.2.

Table 3-2

Comparison of representative temperature control schemes for microring modulators

Category	**Temp Sensor-Based [48]**	**Bit Statistics-Based [49]**	**Insertion-Loss Based [50]–[52]**
Sensing Target	On-chip temp. sensor	Bit-level statistical average	Insertion loss ratio
Feedback	PID control	Digital + LPF	Bang-bang
Pattern Dependence	None	Low	None
Laser Drift Tolerance	No	Partial (statistical tracking)	Yes (ratio sensing)
Analog Hardware	Temp sensor, PD	MPD, TIA	2× PDs, 2× TIAs
Maximum OMA Accuracy	Accurate	Moderate	Inaccurate

3.3.2 Proposed Code-Based Temperature Control Algorithm

The proposed temperature control algorithm is composed of four sequential phases: coarse sweep, fine sweep, reference setting, and locking. Each stage plays a distinct role in identifying and maintaining the optimal resonance condition of the MRM. The full control flow is illustrated in Fig. 3-15.

In the coarse sweep phase, the controller scans a broad range of heater DAC values while alternately transmitting two predefined calibration patterns, '1110' and '0001'. These patterns are selected to emphasize either logic 1 or logic 0 levels and will be discussed in more detail in the next section. For each DAC value H, the average optical output power corresponding to each pattern is measured: $P_{\mathrm{opt},1110}(H)$, $P_{\mathrm{opt},0001}(H)$

The difference between the two is then computed:

$$\Delta P_{\mathrm{opt}}(H) = P_{\mathrm{opt},1110}(H) - P_{\mathrm{opt},0001}(H) \tag{3.1}$$

This difference approximates the optical modulation amplitude (OMA), allowing the system to evaluate the effectiveness of each heater setting. The heater DAC value that maximizes this differential is identified as a candidate for optimal operation. To formally express this, we use the argmax operator, which refers to the input value that yields the maximum of a given function:

$$H_{\mathrm{opt}} = arg\,max(\Delta P_{\mathrm{opt}}(H)) \tag{3.2}$$

After this coarse estimation, the fine sweep phase is initiated to refine the heater DAC value around H_{opt}. A narrower range with finer resolution is explored to improve accuracy. The same procedure is followed to compute ΔP_{opt}, and the refined heater code is selected

accordingly.

Next, the system proceeds to the reference setting phase. At the optimized heater code H_{opt}, the transmitter outputs a third calibration pattern, ‘1100’. The average optical power from this pattern is recorded as:

$$P_{\mathrm{ref}} = P_{\mathrm{opt,1100}}(H_{\mathrm{opt}}) \tag{3.3}$$

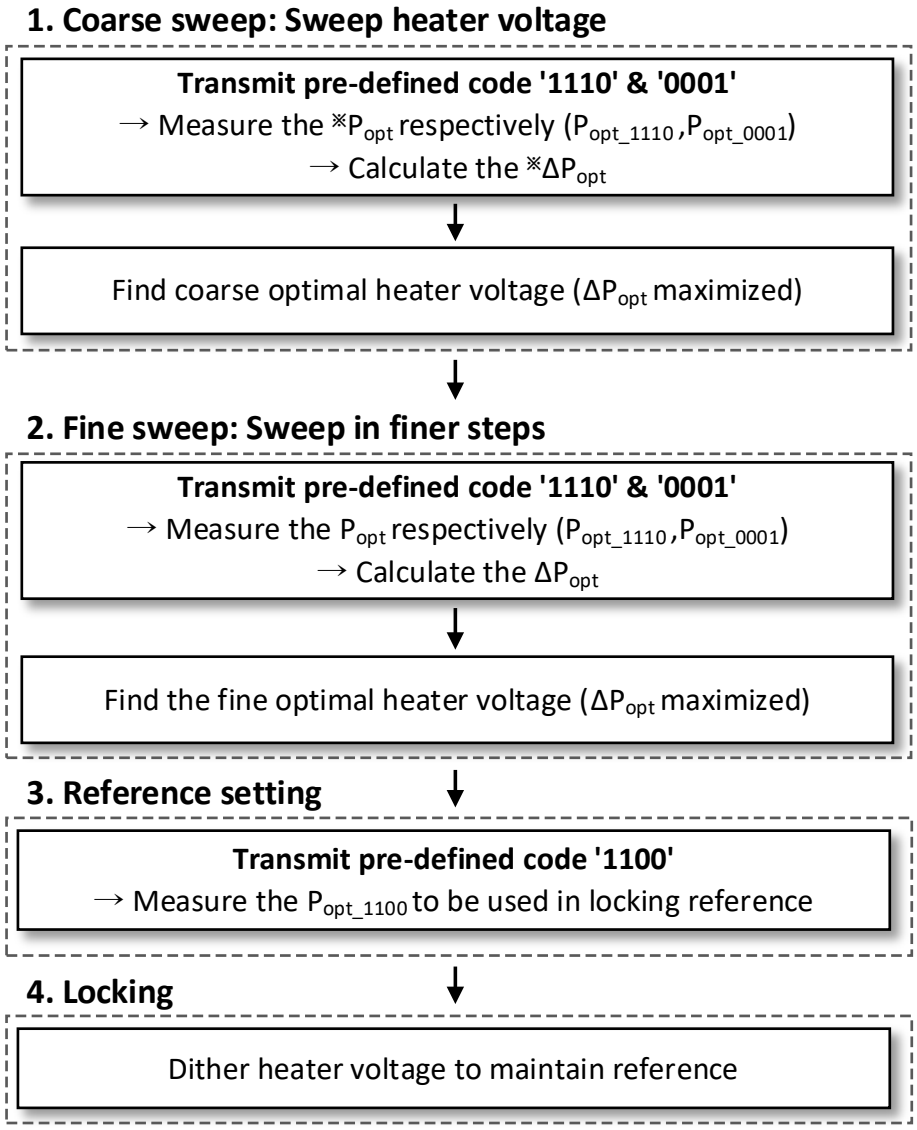
This value serves as a reference level for the feedback mechanism used during the locking phase.

In the locking phase, the system applies a small dither to the heater DAC value around H_{opt}, such that:

$$H = H_{\mathrm{opt}} \pm \Delta H \tag{3.3}$$

The resulting variation in average optical power is monitored using low-pass filtering, and the output is compared against the stored reference P_{ref}. The heater DAC is incremented when the current power falls below the reference level and decremented when it rises above. This feedback loop continuously compensates for thermal drift and maintains resonance alignment even during regular data transmission, such as when sending PRBS payloads. The mechanism relies on low-speed power monitoring and introduces minimal system overhead. The reference power level P_{ref}, which was established during calibration using the '1100' pattern, serves as a proxy for the expected average optical power during random or statistically balanced data transmission. By maintaining this level, the system ensures that the modulator stays locked to the optimal detuning point without the need for high-speed signal analysis.

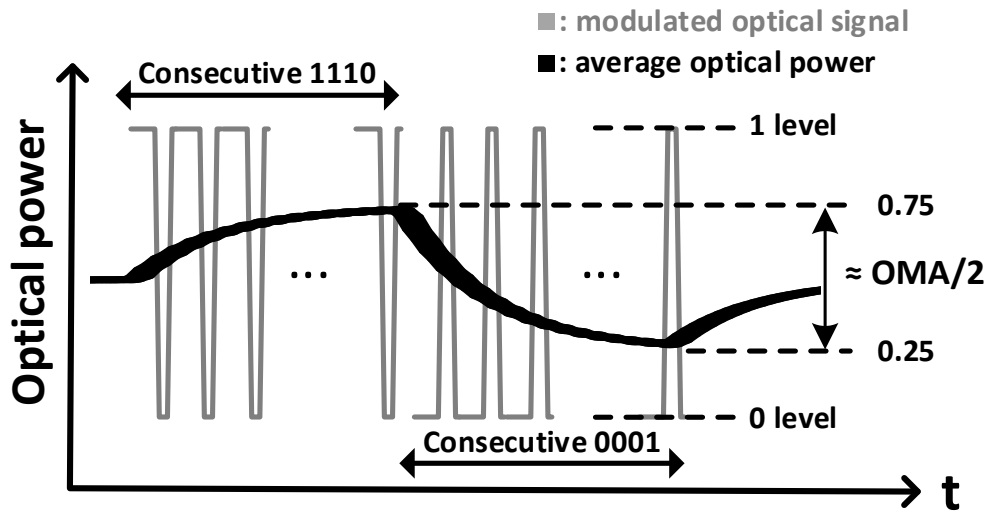
The overall flow of this control sequence is depicted in Fig. 3-15, and the relative optical output levels for each calibration pattern are illustrated in Fig. 3-16.



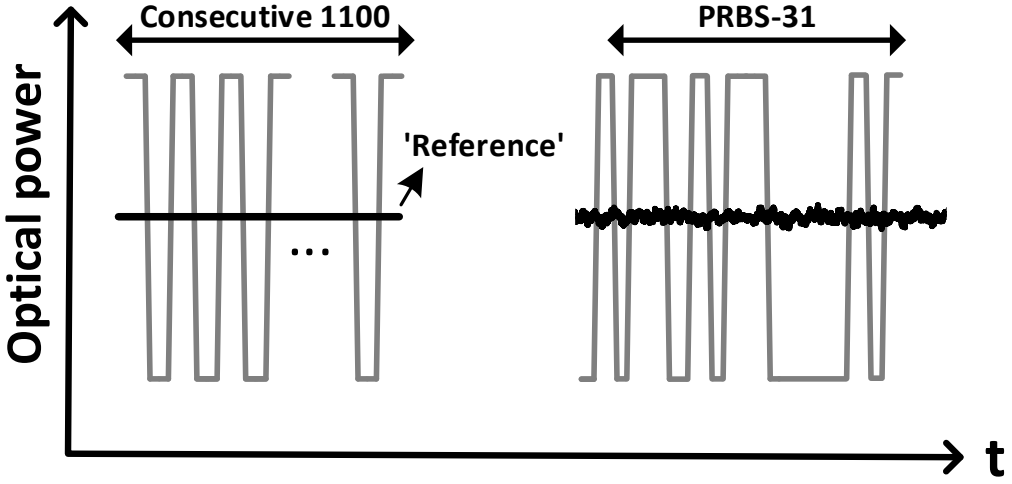
※ P_{opt} : Average optical power from the MRM drop port

※ $\Delta P_{opt} = P_{opt\_1110} - P_{opt\_0001}$

Fig. 3-15. Calibration and locking control flow of the proposed temperature control algorithm.



(a)



(b)

Fig. 3-16. Average optical power measured at the MRM output under different calibration codes. (a) Optical power under repeated ‘1110’ and ‘0001’ patterns. (b) Optical power under repeated ‘1100’ pattern and PRBS-31 input.

The effectiveness of this algorithm is strongly supported by the deliberate choice of calibration codes: '1110', '0001', and '1100'. These sequences are selected to simultaneously satisfy three essential criteria: statistical DC balance, realistic transition density, and direct estimability of the OMA, all of which are critical for robust and accurate control using only low-speed circuitry.

The first consideration in this code design is the need to maintain a stable DC baseline during calibration. In typical silicon photonic transmitters, AC coupling between the CMOS driver and the modulator eliminates static voltage offsets but also removes the DC component, making the signal susceptible to baseline drift. If calibration were performed with long sequences of the same bit, this drift would distort the measured average optical power. By alternating between '1110' and '0001', the system applies mirrored patterns with similar structure but opposite polarity. Subtracting their average optical powers cancels out common-mode offsets and low-frequency baseline wander, leading to robust differential estimation.

Secondly, the transition density of these patterns is carefully selected to mirror that of typical high-speed data transmissions. Since the microring modulator behaves as a capacitive load, dynamic power is dissipated during each bit transition, which induces dynamic-heating and shifts the resonance wavelength. This dynamic heating behavior can be approximated by the well-known switching power expression:

$$P = \alpha \cdot C \cdot V^2 \cdot f \tag{3.4}$$

where α is the the average transition probability, C is the modulator's load capacitance, V is the modulation voltage swing, and f is the bit rate. PRBS data typically yields an activity factor of $\alpha = 0.25$, assuming a random and uncorrelated sequence. The calibration codes '1110' and '0001' are selected such that, when repeated, they exhibit the same

activity factor of $\alpha = 0.25$, resulting in comparable transition density and thus matching thermal behavior. By ensuring that the thermal load during calibration closely resembles that of random data transmission, the algorithm avoids resonance misalignment due to mismatched dynamic heating conditions.

Finally, the pattern structure enables direct estimation of modulation depth using only low-speed measurements. If P_1 and P_0 denote the average optical power corresponding to logic 1 and logic 0, the time-averaged outputs for the two calibration patterns can be approximated as:

$$P_{\text{opt,1110}} \approx 0.75P_1 + 0.25P_0, \quad P_{\text{opt,0001}} \approx 0.25P_1 + 0.75P_0 \tag{3.5}$$

Taking the difference yields:

$$\Delta P_{\text{opt}} = 0.5(P_1 - P_0) = \frac{1}{2}\text{OMA} \tag{3.6}$$

Thus, the system can estimate the modulation amplitude without requiring high-speed sampling or waveform analysis.

Finally, the '1100' pattern yields an average output of:

$$P_{\text{opt,1100}} \approx 0.5P_1 + 0.5P_0 \tag{3.7}$$

This mid-level output remains stable across payload data conditions and serves as the comparison point for the feedback loop in the locking phase. As shown in Fig. 3-17, the system adjusts the heater DAC around the optimal point such that the average output power continues to track this reference during actual PRBS or random data transmission. In this way, the controller maintains resonance alignment over time using only a simple, low-speed analog comparator.

The combined effect of this calibration and locking strategy allows the proposed temperature control system to operate entirely in the electrical domain, using only digital

logic and slow analog monitoring, while achieving performance comparable to more complex optical-domain feedback methods.

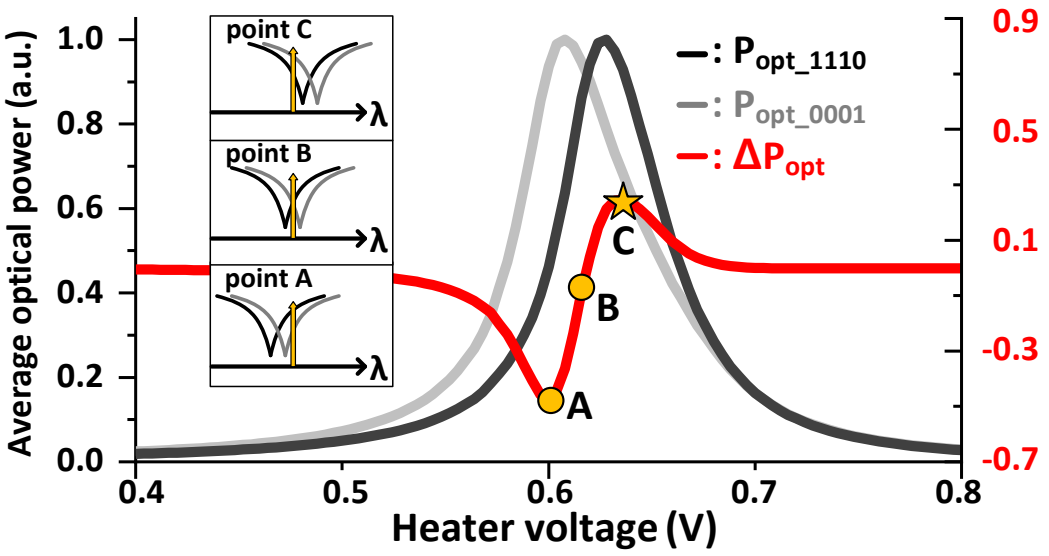


Fig. 3-17. Measured average optical power (P_{opt}) under '1110' (black) and '0001' (gray) patterns, and their difference ΔP_{opt} (red) versus heater voltage.

To validate our algorithm, a standalone PIC test is conducted using an MRM sample, and the results are presented in Fig. 3-17. Detailed information regarding the MRM sample in the PIC will be provided in Chapter 3.4. Fig. 3-17 plots the average output optical power of the MRM under repeated '1110' and '0001' patterns while sweeping the heater voltage. The dark gray line represents $P_{\mathrm{opt},1110}$ measured when the MRM is modulated with the repeating patterns of '1110', and the light gray line corresponds to $P_{\mathrm{opt},0001}$ measured under '0001' modulation. The red line indicates ΔP_{opt}, which represents the half of the OMA.

It is observed that the difference between the two curves reaches its maximum at two

distinct heater voltage settings, labeled as points A and C in the figure. While both correspond to conditions of high modulation amplitude, point C is chosen as the optimal operating point for locking, since point A lies on the right-hand side of the resonance curve in the wavelength domain, where the MRM is known to exhibit bistable behavior.

3.3.3 On-chip Controller Implementation

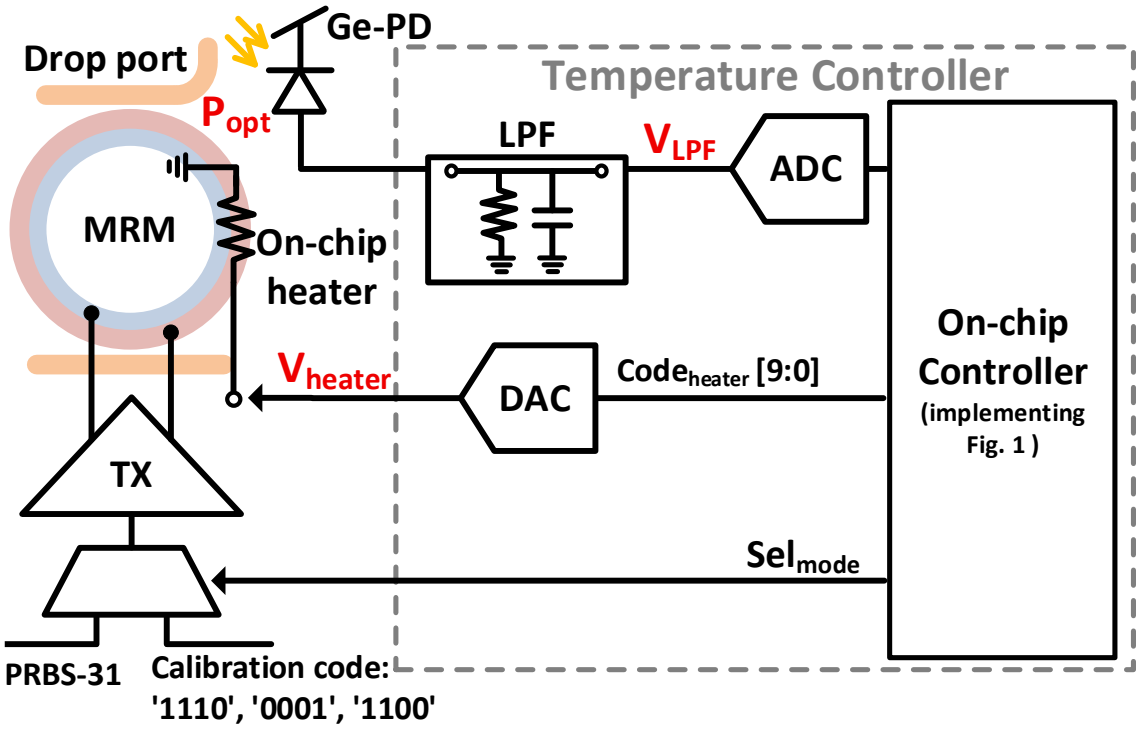


Fig. 3-18. Block diagram of the MRM temperature controller.

The overall architecture of the proposed on-chip controller is illustrated in Fig. 3-18. This controller autonomously performs both the initial calibration and real-time thermal tracking of the MRM, based on low-speed optical power measurements and digitally programmable heater control.

The average optical power from the MRM's drop port, denoted as P_{opt}, is first converted into a photocurrent by an integrated on-chip photodetector. This photocurrent passes through a LPF, which extracts the slow envelope of the optical signal, and generates a voltage signal V_{LPF} proportional to the time-averaged optical intensity.

This voltage signal is digitized by a 8-bit SAR ADC, as discussed in Section 3.2.The resulting digital value is then fed into the controller's finite state machine, which interprets the digitized power level according to the current operating mode, either calibration or tracking.

During calibration mode, the controller internally selects predefined codes ('1110' and '0001') and sends them to the transmitter via a multiplexer (MUX). The signal path is configured using a mode selection bit, $\mathrm{Sel}_{\mathrm{mode}}$, which switches between the calibration pattern and actual PRBS-31 transmission data. For each heater DAC value in the sweep, the FSM alternates between the two calibration codes, accumulates the corresponding V_{LPF} samples, and calculates ΔP_{opt}. The heater DAC value that maximizes this difference is selected as the optimal point and stored internally.

The controller then outputs a 10-bit digital value representing the selected heater DAC code, which is applied to the MRM's on-chip metal heater through a R-2R DAC. Once the calibration phase is complete, the FSM exits the calibration mode and enters the tracking phase using PRBS transmission.

In operation mode, the controller first sends the '1100' pattern once to establish a reference power level. After this initialization step, PRBS-31 data is transmitted

continuously. The average optical output during PRBS transmission is continuously monitored and compared with the stored reference value. Any deviation due to thermal drift is corrected using a dithering-based feedback loop that incrementally adjusts the heater DAC to maintain resonance alignment [53].

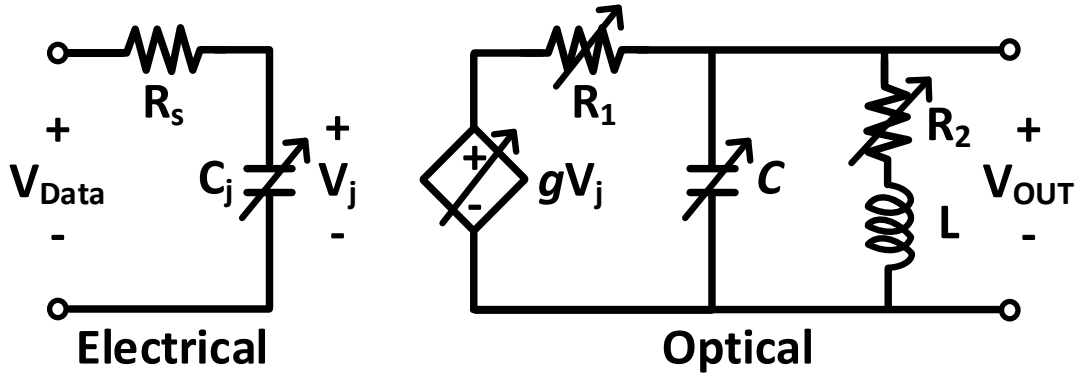


Fig. 3-19. Simplified behavioral model of the MRM including both electrical and optical components used in the gate-level simulation.

To validate the functionality of the proposed control algorithm, a gate-level simulation was carried out using a co-simulation framework that integrates a synthesized controller and an equivalent electrical model of the MRM. The model, illustrated in Fig. 3-19, incorporates voltage-dependent R, L and C to replicate the nonlinear electro-optic response of the modulator under large-signal drive conditions [23], [54]. These components are parameterized with respect to temperature, allowing the model to reproduce realistic thermal behavior, including resonance drift, over a range of operating conditions [55].

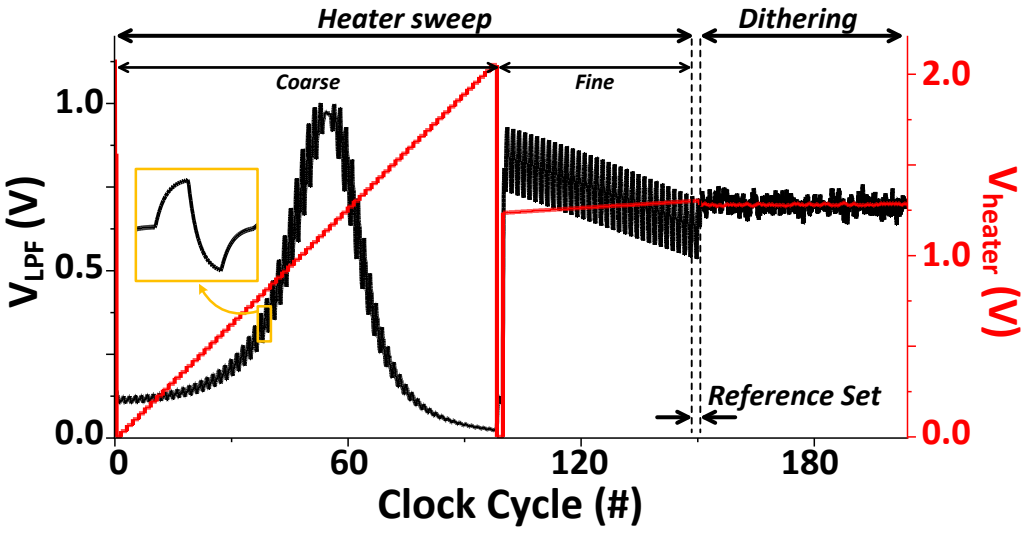
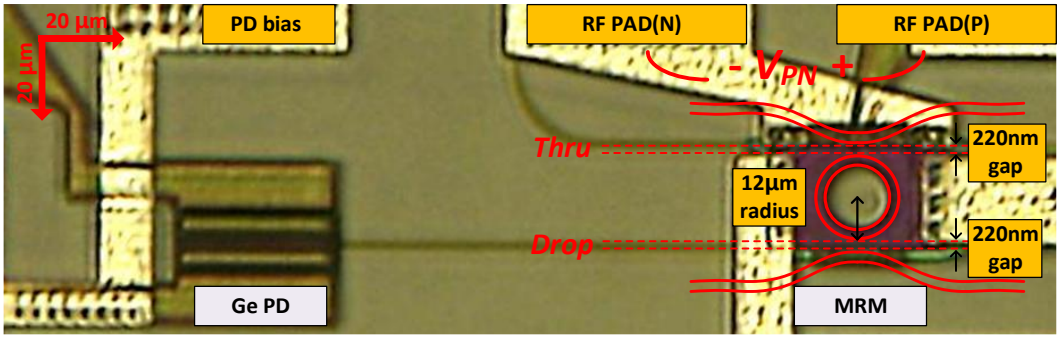


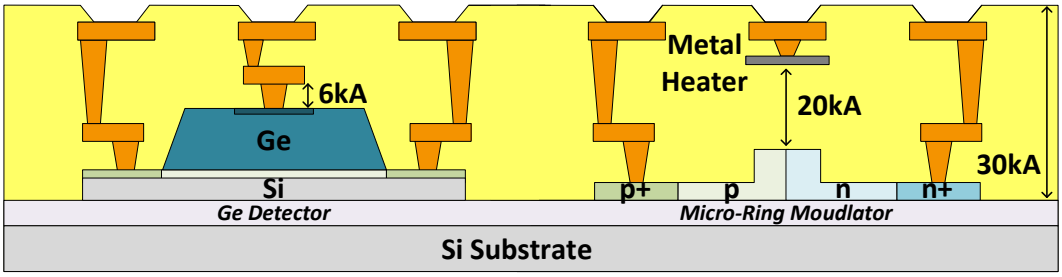
Fig. 3-20. Gate-level simulation result showing the heater voltage sweep (red) and the low-pass-filtered voltage V_{LPF}(black)

Using this setup, the full calibration and locking sequence of the controller was simulated. As shown in Fig. 3-20, the controller begins by performing a coarse sweep of the heater DAC while alternating between predefined calibration patterns. It then performs a fine sweep around the region of maximum modulation depth to accurately determine the optimal detuning point. Once the optimal heater code is selected, a reference optical power level is established using a known calibration pattern. The simulation confirms that each step of the algorithm, including initial sweeping, reference setting, and real-time tracking is correctly executed by the gate-level design, demonstrating the feasibility of full on-chip operation.

3.4 MEASUREMENT RESULTS



(a)

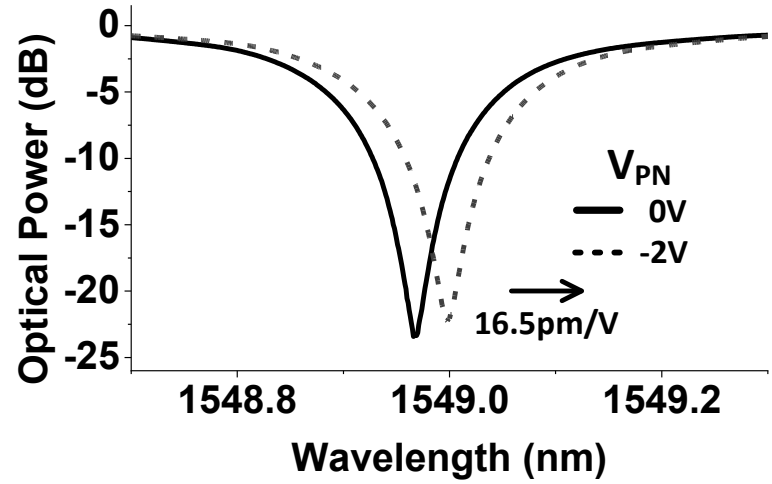


(b)

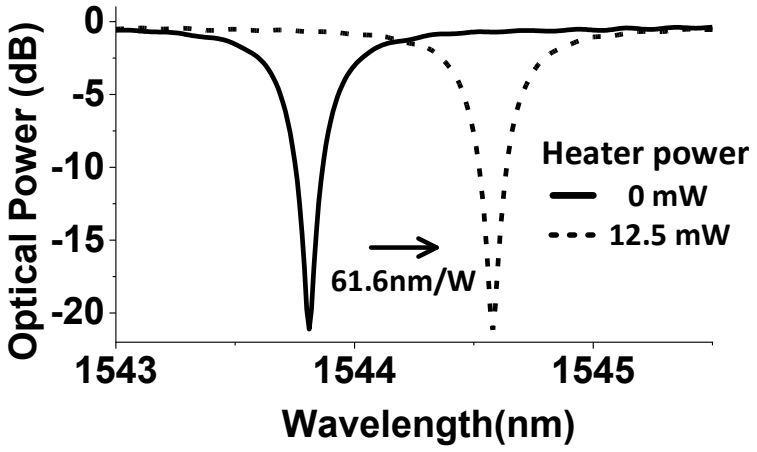
Fig. 3-21. Micrograph and cross-sectional view of the fabricated PIC integrating a micro-ring modulator and germanium photodetector.

To validate the behavior of individual photonic devices prior to full system integration, standalone measurements were first conducted on a fabricated silicon PIC including the MRM and the germanium-photodetector (Ge-PD). The optical micrograph and cross-sectional structure of the fabricated PIC are shown in Fig. 3-21(a) and Fig. 3-21(b), respectively. The MRM has a 12-µm radius and is side-coupled to a bus waveguide with a

220-nm gap. A metal heater is integrated above the ring to enable fine thermal tuning of its resonant wavelength. The Ge-PD enables local monitoring of the modulated optical signal from the drop port, which is critical for enabling the feedback control scheme.



(a)



(b)

Fig. 3-22. Measured optical transmission spectra of the MRM under reverse bias and heater power.

The optical characteristics of the MRM were measured to characterize both electro-optic and thermo-optic tuning behavior. Fig. 3-22(a) shows that the resonance wavelength of the MRM shifts toward longer wavelengths as the reverse bias increases, with a measured tuning efficiency of 16.5 pm/V. Fig. 3-22(b) shows the impact of thermal tuning by applying heater power up to 12.5 mW. A substantial red shift is observed with a tuning efficiency of approximately 61.6 pm/mW.

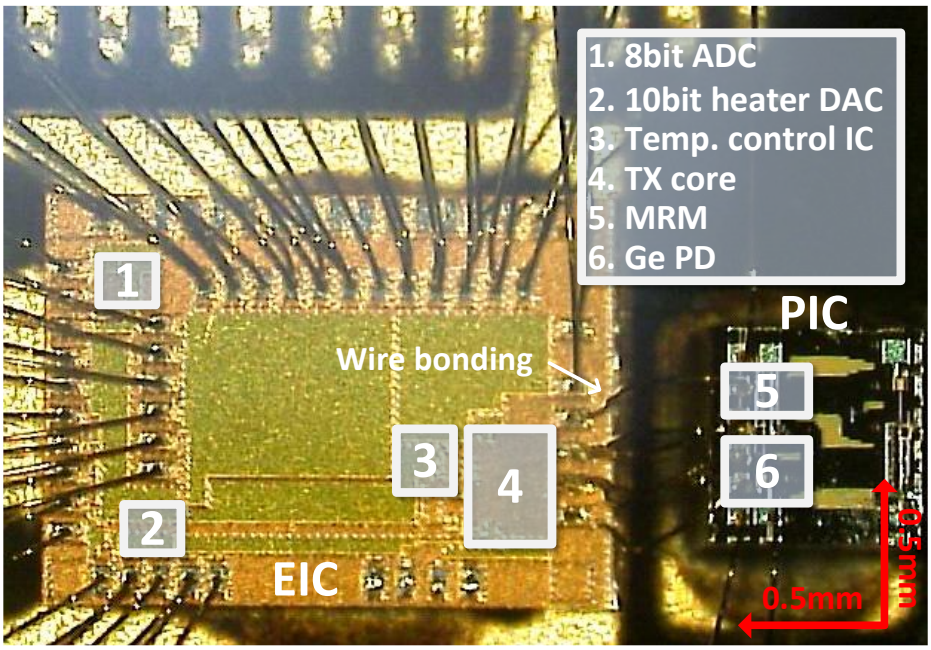


Fig. 3-23. Die photograph of the hybrid-integrated 1-channeloptical transmitter

Fig. 3-23 shows the die micrograph of the fabricated hybrid transmitter, consisting of an EIC and a PIC. The EIC is fabricated in a 28-nm CMOS process and includes the 8-bit ADC, 10-bit DAC for heater control, digital controller for temperature calibration and locking, and the TX core. The PIC, fabricated via the AMF 220-nm silicon photonics platform, integrates a MRM and a Ge-PD. Both chips are wire-bonded for hybrid

integration, enabling compact and efficient electro-optic co-design.

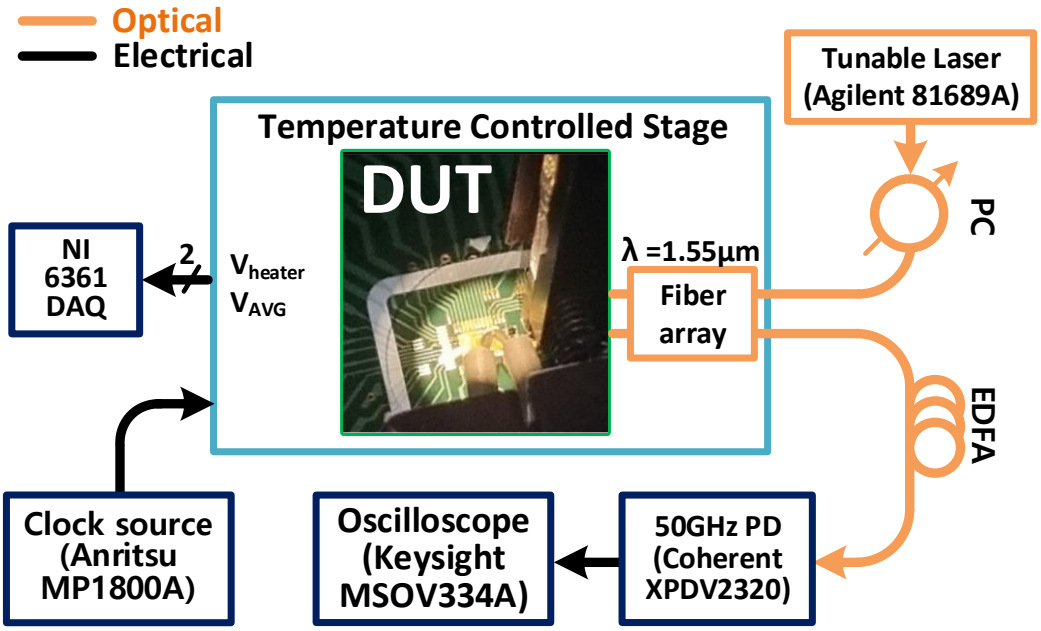


Fig. 3-24. Measurement setup.

Fig. 3-24 illustrates the optical and electrical measurement setup used to evaluate the proposed hybrid transmitter. A tunable laser (Agilent 81689A) provides a 1550-nm optical carrier, which is coupled into the PIC using a fiber array and grating couplers. The modulated optical output is amplified with an EDFA and converted to an electrical signal using a 50-GHz photodetector (Coherent XPDV2320), before being observed on a high-speed oscilloscope (Keysight MSOV334A). An Anritsu MP1800A clock generator drives the PRBS data. The packaged chip is mounted on a temperature-controlled stage, and both the heater voltage(V_{heater}) and LPF output voltage (V_{LPF}) are monitored via a NI 6361 DAQ interface.

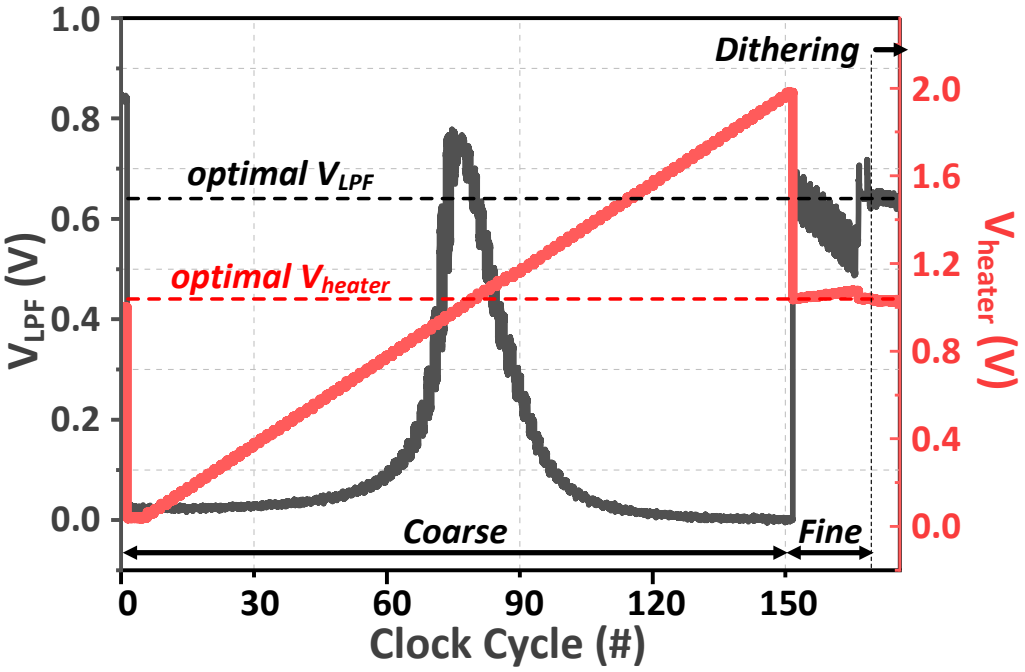
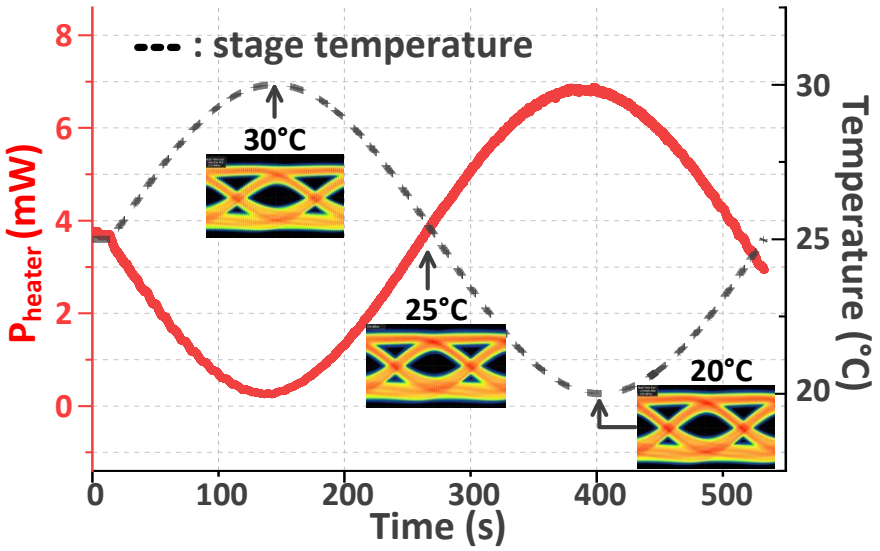


Fig. 3-25. Experimental validation of calibration and locking accuracy.

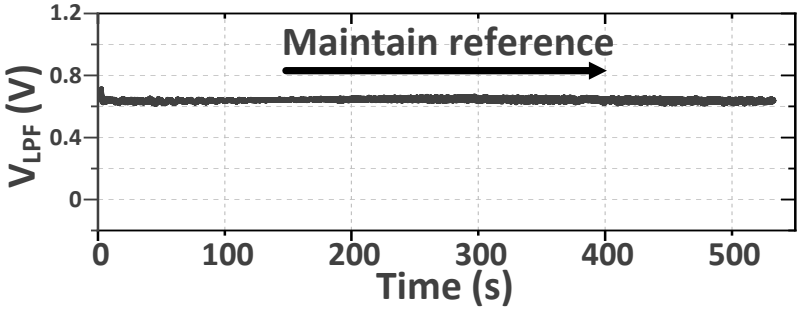
Fig. 3-25 presents the measured waveforms of V_{LPF} and V_{heater} during the calibration and locking sequence. The controller initially performs a coarse heater sweep from 0 V to 2 V, followed by a fine sweep near the peak region to locate the optimal heater code that maximizes the optical modulation amplitude. Once the optimal point is found, the controller transmits a '1100' calibration pattern to establish a reference power level and then transitions to dithering mode for real-time thermal tracking.

The black and red dotted lines in the figure indicate baseline values of V_{LPF} and V_{heater}, respectively, which were manually identified in an offline measurement by sweeping the heater and observing the maximally open eye diagram. The controller's output closely aligns with these baseline references, confirming the accuracy and reliability of the proposed calibration and feedback scheme. Furthermore, the temporal behavior of

the controller and the final locked values agree with the gate-level simulation results presented in Fig. 3-20, validating both the algorithm and its circuit implementation.



(a)

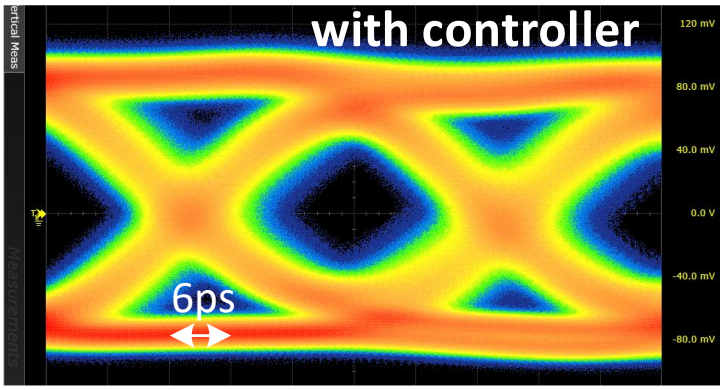


(b)

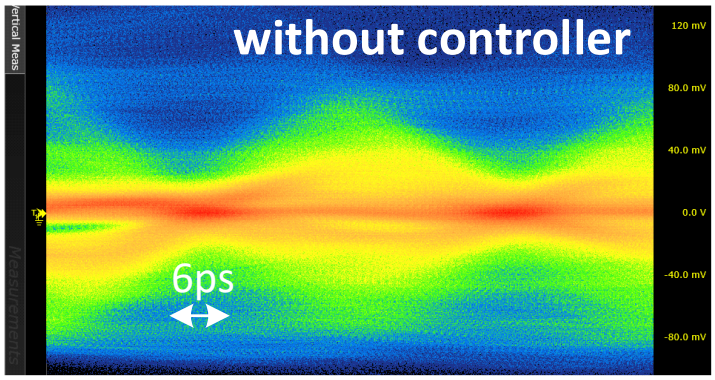
Fig. 3-26. Experimental demonstration of the on-chip temperature control. (a) On-chip heater power (P_{heater}) response to sinusoidal variation of external stage temperature from 20 °C to 30 °C. (b) Corresponding average optical power (V_{LPF}) maintained at the reference level during the external temperature variation.

Fig. 3-26 shows the dynamic response of the proposed controller under external thermal stress, validating its ability to maintain optimal modulation in real-time. During this experiment, the chip stage temperature is sinusoidally varied between 20°C and 30°C over a duration of approximately 500 seconds, while the controller operates in dithering mode. As shown in Fig. 3-26(a), the heater voltage V_{heater} (red solid line) actively tracks the inverse of the applied temperature fluctuation (gray dotted line), increasing as the ambient temperature decreases and vice versa. This behavior confirms that the controller compensates for thermal variations by adjusting the heater input to maintain resonance alignment.

Fig. 3-26(b) presents the corresponding variation of the average optical power V_{LPF}, which remains stably locked to the calibrated reference level despite the external disturbance. The observed stability demonstrates that the dithering-based feedback effectively preserves the optimal modulation condition without requiring high-speed feedback or off-chip monitoring. These results confirm that the proposed control scheme provides reliable, autonomous temperature compensation.



(a)



(b)

Fig. 3-27. Measured 32-Gb/s eye diagrams under an external temperature variation from 20 °C to 30 °C: (a) with the temperature controller enabled, and (b) with the controller disabled.

Fig. 3-27 presents the measured eye diagrams under a 32-Gb/s PRBS-31 data transmission when the chip is subjected to thermal variation between 20 °C and 30 °C. In Fig. 3-27(a), the controller is enabled and dynamically compensates for the thermal drift using the dithering-based locking scheme. As a result, a clearly open eye is maintained, demonstrating stable modulation and precise resonance alignment. In contrast, Fig. 3-27(b)

shows the eye diagram measured under the same temperature fluctuation but with the controller disabled. The eye becomes significantly closed due to the shift in the modulator's resonance wavelength, confirming that without active temperature control, the MRM can no longer be properly driven, as the resonance misalignment prevents effective modulation.

Table 3-3 provides a comparison between the proposed transmitter and recently reported optical TXs with integrated temperature control schemes.

Table 3-3

Comparison Table of the proposed TX

	This work	**[56]**	**[48]**	**[49]**	**[50]**	**[51]**
Integration	Wire-bonded	Wire-bonded	Monolithic	Monolithic	Wire-bonded	3D Integration
EIC process	28nm CMOS	250nm BiCMOS	250nm BiCMOS	45nm CMOS SOI	65nm CMOS	28nm CMOS
PIC process	220nm SOI				130nm SOI	Custom Si
Modulation	NRZ	NRZ	NRZ	NRZ	NRZ	PAM-4
Laser Band	C (1550nm)	C (1550nm)	C (1550nm)	NIR (1180nm)	C (1550nm)	O (1310nm)
TX Swing (V_{pp})	2	[1]N/A	3	1.2	4.4	3.2
Data rate (Gb/s)	32	25	25	5	25	112
Integrated thermal control	Yes	No (Off-chip PD)	Yes	Yes	Yes	Yes
Thermal control scheme	Average power with coded -based pattern	OMA monitor w/ power detector	OMA monitor w/ power detector	Closed-loop bit-statistics	Average power	Average power
Max. OMA optimization	Yes	Yes	Yes	Yes	No	No

[1]Not applicable

3.5 CONCLUSION

In Chapter 3, a 32-Gb/s silicon MRM transmitter with an integrated code-based temperature controller has been successfully demonstrated. The primary contributions of this work include the proposal of DC-balanced calibration codes optimized for low-speed optical monitoring and the design of a compact on-chip controller capable of autonomous resonance alignment and thermal tracking. The system achieves stable operation by calibrating the heater DAC value that maximizes the OMA, and continuously maintaining this condition through a dithering-based feedback loop. All control operations are performed without high-speed optical signal processing or external monitoring, which makes the approach highly scalable and energy-efficient.

Experimental results confirm that the proposed scheme effectively compensates for ambient temperature variations. It maintains open eye diagrams and consistent optical output even under a ±5 °C thermal disturbance. While the current prototype exhibits certain limitations in calibration speed and temperature range, these are attributed to hardware constraints, such as ADC resolution, heater drive capability, DAC linearity, and the thermal efficiency of the MRM heating structure rather than inherent shortcomings of the control algorithm itself. These aspects can be significantly improved through circuit-level enhancements in both the PIC and EIC, indicating promising potential for future scalability.

CHAPTER 4 Design of a 224-Gb/s PAM-4 WDM Transmitter with OMA and RLM Calibration

In this chapter, the transmitter architecture introduced in Chapter 3 is extended to increase overall data throughput. This is achieved by combining two key strategies. First, the modulation format is upgraded from NRZ to PAM-4. Second, the system is scaled from a single-channel transmitter to a four-channel WDM transmitter. These two changes enable an aggregate data rate of 224 Gb/s by operating four channels at 56 Gb/s each.

To implement WDM, four MRMs are cascaded along a single bus waveguide. Each ring is designed with a slightly different radius. This ensures that each MRM resonates at a distinct wavelength within the free spectral range and allows independent modulation of four optical carriers. The cascaded structure improves bandwidth density but introduces additional challenges such as inter-ring thermal coupling and resonance misalignment. These issues require precise control of each ring's operating point.

The use of PAM-4 modulation increases the number of signal levels from two to four. As a result, the signal becomes more sensitive to amplitude imbalance and nonlinearity. OMA alone is not sufficient to characterize signal quality. In PAM-4 systems, RLM becomes a critical factor in determining the uniformity of signal levels and overall eye quality. Even when OMA is high, poor RLM can cause eye closure and lead to increased bit errors.

To address these challenges, this chapter presents the design of a four-channel PAM-4 WDM transmitter that includes an on-chip code-based calibration controller. This controller performs simultaneous optimization of both OMA and RLM.

4.1 WDM TRANSMITTER ARCHITECTURE

Fig. 4-1 shows the overall block diagram of the EIC for the four-channel PAM-4 WDM transmitter. The EIC is composed of three functional paths: the control path, the data path, and the clock path.

Each path is digitally coordinated through the on-chip controller, which enables both OMA locking and RLM optimization across all four channels.

In the control path, a four-channel MRM controller manages the wavelength calibration and signal linearity of each MRM.

The monitor photodiode output is amplified by a transimpedance amplifier (TIA) and digitized by an 8-bit successive-approximation ADC. The resulting digital code is processed by the MRM controller, which determines the optimal heater bias for each ring and updates it through a 10-bit DAC. This interface operates based on the same principle described in Chapter 3, where the closed-loop control stabilizes the resonance wavelength of each MRM against temperature variations and process drift. The overall structure and signal flow are maintained, but the calibration system in this design is extended to support four channels.

In addition to heater control, the MRM controller adjusts the driver strength for each channel using two independent 4-bit digital control words ($w_{\mathrm{PU}}$and w_{PD}) that define the pull-up and pull-down weights of the SST driver. These parameters regulate the pull-up and pull-down strengths of the segmented SST driver, allowing the controller to fine-tune the PAM-4 signal levels and perform RLM optimization together with OMA locking.

The data path generates and delivers the high-speed PAM-4 signals to the MRMs. A built-in PRBS31 generator produces the test sequence for calibration and measurement.

The generated data are retimed and serialized through an 8:4 and 4:1 multiplexer chain to achieve a 56-Gb/s data rate per channel.

The SST driver receives three thermometer-encoded input signals (T_{A}, T_{B}, and T_{C}) that represent the PAM-4 data levels and converts them into three discrete output voltages for optical modulation.

An active-resistance network is implemented at the MRM anode and cathode to stabilize the DC bias and suppress low-frequency drift. The resistance value is designed to be sufficiently large so that DC wander remains within an acceptable range during both calibration and data transmission. This design maintains a stable DC operating point and prevents pattern-dependent baseline drift during PAM-4 operation. The detailed circuit implementation and resistance design method are described in Section 4.1.2.

The Sel_{mode} signal from the controller determines whether the channel operates in calibration or normal data transmission mode.

The clock path distributes a low-jitter reference clock to the controller, serializer, and driver circuits. An external clock input is processed by a global QEC, DCC, and digitally controlled delay line (DCDL) block to generate synchronized clock phases. Since the physical routing of the clock signal can vary slightly among the four transmitter channels, each channel also includes local DCC, QEC, and DCDL control circuits that allow fine phase and duty adjustment. This hierarchical clock correction structure minimizes inter-channel skew and ensures consistent timing alignment across the multi-channel transmitter.

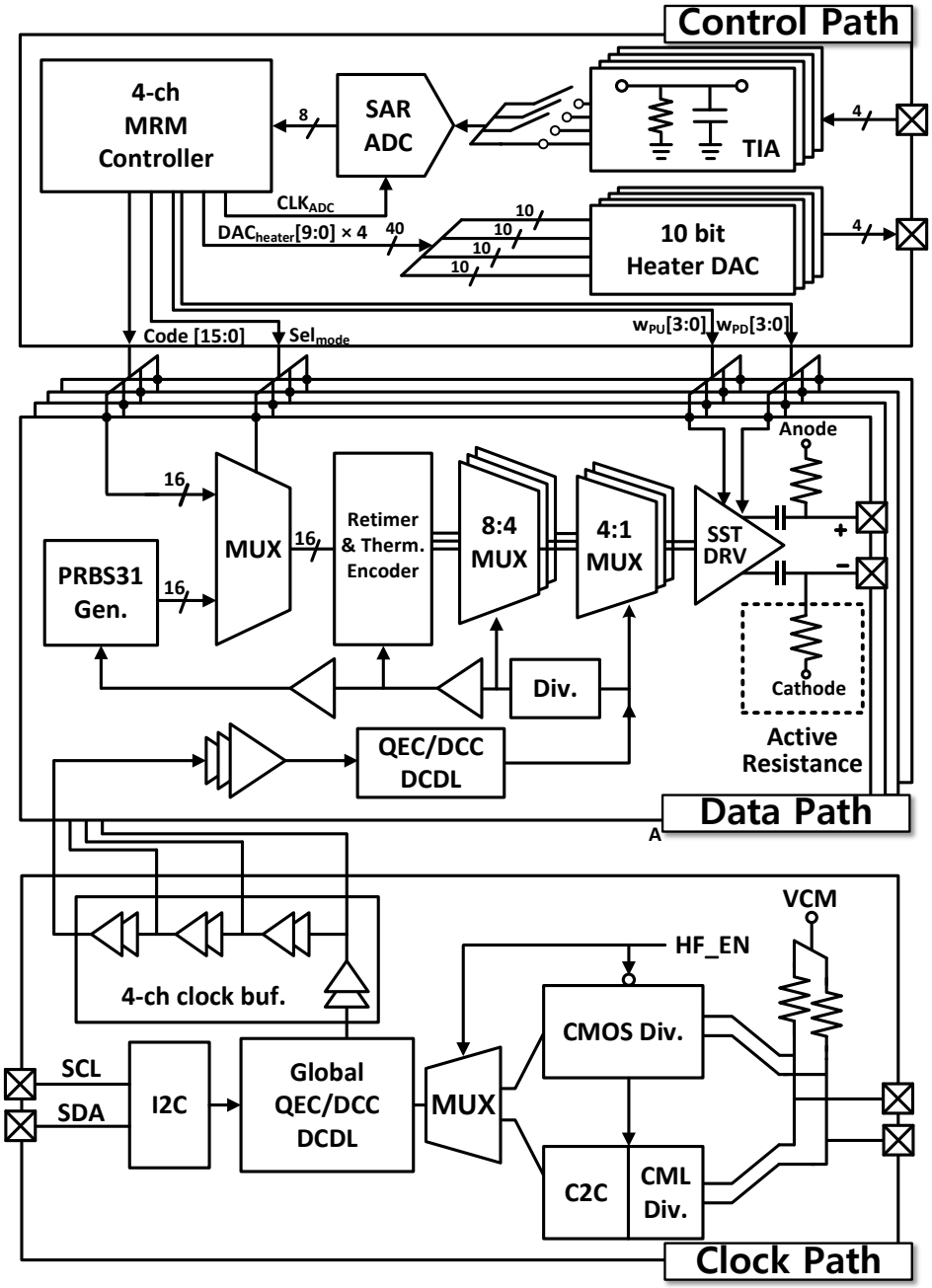


Fig. 4-1. Overall block diagram of the 4-channel EIC.

4.1.1 PAM-4 Driver Structure and Thermometer Encoding

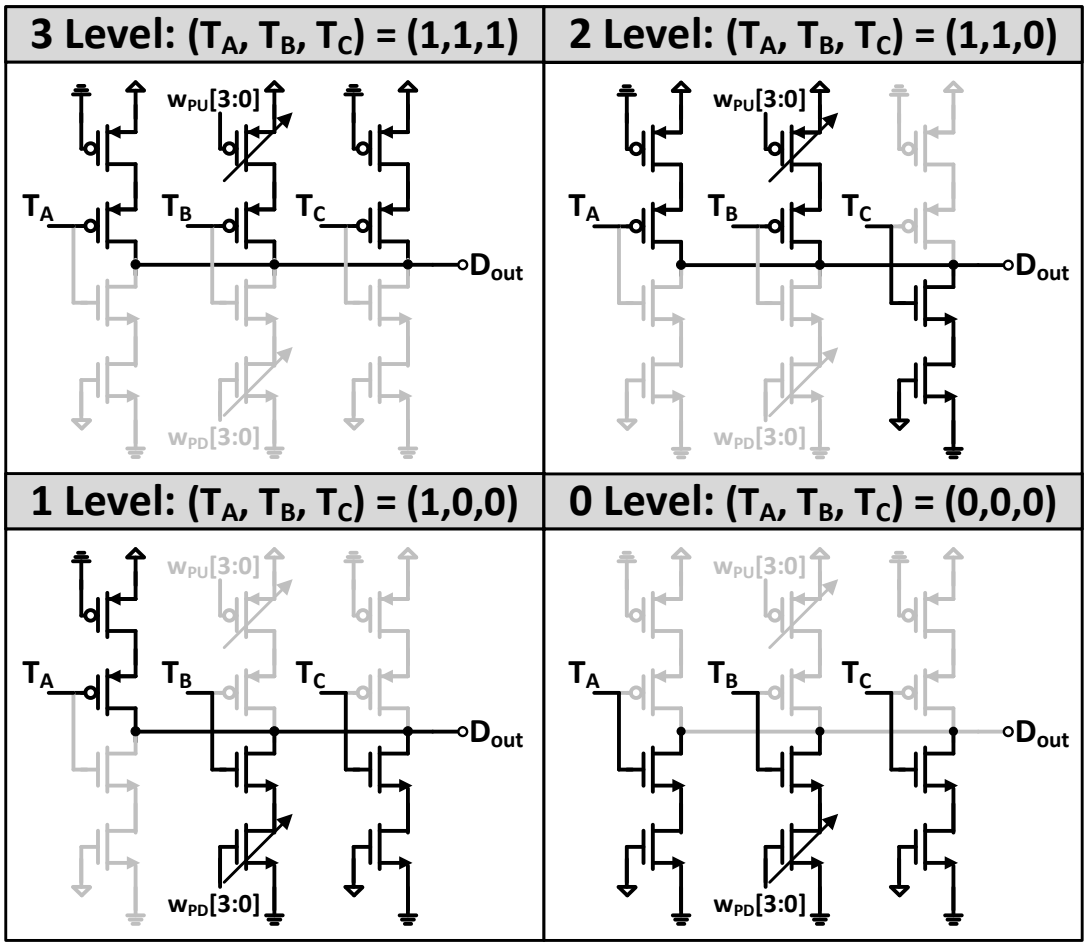


Fig. 4-2. PAM-4 driver operation based on thermometer-encoded inputs (T_A, T_B, T_C) and tunable driver weights (w_{PU}, w_{PD}) for RLM adjustment.

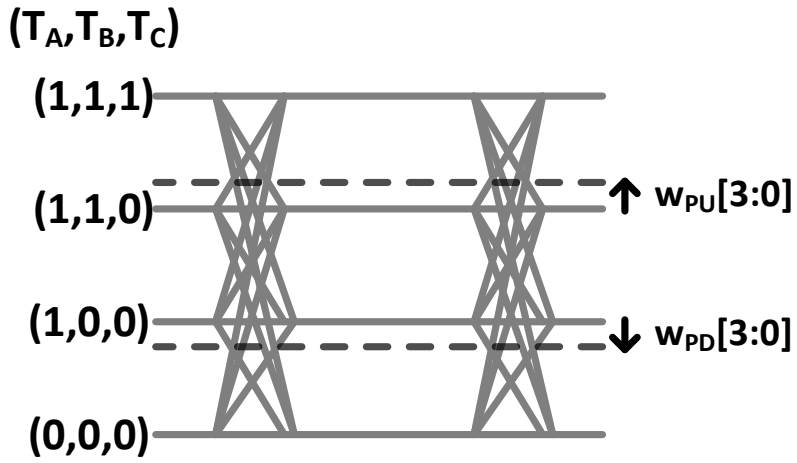


Fig. 4-3. Conceptual diagram showing PAM-4 level formation and the effect of w_{PU} and w_{PD} tuning on the middle signal levels.

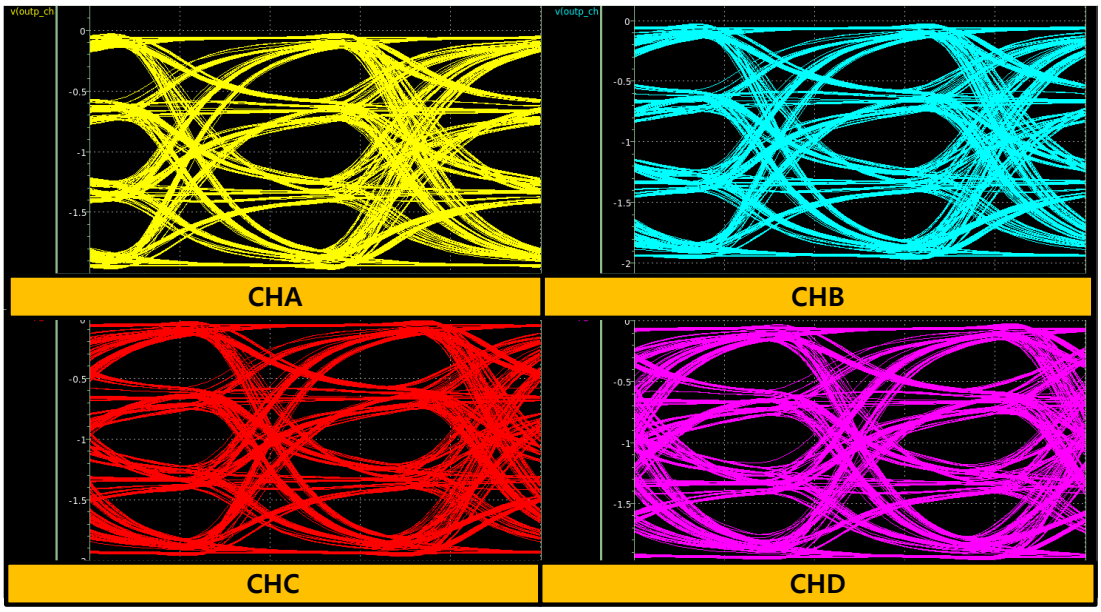


Fig. 4-4. Post-layout simulation showing 56-Gb/s eye diagrams of four WDM channels with the PU/PD driver code set to 1000

Fig. 4-2 illustrates the operation of the SST driver and its thermometer-encoded input configuration. The driver receives three input control signals (T_{A}, T_{B}, T_{C}) generated by the thermometer encoder. Each input combination corresponds to one of the four PAM-4 output levels.

This encoding scheme ensures monotonic switching and avoids glitches that could occur with binary-coded inputs at high speed.

Depending on the input combination, different numbers of PMOS and NMOS devices are turned on, and the resulting ratio of pull-up to pull-down driving strength determines the output voltage level. In this way, the four PAM-4 levels are generated by the relative on-resistance of the transistor stacks rather than by discrete voltage sources.

Each driver branch includes adjustable weighting networks that are controlled by two independent 4-bit digital control bits, $w_{\mathrm{PU}}[3:0]$ and $w_{\mathrm{PD}}[3:0]$. These control codes define the pull-up and pull-down strengths of the SST driver, allowing fine adjustment of the intermediate levels during RLM calibration.

As shown in Fig. 4-3, increasing w_{PU} activates additional pull-up transistors, which reduces the pull-up resistance and raises Level 2. Conversely, increasing w_{PD}turns on more pull-down transistors, decreasing the pull-down resistance and lowering Level 1. Through this tuning process, the controller can adjust the spacing between the middle PAM-4 levels while keeping the outer levels fixed, thereby optimizing the RLM for each channel. This structure provides a simple and effective way to control level symmetry without additional analog bias circuitry, enabling precise eye-level alignment in high-speed PAM-4 signaling. Based on this driver structure, we design a controller that compensates for the nonlinearity of the MRM by dynamically adjusting the intermediate levels. The detailed control algorithm of this controller is described in Chapter 4.2.

In addition, Fig. 4-4 presents the post-layout 56-Gb/s eye diagrams obtained with the

PU/PD weights set to the baseline code (1000). Even under this reduced-strength configuration, all four channels maintain open eyes, indicating that the driver and interconnect parasitics provide sufficient bandwidth for high-speed operation.

4.1.2 Active Resistance Network

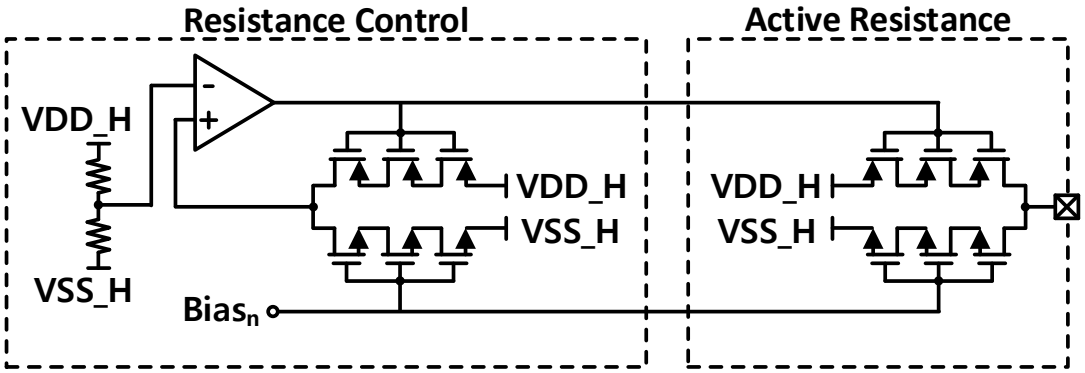


Fig. 4-5. Circuit diagram of the resistance control circuit and active resistance core.

To suppress DC wander at the transmitter output, a high-impedance biasing network is required at the anode and cathode of the MRM.

If a passive resistor were used, a very large resistance value would be needed, which would occupy significant area and introduce parasitic capacitance that degrades high-speed performance. To overcome this limitation, an active resistance circuit is adopted, as shown in Fig. 4-5.

The active resistance consists of two functional blocks: a resistance control circuit and an active resistance core. The input control voltage $\mathrm{Bias_n}$ is applied to the NMOS transistor network to adjust its effective resistance. As $\mathrm{Bias_n}$ increases, the conduction of the NMOS stack becomes stronger, and the equivalent resistance decreases. A feedback loop with an operational transconductance amplifier (OTA**)** regulates the PMOS gate bias such that the output node is maintained approximately at the midpoint between 'VDD_H'

and ‘VSS_H’, ensuring a high-impedance bias condition.

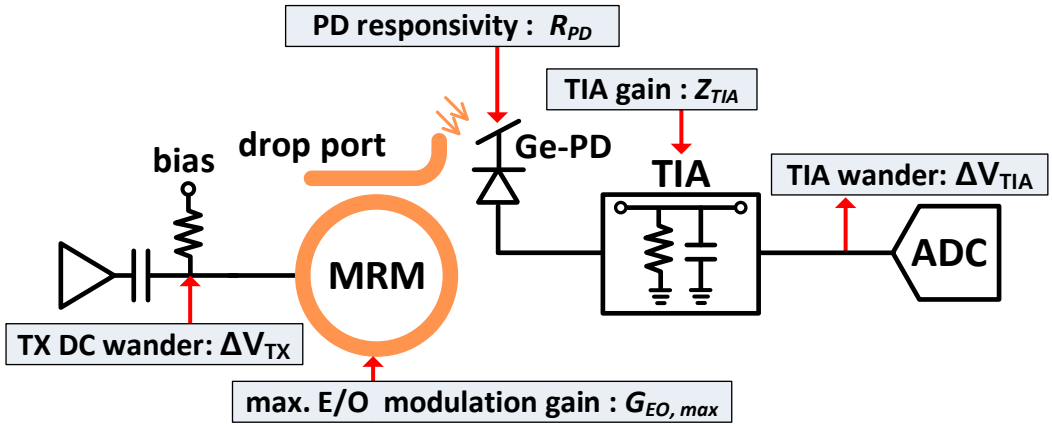


Fig. 4-6. Circuit diagram of the resistance control circuit and active resistance core.

Through this mechanism, the PMOS devices operate in a stable bias region, and the overall circuit behaves as a tunable high-value resistor. The allowable TX DC wander is determined from the ADC resolution and the maximum allowable TIA wander.

For an 8-bit ADC with a 1-V input range, the least significant bit (LSB) corresponds to:

$$V_{\mathrm{LSB}} = \frac{1}{2^8}\,\mathrm{V} = 3.9\,\mathrm{mV} \tag{4.1}$$

To ensure measurement accuracy, the variation of the TIA output ΔV_{TIA} must remain below one LSB:

$$\Delta V_{\mathrm{TIA}} \leq V_{\mathrm{LSB}} \tag{4.2}$$

The relationship between the TIA wander and the transmitter output wander is illustrated in Fig. 4-6, which shows the optical-to-electrical signal conversion chain consisting of the modulator, photodiode, and transimpedance amplifier.

he relationship between the TIA wander and the transmitter output wander is illustrated in

Fig. 4-6, which shows the optical-to-electrical signal conversion chain consisting of the modulator, photodiode, and transimpedance amplifier.

In this model, the small change in the transmitter output bias ΔV_{TX} is converted into a variation at the TIA output according to

$$\Delta V_{\mathrm{TIA}} = G_{\mathrm{EO,max}} \times R_{\mathrm{PD}} \times Z_{\mathrm{TIA}} \times \Delta V_{\mathrm{TX}} \tag{4.3}$$

where $G_{\mathrm{EO,max}} = 5.6 \times 10^{-5}\mathrm{W/V}$, $R_{\mathrm{PD}} = 0.95\ \mathrm{A/W}$ and $Z_{\mathrm{TIA}} = 10^{3}\ \mathrm{A/W}$.

By substituting these values into Equation (4-3) and applying Equation (4-2), the allowable transmitter wander becomes

$$\Delta V_{\mathrm{TX}} \leq \frac{V_{\mathrm{LSB}}}{G_{\mathrm{EO,max}} R_{\mathrm{PD}} Z_{\mathrm{TIA}}} = 75\ \mathrm{mV} \tag{4.4}$$

To guarantee that the TX DC wander remains below 75 mV even during long repetitive data sequences such as “1110” or “0001,” the required HPF time constant is derived as

$$\tau_{\mathrm{HPF}} \geq \frac{\Delta V_{\mathrm{TX}}}{2\pi f_{\mathrm{data}} V_{\mathrm{swing}}} \tag{4.5}$$

Here, f_{data} is set arbitrary to one-fourth of the main data rate, corresponding to 3.5-GHz,

so that the algorithm remains effective even under slower operating conditions. This conservative choice ensures that the bias stabilization loop maintains proper operation across various data patterns and modulation speeds.

The parameter V_{swing} denotes the single-ended voltage swing of the SST driver output, which is 1 V in this design. For a coupling capacitance of $C_{\mathrm{HPF}} = 1\mathrm{pF}$, the required resistance can be expressed as

$$R_{\mathrm{HPF}} \geq \frac{\tau_{\mathrm{HPF}}}{C_{\mathrm{HPF}}} = 0.74\,\mathrm{M\Omega} \tag{4.6}$$

Therefore, the active resistance circuit must provide an equivalent resistance of at least 0.74 MΩ to maintain sufficient DC bias stability at the 3.5-GHz operation condition.

The post-layout simulation results shown in Fig. 4-7 confirm that the designed circuit satisfies this requirement across process corners and temperature variations.

As the control input $\mathrm{Bias_n}$ increases, the effective resistance decreases due to stronger NMOS conduction. This tunable configuration ensures that the DC wander at the transmitter output remains below the specified limit while minimizing the required chip area and parasitic capacitance.

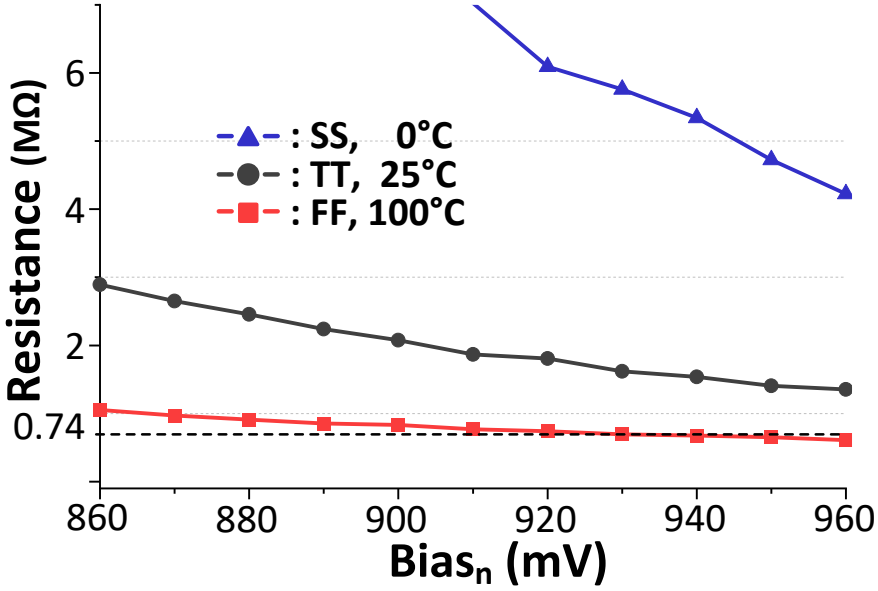
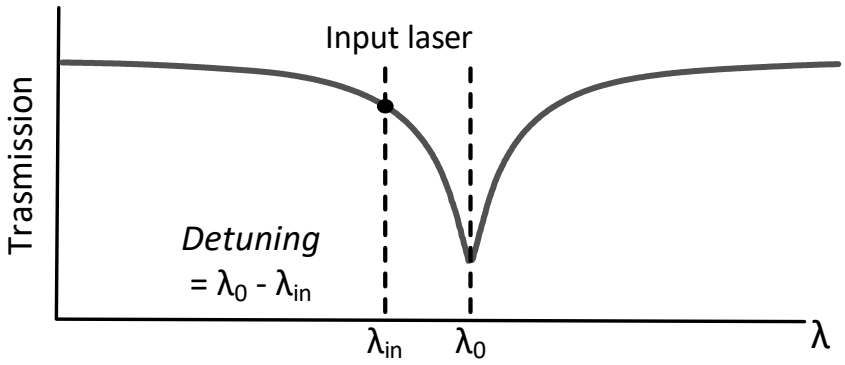
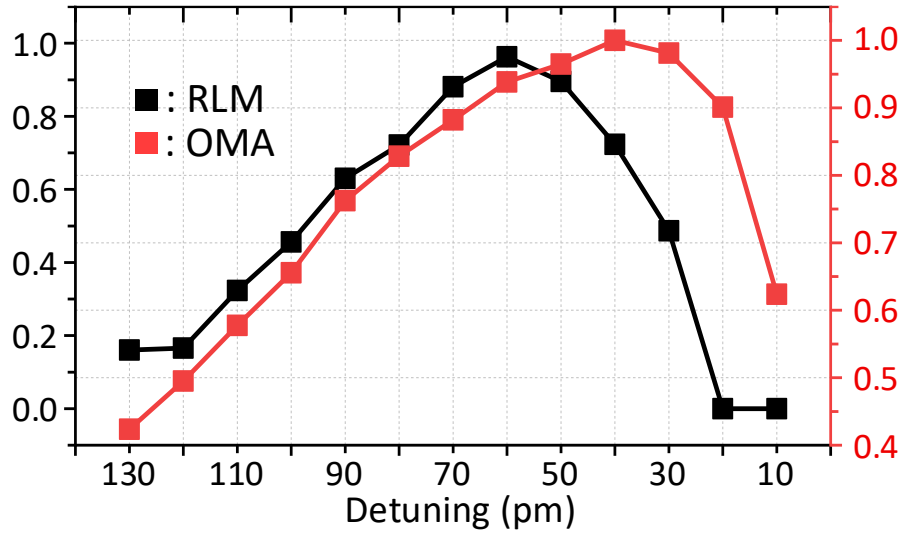


Fig. 4-7. Post layout simulated active resistance variation across process corners and temperatures with respect to the input control voltage.

4.2 DUAL-OBJECTIVE CALIBRATION CONTROL ALGORITHM



(a)



(b)

Fig. 4-8. (a) Illustration of wavelength detuning ($\lambda_o - \lambda_{in}$) and its effect on ring transmission. (b) Measured detuning dependence of OMA and RLM in the AMF 220-nm microring modulator at 56-Gb/s.

The detuning, defined as the wavelength difference between the input laser (λ_{in}) and the resonance wavelength of the modulator (λ_0), is conceptually illustrated in Fig. 4-8(a). To analyze its effect on modulation characteristics, a single micro-ring modulator fabricated in the AMF 220-nm silicon photonics platform was characterized.

The measured dependence of OMA and RLM on detuning, shown in Fig. 4-8(b), reveals that the RLM maximum point and OMA maximum detuning point occur at different detuning values. In other words, the wavelength that provides the highest OMA does not correspond to the wavelength that achieves the best linearity.

Because these two optimal points do not coincide, adjusting the heater bias alone cannot simultaneously optimize both parameters.

The proposed transmitter therefore employs a dual-objective calibration algorithm. The OMA control loop tunes the heater voltage to search for and lock the operating point that maximizes the OMA, following the same calibration principle described in Chapter 3. However, at this OMA-locked point, the PAM-4 output often shows level asymmetry because the nonlinear transfer function of the MRM distorts the intermediate levels.

To correct this distortion, the RLM control loop automatically adjusts the driver strength codes (w_{PU} and w_{PD}) to apply electrical predistortion to the PAM-4 signal, thereby compensating for the modulator nonlinearity and restoring level linearity.

Through this combined operation, the controller dynamically converges to an operating point that satisfies both OMA and RLM requirements, maintaining high modulation efficiency and balanced PAM-4 eye levels.

4.2.1 Previous RLM Control Algorithms

In previously reported microring-based transmitters, RLM control has been implemented using either electrical-domain predistortion or thermal-domain optimization, each of which exhibits inherent constraints in achieving full automation.

One approach employed a lookup-table (LUT)-based nonlinear equalizer, where the PAM-4 driver output was digitally pre-distorted to compensate for static and dynamic nonlinearities of the MRM [51].

This method effectively improved eye linearity under fixed bias conditions and reduced pattern-dependent distortion through digital correction at the transmitter output.

The heater tuning in that system was performed automatically through a thermal feedback loop, but the RLM adjustment required an offline calibration process using pre-characterized LUT data.

Because the electrical predistortion table was generated externally and independently of the optical bias loop, the RLM could not adapt to thermal drift or process variation.

Whenever the optical operating condition changed, the LUT had to be manually updated to restore level symmetry, which significantly limited the practicality of this method for continuous or multi-channel operation.

Another reported technique adopted a multi-objective thermal controller, which used photocurrent feedback from an on-chip monitor photodiode to iteratively adjust the heater bias voltage [57]. The same control variable was used to optimize multiple optical performance metrics such as extinction ratio (ER), OMA, or RLM. Such a scheme demonstrated the feasibility of autonomous optical bias tuning and RLM-oriented calibration.

However, since all objectives shared the same thermal control variable, the controller could optimize only one metric at a time. For example, when the controller was tuned to maximize OMA, the resulting RLM typically deviated from its optimal value, and vice versa. The algorithm therefore required repeated calibration cycles whenever the optimization target changed.

Moreover, because the tuning relied solely on optical bias adjustment, it could not compensate for the electrical-level mismatch originating from the driver's nonlinearity.

The thermal feedback loop also required a relatively long search time to find the optimal bias point, making it unsuitable for fast or multi-channel calibration.

In essence, the limitation of this architecture arises from its single-parameter nature, where all optical metrics must share one heater control variable.

In summary, previous RLM control schemes integrated automatic heater calibration but still relied on either manual LUT updates or single-parameter thermal tuning, both of which prevented simultaneous optimization of OMA and RLM.

The proposed transmitter eliminates these limitations by performing LUT-free, on-chip initialization that automatically determines both the OMA and RLM operating points without external training or manual calibration.

After the initial calibration, the heater bias is locked to maintain the resonance condition, ensuring stable operation of both parameters across temperature variations.

This dual-loop structure provides a unified control framework in which optical efficiency and signal linearity are autonomously established and maintained on chip, enabling stable and repeatable operation across multi-channel PAM-4 WDM transmitters.

4.2.2 Proposed RLM Control Algorithm

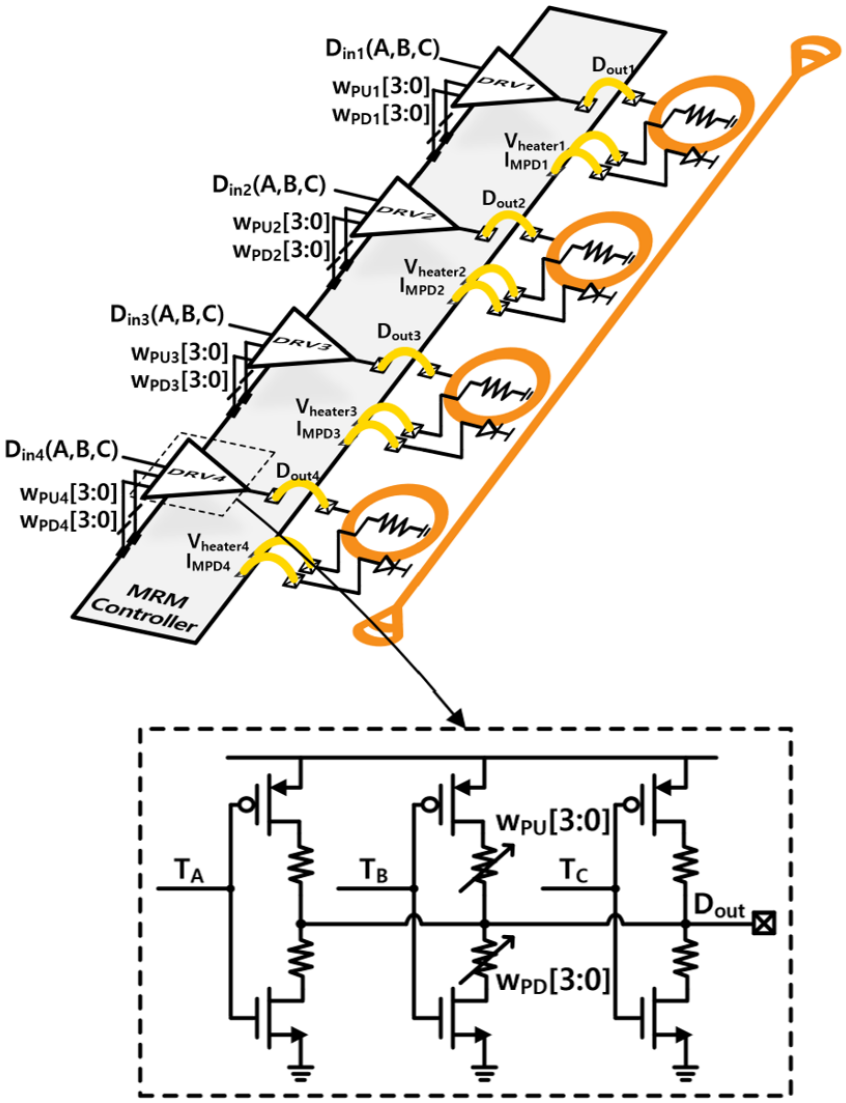


Fig. 4-9. Overall block diagram of the proposed dual-objective calibration architecture for OMA and RLM optimization.

Fig. 4-9 illustrates the overall block diagram of the proposed dual-objective calibration architecture, where a centralized MRM controller located at the bottom side manages both optical and electrical control loops for the four transmitter channels.
Each channel integrates a MRM with an embedded heater, a monitor photodiode (MPD), and a segmented PAM-4 driver composed of three binary input branches (T_{A}, T_{B}, and T_{C}). Among them, only the T_{B} branch, which determines the two intermediate PAM-4 levels, is tunable in strength. Its pull-up and pull-down transistors are digitally weighted through two independent 4-bit control codes, w_{PU}[3:0] and w_{PD}[3:0], respectively. By adjusting these codes, the controller can fine-tune the output swing of the T_{B} branch to correct level asymmetry and optimize the RLM of the transmitted signal.

The MRM controller coordinates all calibration activities within the transmitter.
It regulates the heater DAC code that determines the resonance wavelength of each microring and adjusts the driver strength codes (w_{PU} and w_{PD}) to correct RLM in the PAM-4 waveform. During the calibration process, the controller also configures the pattern generator to inject dedicated test sequences that facilitate accurate measurement of the optical modulation amplitude and level symmetry.

After completing both optical and electrical calibrations, the controller switches the transmitter from calibration mode to data-transmission mode through an internal digital multiplexer, enabling a transition without external intervention. All of these operations are integrated into a single digital control framework that sequentially addresses each of the four channels while sharing the common ADC and DAC interfaces.

During the OMA calibration phase, the controller adjusts the heater bias (V_{heater}) of each MRM to maximize the optical modulation amplitude. The photocurrent generated by the monitor PD is amplified and digitized by an 8-bit ADC, and the resulting digital value is processed by the controller to determine the heater code corresponding to the maximum

OMA, following the code-based search procedure introduced in Chapter 3. Once the optimal bias point is found, the DAC code is latched to stabilize the resonance condition, ensuring consistent optical performance under temperature variation.

After completing the OMA calibration, the controller proceeds to the RLM calibration phase, where the pull-up and pull-down weight codes of the TB branch are iteratively adjusted to equalize the middle levels of the PAM-4 waveform.

The optical signal is monitored through the same MPD, TIA, ADC path used during OMA calibration, allowing the controller to evaluate RLM without additional sensing circuitry.

By analyzing the digitized levels obtained from this shared feedback interface, the controller estimates the current RLM and updates the driver weight codes (w_{PU} and w_{PD}) until level symmetry is achieved.

This unified feedback structure simplifies implementation and ensures consistent measurement accuracy between OMA and RLM optimization.

Through this process, the calibration compensates for both the optical nonlinearity of the MRM and the electrical mismatch within the driver, effectively linearizing the overall electro-optical transfer function. When the RLM error converges within a predefined tolerance, the final codes are stored in on-chip registers, and the transmitter transitions to normal operation.

All calibration tasks, including pattern generation, bias tuning, and mode switching, are performed autonomously on chip without external DSP or host control.

Once the initialization is complete, the OMA control loop continuously maintains the optical output power at the calibrated operating point where the maximum OMA was achieved. Because the RLM optimization was performed at this same condition, by only maintaining the OMA-locked optical power level, the transmitter inherently preserves the calibrated RLM without requiring additional adjustment. This integrated dual-loop

structure enables consistent optimization of both OMA and RLM across all WDM channels, achieving self-contained and repeatable transmitter performance through a unified on-chip control framework.

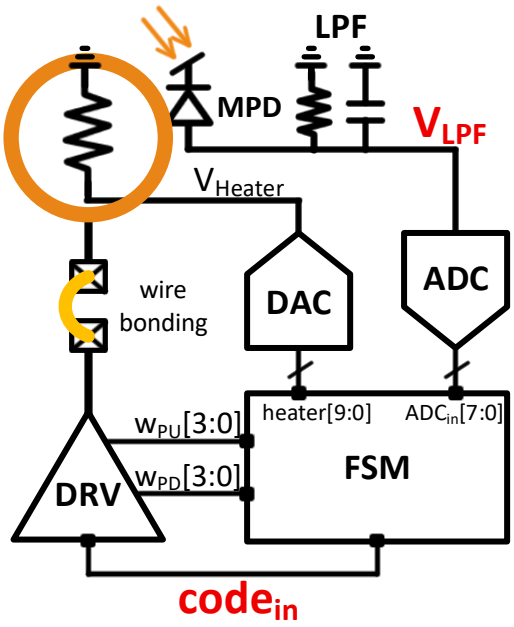


Fig. 4-10. Control interface for implementing the dual-objective OMA and RLM calibration algorithm in a single transmitter channel.

The control interface used to implement the dual-objective calibration algorithm for a single transmitter channel is shown in Fig. 4-10. The FSM coordinates the 10-bit heater DAC, 8-bit ADC, and the PAM-4 driver weight controls (w_{PU}[3:0] and w_{PD}[3:0]). During calibration, predefined digital patterns ($code_{\mathrm{in}}$) are applied to the driver, and the corresponding optical response is monitored through the integrated MPD and low-pass-filtered to produce the feedback signal (V_{LPF}). The FSM processes this feedback to update the DAC and driver weights according to the control logic described in the following

section. This diagram is provided as a reference to define the key signal and node names, such as $code_{\mathrm{in}}$, V_{LPF}, w_{PU}[3:0], and w_{PD}[3:0] used in the control algorithm illustrated in the subsequent figures.

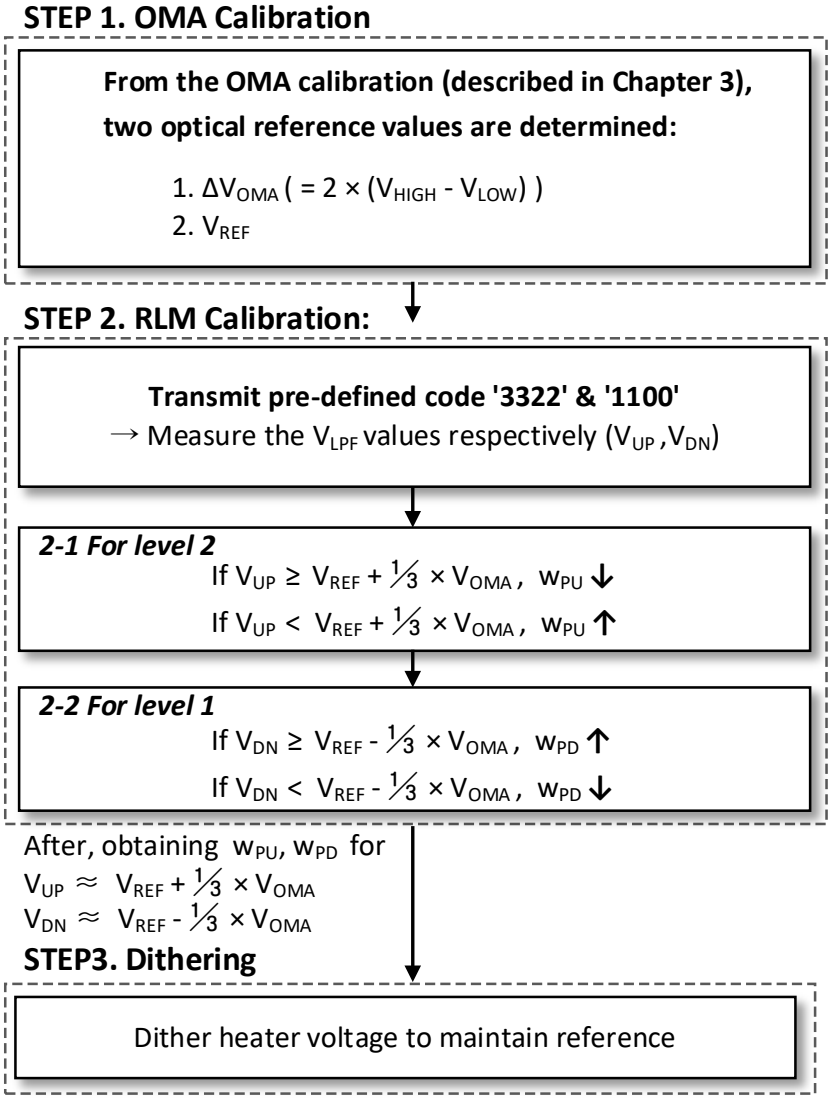


Fig. 4-11. Flow chart of the proposed dual-objective calibration algorithm.

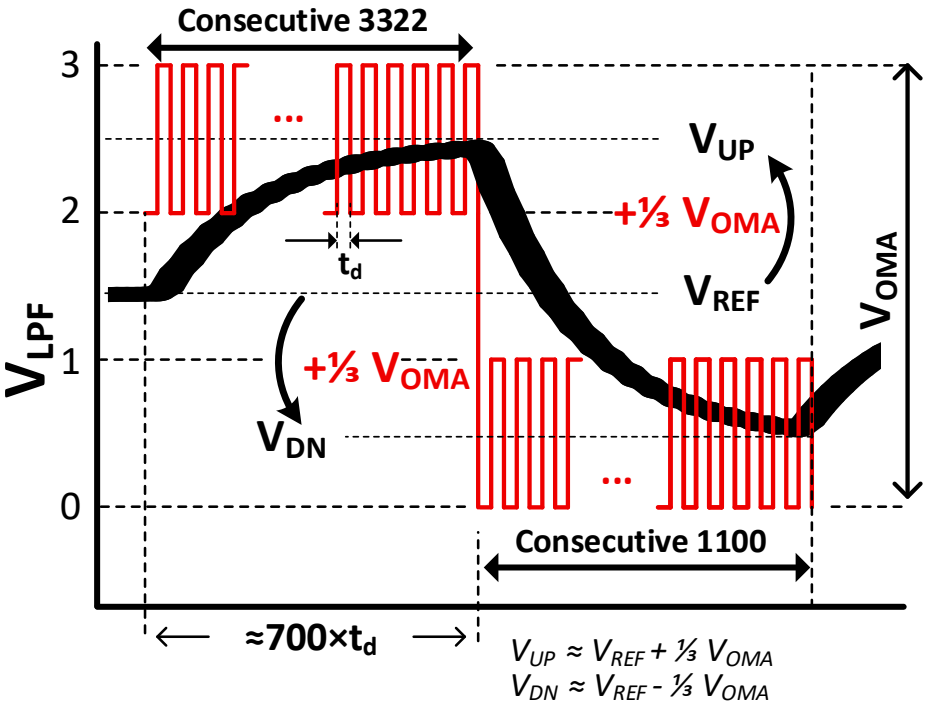


Fig. 4-12. Relationship between optical reference voltages and intermediate PAM-4 levels used in RLM calibration.

Table 4-1

Predefined input codes and corresponding V_{LPF} used in each calibration step.

$Code_{in}$	V_{LPF}	STEP	Notes
3330	V_{HIGH}	OMA Calibration	$\Delta V_{OMA} = 2 \times (V_{HIGH} - V_{LOW})$
0003	V_{LOW}		
3300	V_{REF}	Reference Set	Average optical power for dithering
3322	V_{UP}	RLM Calibration	$V_{UP} \approx V_{REF} + \frac{1}{3} \times V_{OMA}$
1100	V_{DN}		$V_{DN} \approx V_{REF} - \frac{1}{3} \times V_{OMA}$
PRBS	V_{PRBS}	PRBS Operation (with dithering)	

Fig. 4-11 and Fig. 4-12, together with Table 4-1, illustrate the detailed operation of the proposed dual-objective calibration algorithm that simultaneously establishes the optimum OMA and RLM conditions for the PAM-4 transmitter.

The overall calibration procedure begins with the OMA calibration phase, followed by the RLM calibration and the dithering step for long-term bias maintenance. The full control flow is summarized in Fig. 4-11, while the predefined input codes and their corresponding low-filtered voltages (V_{LPF}) are listed in Table 4-1.

At the end of the OMA calibration phase, two optical reference voltages are obtained: the total optical swing ΔV_{OMA} and the reference bias level V_{REF}. The optical swing represents the full modulation range of the transmitter output and is defined as

$$\Delta V_{\mathrm{OMA}} = 2 \times (V_{\mathrm{HIGH}} - V_{\mathrm{LOW}}) \tag{4.7}$$

The reference bias voltage, V_{REF} is obtained by applying the "3300" input pattern to the driver and recording the corresponding DC output level from the monitor photodiode. This value serves as the optical bias reference that represents the nominal center of the PAM-4 eye diagram and becomes the basis for subsequent level calibration as described in Chapter 3

After the reference values are determined, the controller proceeds to the RLM calibration phase. During this step, two newly added dedicated input patterns, "3322" and "1100," are sequentially applied to isolate the upper and lower intermediate PAM-4 levels. The optical outputs corresponding to these patterns are detected by the monitor photodiode, low-pass-filtered, and converted into feedback voltages V_{UP} and V_{DN}. The ideal target conditions for perfectly linear level spacing are defined as

$$V_{\mathrm{UP}} = V_{\mathrm{REF}} + \frac{1}{3}\Delta V_{\mathrm{OMA}}\ , \qquad V_{\mathrm{DN}} = V_{\mathrm{REF}} - \frac{1}{3}\Delta V_{\mathrm{OMA}} \tag{4.8}$$

These reference relations are illustrated conceptually in Fig 4-11. When V_{UP} is larger than $V_{\mathrm{REF}} + \frac{1}{3}\Delta V_{\mathrm{OMA}}$, the upper intermediate level (level 2) is higher than the ideal value, and the controller decreases the pull-up weight code w_{PU}, thereby increasing the pull-up resistance and lowering level 2. Conversely, if V_{UP} is smaller than the target, w_{PU} is increased. For the lower intermediate level (level 1), if V_{DN} exceeds $V_{\mathrm{REF}} - \frac{1}{3}\Delta V_{\mathrm{OMA}}$, the level 1 is too high and w_{PD} is increased, which decreases the pull-down resistance and lowers the level. Otherwise, w_{PD} is decreased. Through this iterative adjustment, the finite-state machine automatically tunes w_{PU} and w_{PD} until both intermediate levels converge to their target positions.

The entire routine operates autonomously within the on-chip controller, sequentially updating the heater DAC and driver weight codes until convergence is achieved. After the RLM loop is completed, the controller stores the optimized codes and activates the dithering phase to preserve the resonance bias at V_{REF}. By sharing a common feedback interface and digital control logic across channels, the architecture provides a compact and scalable solution for multi-channel WDM PAM-4 transmitters.

4.3 MEASUREMENT RESULTS

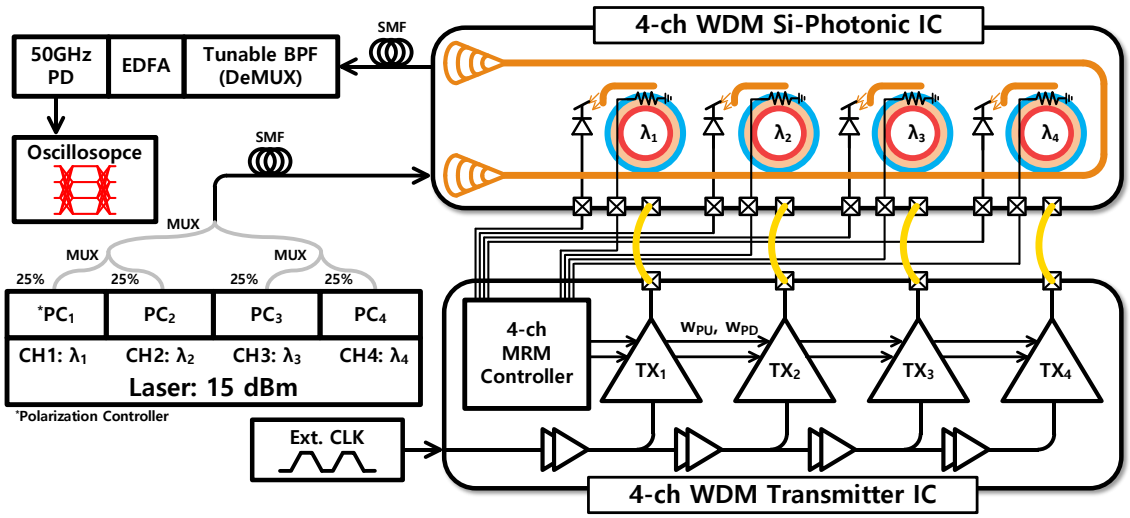
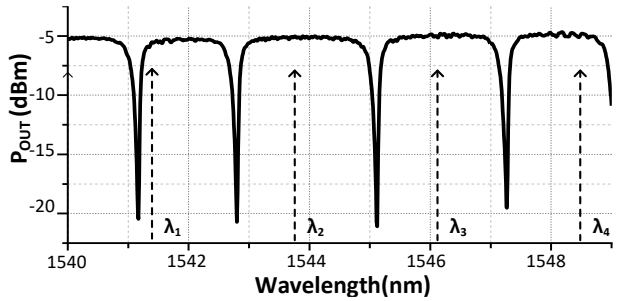


Fig. 4-13. Block diagram of the 4-channel WDM transmitter and measurement setup.



TX Channel	Wavelength
TX_1	λ_1 = 1541.3nm
TX_2	λ_2 = 1543.7nm
TX_3	λ_3 = 1546.1nm
TX_4	λ_4 = 1548.5nm

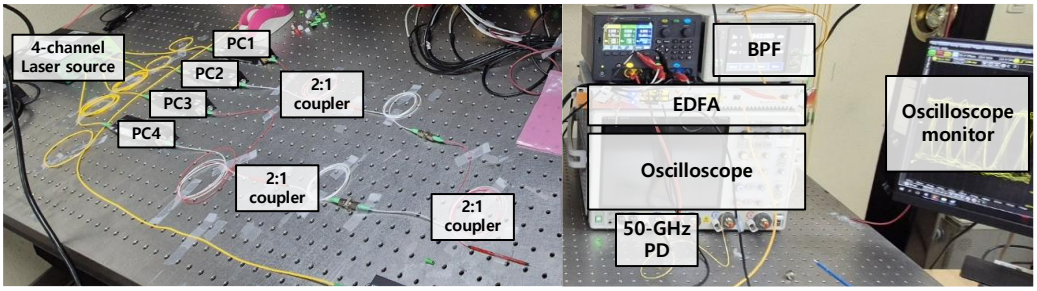
Fig. 4-14. Transmission spectra of TX and input laser wavelength settings.

The experimental verification of the proposed dual-objective calibration algorithm was conducted using the fabricated 4-channel WDM PAM-4 transmitter composed of the Si-photonic IC and CMOS electrical transmitter IC.

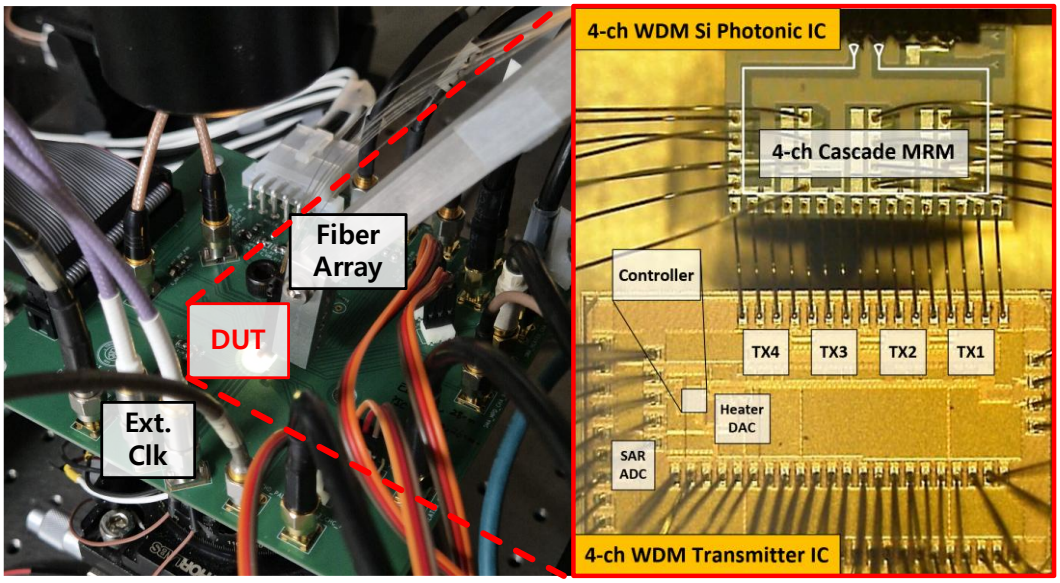
The complete optical measurement environment is illustrated in Figs. 4-12–4-14, which collectively show the system-level block diagram, wavelength allocation, and laboratory setup used for performance evaluation.

As shown in Fig. 4-13, a four-wavelength continuous-wave (CW) laser source with a total output power of 15 dBm was divided into four optical carriers (λ_1–λ_4) through 25% optical couplers. Each wavelength was individually polarization-controlled (PC_1–PC_4) and coupled into the microring-based WDM transmitter through single-mode fibers. The transmitter chip integrates four cascaded MRMs and a shared on-chip controller that coordinates the driver weights and heater biases for each channel. The modulated optical signals were wavelength-multiplexed and transmitted through a single-mode fiber (SMF) link to an optical receiver path consisting of an EDFA, a tunable band-pass filter (BPF), and a 50-GHz photodiode connected to a high-speed oscilloscope for waveform observation.

The measured optical transmission spectra of the four MRMs are shown in Fig. 4-14, along with the corresponding laser wavelength allocation. Each resonance wavelength was individually tuned using the integrated heater bias to align with the laser source, resulting in channel spacings of approximately 2.4 nm (λ_1 = 1541.3 nm, λ_2 = 1543.7 nm, λ_3 = 1546.1 nm, λ_4 = 1548.5 nm). These channels were used as the optical carriers for the PAM-4 modulation experiments and calibration tests.



(a)



(b)

Fig. 4-15. measurement setup (a) Benchtop setup (b) Stage setup and chip micrograph

Fig. 4-15 presents the overall laboratory setup for optical and electrical measurements. Fig. 4-15(a) shows the benchtop optical setup, including the polarization controllers, 2:1 optical couplers, EDFA, tunable BPF, and oscilloscope used to monitor the optical eye diagrams. Fig. 4-15(b) shows the mounted transmitter on the measurement stage and the chip micrograph of the fabricated WDM transmitter, where the Si-photonic IC and CMOS

driver IC are wire-bonded and interfaced through a fiber array for optical input and output connections. This setup enables full verification of the on-chip OMA and RLM calibration loops and allows real-time eye-diagram monitoring for all four WDM channels.

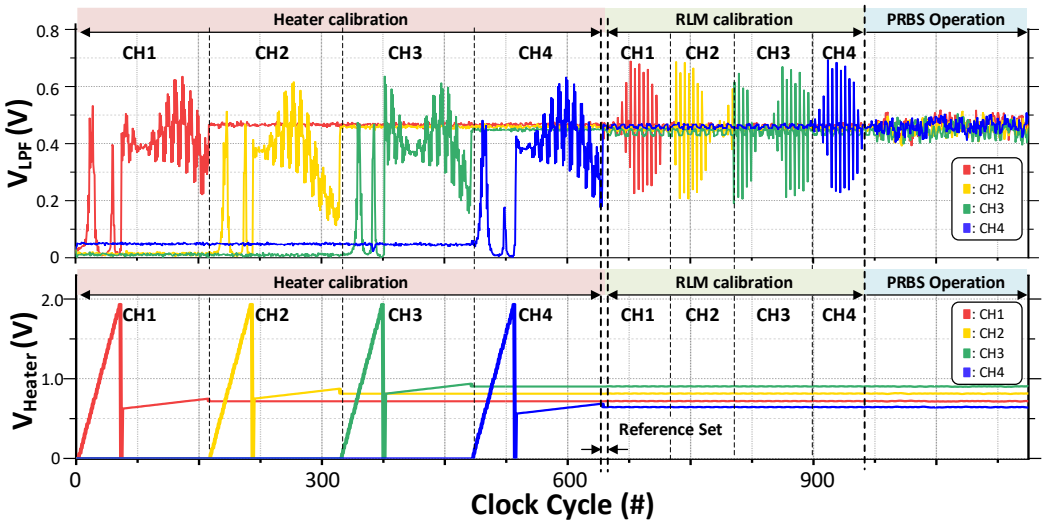


Fig. 4-16. Experimental results of the on-chip dual-objective calibration controller

The functionality of the proposed on-chip dual-objective calibration controller was experimentally verified using the 4-channel WDM transmitter described in Section 4.3. Fig. 4-16 shows the measured operation sequence of the integrated controller, demonstrating the autonomous execution of the OMA calibration, RLM calibration, and transition to PRBS operation. Each color represents one of the four WDM channels.

In the top panel, the feedback voltage V_{LPF} from the monitor photodiodes is plotted as a function of time. The controller sequentially performs the heater calibration for each channel to locate the maximum OMA point, followed by RLM calibration through electrical-level tuning of w_{PU} and w_{PD}. After calibration, the system switches to PRBS transmission mode, where the feedback remains constant, confirming that the resonance

condition and RLM are both stabilized.

The bottom panel of Fig. 4-16 shows the corresponding heater voltages for each channel during the same process. The gradual increase in the DAC output during the OMA calibration phase indicates the search for the optimal resonance bias. Once the reference set is established, the heater voltages are maintained through a periodic dithering operation during the RLM calibration and subsequent PRBS transmission, ensuring that each channel remains locked to its optimal optical bias point. These results confirm that the proposed controller can autonomously complete both optical and electrical calibrations for all four WDM channels without external assistance.

To further validate the robustness of the dithering mechanism, Fig. 4-17 shows the measured response of the transmitter when an external thermal disturbance was intentionally applied by sweeping the stage temperature from 20 °C to 30 °C. In this test, the stage temperature acts as an aggressor, while the on-chip controller actively compensates for the induced thermal drift.

The upper plot shows that the optical output voltage V_{LPF} of all channels remains stable, confirming that the resonance bias is successfully maintained. In contrast, the lower plot presents the corresponding heater power trajectories, which vary in the opposite phase to the stage temperature. This behavior demonstrates that the integrated dithering loop adaptively adjusts the heater DAC output to counteract external temperature fluctuations, thereby preserving the calibrated OMA and RLM conditions.

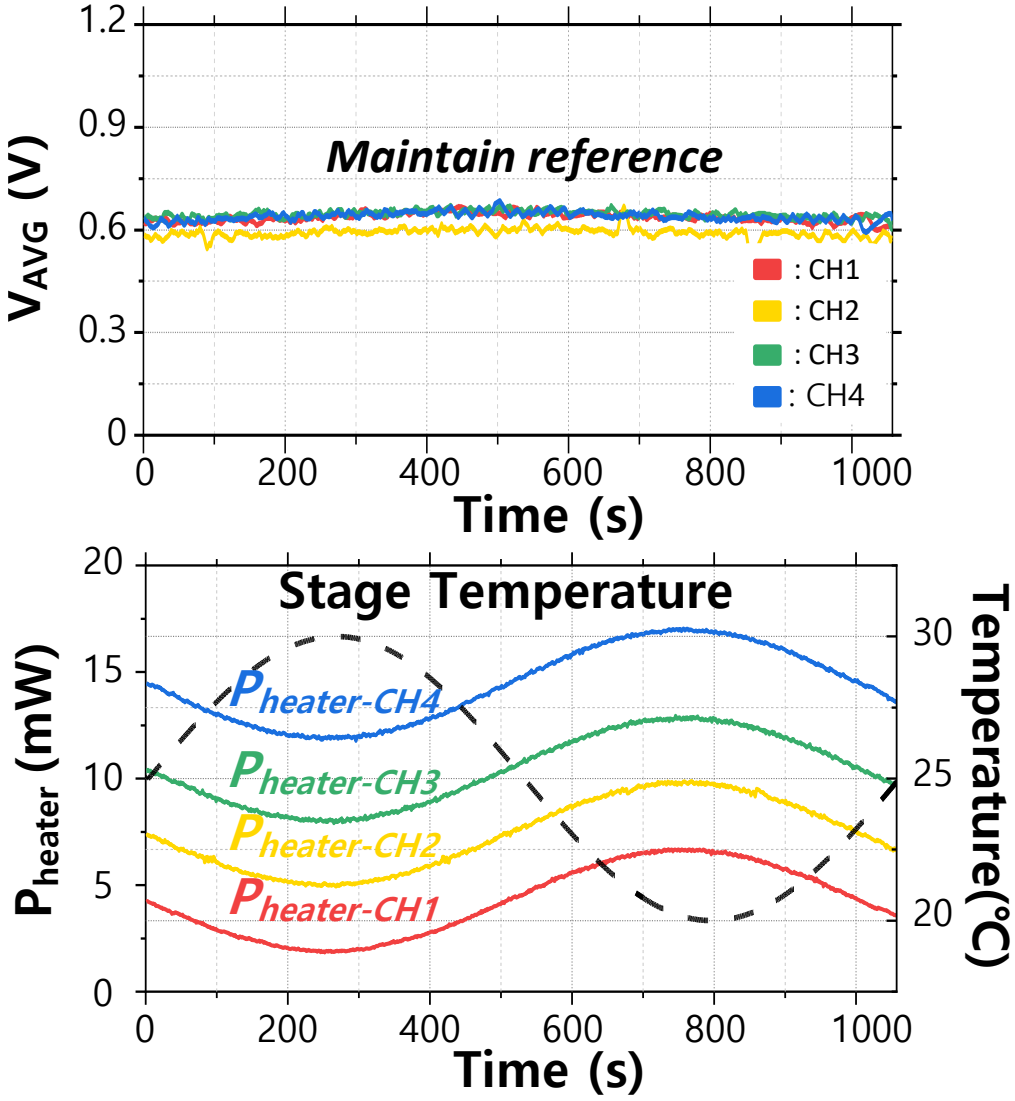


Fig. 4-17 Experimental results of the on-chip thermal controller's dithering performance under an external temperature variation from 20 °C to 30 °C.

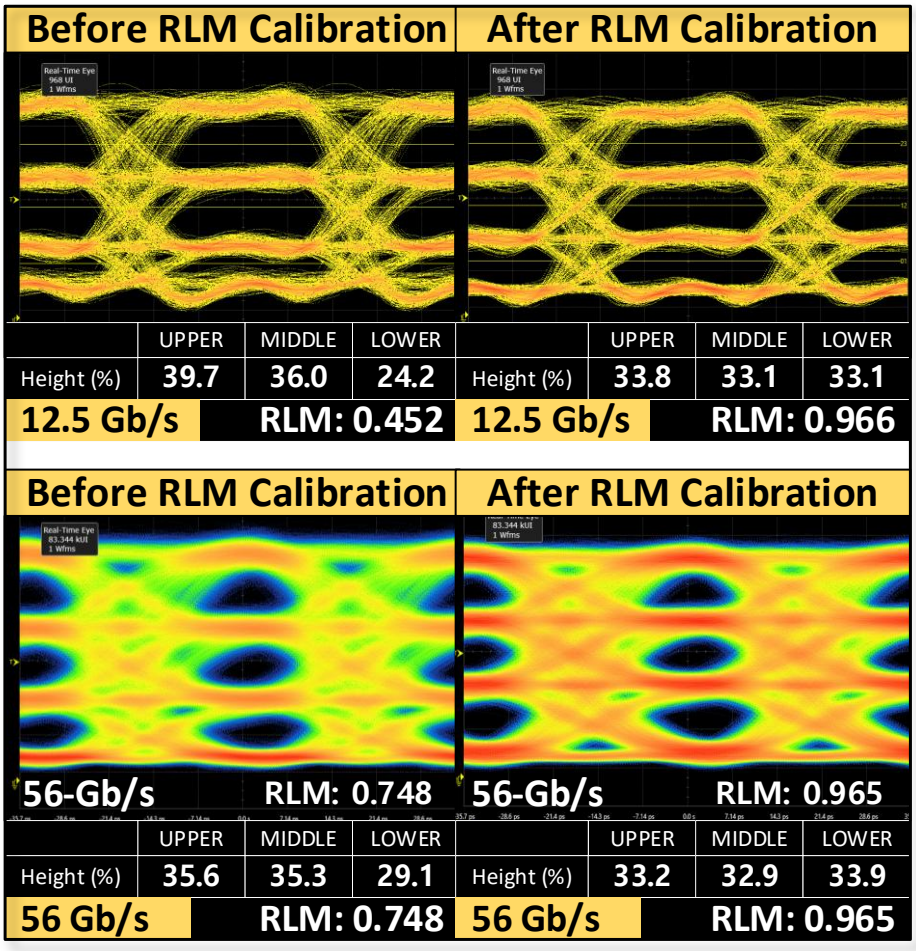


Fig. 4-18 Measured eye diagrams before and after RLM calibration at 12.5-Gb/s and 56 -Gb/s.

Fig. 4-18 shows the measured PAM-4 eye diagrams before and after RLM calibration for a single transmitter channel at 12.5 Gb/s and 56 Gb/s. The lower data rate of 12.5 Gb/s was included to provide sufficient bandwidth headroom and to observe the RLM more clearly without bandwidth-limited ISI. At the maximum-OMA operating point, the PAM-4 eyes still exhibit severe level imbalance, with RLM values of 0.452 at 12.5 Gb/s and

0.748 at 56 Gb/s. After the proposed calibration, the eye openings become symmetrically aligned, and the RLM improves to 0.966 and 0.965, respectively, demonstrating that the on-chip controller automatically restores proper level spacing across data rates.

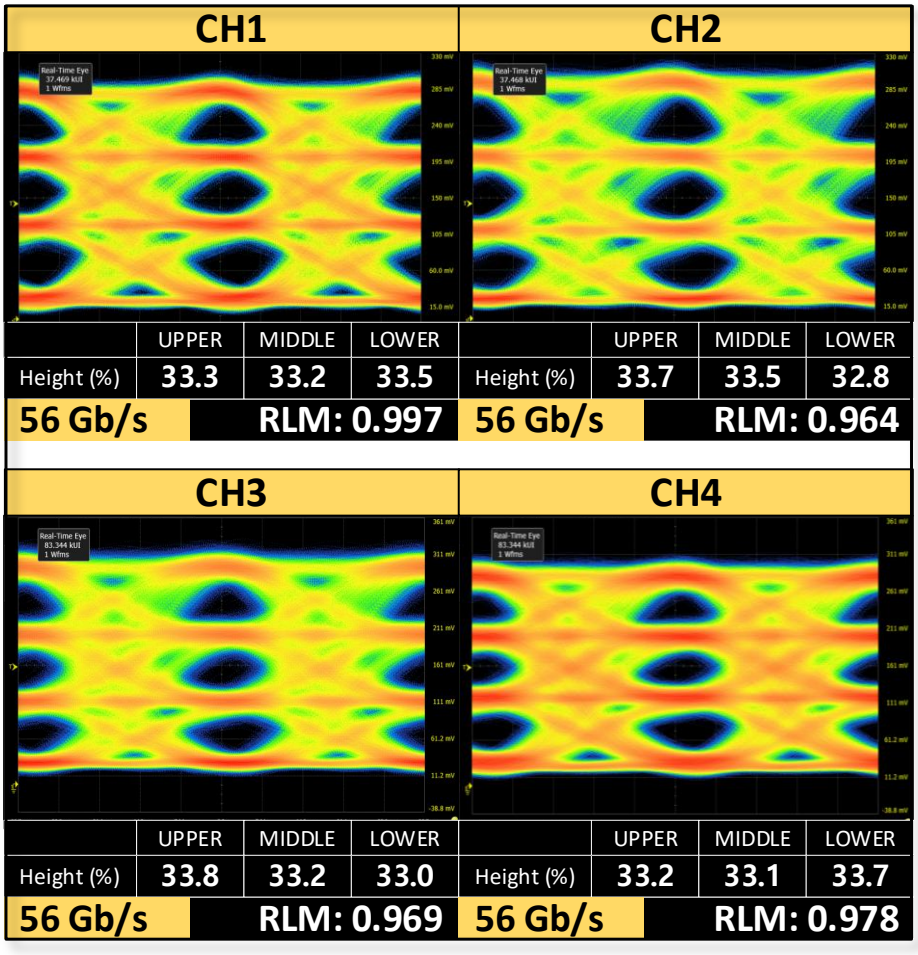


Fig. 4-19 Measured eye diagrams before and after RLM calibration at 12.5-Gb/s and 56 -Gb/s.

Fig. 4-19 extends this verification to all four WDM channels operating at 56 Gb/s per

channel after the dual-objective calibration. All channels show uniform PAM-4 level symmetry and comparable RLM values between 0.964 and 0.997, confirming consistent calibration performance and balanced operation across the entire four-channel transmitter. The resulting aggregate throughput of 224 Gb/s validates the scalability and robustness of the proposed on-chip calibration architecture. Table 4-2 summarizes the performance comparison with previously reported silicon photonic transmitters. The proposed work uniquely integrates both OMA and RLM calibration loops within a hybrid wire-bonded architecture, enabling simultaneous optimization and autonomous bias tracking across four WDM channels. Despite the added control circuitry, the transmitter achieves competitive energy efficiency of 1.99 pJ/b while maintaining 56-Gb/s per wavelength operation, demonstrating a favorable trade-off between performance and integration complexity. As shown in Fig. 4-20, the total power consumption of 398.5 mW is distributed among the driver, clocking network, re-timer, MUX, and pattern generator blocks, consistent with the overall system architecture.

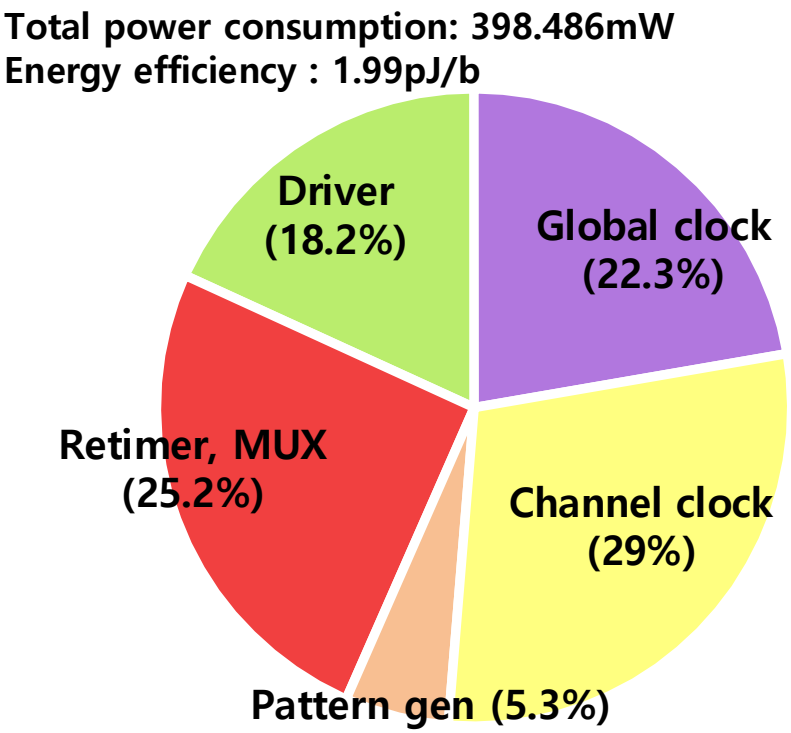


Fig. 4-20 Power consumption breakdown of the 4-channel PAM-4 WDM transmitter

Table 4-2

Performance comparison with previously reported silicon photonic transmitters.

Reference	**This work**	**[51]**	**[57]**	**[48]**	**[49]**	**[36]**
Integration	Hybrid (Wire-bonded)	Hybrid (3D Integration)	Hybrid (Wire-bonded)	Monolithic	Monolithic	Hybrid (Wire-bonded)
Modulation	PAM-4	PAM-4	PAM-4	NRZ	NRZ	NRZ
Laser Band	C (1550nm)	O (1310nm)	O (1310nm)	C (1550nm)	NIR (1180nm)	O (1310nm)
Gb/s/per-λ	56	112	40	25	5	50
# of Channel	4	4	1	1	11	4
Integrated OMA control	Yes	Yes	Yes	Yes	Yes	N/A
Integrated RLM control	Yes	No	Yes	No	No	No
Simultaneous RLM & OMA optimization	Yes	No	No	No	No	No
Self- heater optimization	Yes	No	No	Yes	Yes	N/A
Measurement configuration	All-λ	Per-λ	[2]N/A	[2]N/A	Per-λ	Per-λ
Energy efficiency (pJ/b)	1.99	5.8	1.7	13.8	[3]0.17	2.25

[1]Not Reported, [2]Not applicable, [3]Including driver and serializer only

CHAPTER 5 Conclusion

This dissertation has presented the design and experimental demonstration of integrated silicon photonic transmitters that enable scalable optical input and output for future high-performance computing and artificial intelligence systems. The primary contribution of this work is the introduction of a compact, code-based calibration framework that autonomously aligns and maintains the resonance of micro-ring modulators without the need for external digital signal processing or optical monitoring. Through the co-design of photonic and electronic circuits, the proposed systems achieve high data throughput with stable operation over temperature variations while maintaining low power consumption and compact footprint.

The first part of this work introduced a 32-Gb/s single-channel silicon micro-ring transmitter featuring an on-chip temperature control algorithm implemented entirely in the electrical domain. The controller determines the heater bias voltage that maximizes the optical modulation amplitude and continuously maintains this point through a low-bandwidth dithering loop. By employing DC-balanced calibration codes “1110,” “0001,” and “1100,” the system accurately estimates modulation depth using low-speed analog signals while suppressing baseline wander caused by AC coupling. Experimental results verified that the proposed transmitter maintains open eye diagrams and stable optical power under ambient temperature variations between 20 °C and 30 °C. These results confirm that reliable and fully autonomous resonance control of micro-ring modulators can be achieved with minimal hardware overhead.

The second part of the dissertation extended this concept to a four-channel 224-Gb/s wavelength-division-multiplexed transmitter using four PAM-4 drivers and on-chip control

logic. A dual-objective calibration algorithm was proposed to optimize both optical modulation amplitude and relative-level mismatch simultaneously. The controller coordinates heater tuning for optical bias and digital weighting in the driver for electrical predistortion, thereby establishing balanced PAM-4 signal levels across all channels. Measurements confirmed that all four wavelength channels achieved symmetric level spacing with RLM values close to unity while maintaining consistent optical output across thermal variations. These results demonstrate that the proposed approach is scalable and effective for multi-channel high-speed optical transmitters.

Although the demonstrated systems achieved robust operation and competitive energy efficiency, several limitations remain, which primarily arise from hardware constraints rather than from the proposed algorithms. The validated temperature range of ±5 °C was limited by heater drive capability, digital-to-analog converter resolution, and the thermal efficiency of the photonic platform. Extending this range will require higher-efficiency heaters, improved DAC linearity at high output voltage, and enhanced thermal isolation on the silicon photonics die. Similarly, the calibration time, currently on the order of a few seconds, was limited by the large parasitic capacitance at the monitoring node and by the bandwidth of the analog feedback path. Integrating a fully digitized monitoring circuit with an on-chip analog-to-digital converter and a high-speed serial interface can significantly shorten the calibration cycle and improve responsiveness to rapid thermal transients.

Future research can build upon this work by further co-optimizing the electronic and photonic domains. Improving heater efficiency and optimizing the free spectral range of the micro-ring can reduce the required tuning power, while incorporating adaptive digital control logic can enhance calibration accuracy and convergence speed in dense wavelength-division-multiplexed arrays.

In addition, the current micro-ring modulators exhibit limited modulation efficiency,

which requires the driver to deliver nearly full-swing output voltage to achieve sufficient optical modulation depth. This large voltage swing increases the effective output capacitance and constrains the overall electrical bandwidth, making it a bottleneck to developing even higher data rates. Future work should therefore investigate device-level techniques for enhancing the modulation efficiency of silicon rings and the development of high-speed driver architectures capable of safely operating beyond nominal supply voltage without compromising reliability. In the longer term, the presented architecture may be extended to transceiver-level designs that integrate co-packaged optical input and output directly with computing or memory chiplets. The results of this dissertation establish a foundation for self-calibrating, energy-efficient, and thermally robust silicon photonic interconnects that can support the scalability demands of next-generation data-centric systems.

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Abstract in Korean

실리콘 포토닉 집적 송신기 설계 및 온도·선형성 동시 보정 기법 연구

본 논문에서는 차세대 고성능 컴퓨팅(High-Performance Computing, HPC) 및 인공지능(AI) 시스템을 위한 확장 가능한 광 입출력(Optical I/O) 구현을 목표로, 실리콘 포토닉스(Silicon Photonics) 기반의 집적형 송신기 구조와 제어 기법을 제안하고 실험적으로 검증하였다. 제안된 구조는 마이크로링 변조기(Micro-Ring Modulator, MRM)의 열적 불안정성과 비선형 전송 특성을 근본적으로 해결하기 위한 것으로, 에너지 효율적이고 고속의 광 인터커넥트를 실현하는 데 있어 주요한 한계를 극복하고자 하였다.

첫 번째로, 32 Gb/s 단일 채널 실리콘 MRM 송신기를 설계하고, 온칩 코드 기반 온도 보정(Code-Based Temperature Calibration) 및 잠금 알고리즘을 구현하였다. 제어기는 광 변조 진폭(Optical Modulation Amplitude, OMA)을 최대화하는 히터 바이어스 전압을 자동으로 탐색하고, 저대역폭 디더링(Dithering) 루프를 통해 해당 동작점을 안정적으로 유지한다. 또한 직류 균형(DC-Balanced)을 이루는 보정 코드를 사용함으로써, 저속 아날로그 신호만으로 정확한 OMA 추정을 가능하게 하였으며, 교류 결합(AC-Coupling)으로 인한 기준선 이동 문제를 억제하였다. 실험 결과, 제안된 송신기는 20 °C에서 30 °C의 온도 변화 범위에서도 안정적인 개방 아이 다이어그램(Open Eye Diagram)을 유지하며 일관된 광출력을 확보함을 확인하였다. 이를 통해 외부 광 검출기나 고속 디지털 신호 처리 없이도 완전한 온칩 자율 보정이 가능함을 입증하였다.

두 번째로, 위 개념을 확장하여 224 Gb/s (4 채널 × 56 Gb/s) 파장분할다중화(Wavelength-Division Multiplexing, WDM) 송신기를 설계하였다. 본 구조는 PAM-4 변조 방식을 적용하고, 광 변조 진폭(OMA)과 레벨 비대칭(Relative Level Mismatch, RLM)을 동시에 최적화하는 이중 목표 보정 알고리즘(Dual-Objective Calibration Algorithm)을 제안하였다. 제어기는 광학 영역에서의 열 튜닝(Heater Bias Control)과 전자 영역에서의 디지털 가중 제어를 병행하여 모든 채널에서 균일한 PAM-4 레벨 간격을 확보하였다. 실험 결과, 네 개의 WDM 채널 모두에서 대칭적인 아이 레벨(RLM ≈ 0.97)과 안정된 열 잠금 특성을 달성하였으며, 다채널 환경에서도 높은 재현성과 확장성을 입증하였다.

본 논문에서 제시된 시스템은 높은 에너지 효율과 안정적인 동작을 보여주었으나, 향후 성능 확장을 위해 해결해야 할 하드웨어적 한계 또한 존재한다. 현재의 MRM은 변조 효율(Modulation Efficiency)이 낮아 충분한 광 변조 깊이를 확보하기 위해 드라이버가 거의 풀스윙(Full Swing)에 가까운 전압을 인가해야 한다. 이러한 큰 전압 스윙은 출력 용량성 부하(Capacitive Load)를 증가시키고 전체 전기적 대역폭을 제한함으로써, 더 높은 데이터 속도를 개발하는 데 병목으로 작용한다. 향후 연구에서는 MRM의 변조 효율 향상, 공정 한계를 초과하는 고속 소스-직렬 종단(Source-Series Termination, SST) 드라이버 구조의 개발, 그리고 디지털화된 피드백 구조를 통한 온도 보정 속도 향상 및 히터 효율 개선 등이 요구된다.

본 연구의 결과는 온도 안정화, 선형성 보정, 파장 관리 기능을 단일 칩 상에서 통합한 자율 보정(Self-Calibrating) 실리콘 포토닉 송신기 아키텍처의 실현 가능성을 입증하였다. 이러한 기술은 차세대 컴퓨팅 플랫폼이 요구하는 대역폭, 에너지 효율, 신뢰성을 동시에 만족시키는 코패키지드 광 입출력(Co-Packaged Optical I/O) 솔루션의 기초를 제공한다.

핵심 단어: 실리콘 포토닉스, 마이크로링 변조기, 광 송신기, 온도 보정, PAM-4 변조, 소스-직렬 종단(SST) 드라이버, 파장분할다중화(WDM), 광 인터커넥트, 고속 드라이버, 고성능 컴퓨팅(HPC), 인공지능(AI) 시스템

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