

A Giga-b/s CMOS Clock and Data Recovery Circuit with a Novel Adaptive Phase Detector

Jae-Wook Lee, Cheon-O Lee, Woo-Young Choi

Dept. of Electrical and Electronic Eng., Yonsei University,
134, Shinchon-Dong, Sudaemon-Ku, Seoul 120-749, Korea
TEL : (02) 2123 - 2874, E-mail : patima@tera.yonsei.ac.kr

Abstract

In this paper, a new clock and data recovery circuit (CDR) is proposed for the application of data communication systems requiring GHz-range clock signals. The high frequency jitter is one of major performance-limiting factors in CDR, particularly when NRZ data patterns are used. A novel phase detector is able to suppress this noise, and stable clock generation is achieved. Furthermore, the phase detector has an adaptive delay cell, and thus the optimal characteristic for fast locking is achieved. The proposed circuit has a structure that can be easily extended to multi-channels. The circuit is designed based on CMOS $0.25\mu\text{m}$ fabrication process and verified by measurement results.

1. Introduction

As the critical dimensions decrease and the integration level increases in CMOS process technology, the data rate for chip-to-chip communication can often be a limiting factor for the entire system performance. In a bus system where more than two chips are connected to a signal line, the signal bandwidth of the bus signal line is restricted by the pin capacitance loading and the reflected signals due to transmission line effects. Consequently, there is a growing demand for high-speed serial transmission between ICs. In such applications, the CDR circuit is a key component, which determines the overall transmission performance.

In this paper, a CDR circuit with a novel phase detector (PD) is realized which can be used for multi-channel, large-capacity, high-speed transmission systems. The new PD responds only to the transitions of NRZ data and, thus, very stable clock signals can be generated even with burst-mode data. Our CDR is realized with $0.25\mu\text{m}$ CMOS fabrication process and measurement results confirm its performance.

2. CDR architecture

Figure 1 shows a block diagram for a CDR based on phase locked loop (PLL). The CDR has linear type PD, ring-oscillator type VCO, charge pump and second-order loop filter. The VCO has both course and fine and controls. The course control signal is supplied externally in the present circuit, and the fine control tunes the clock phase.

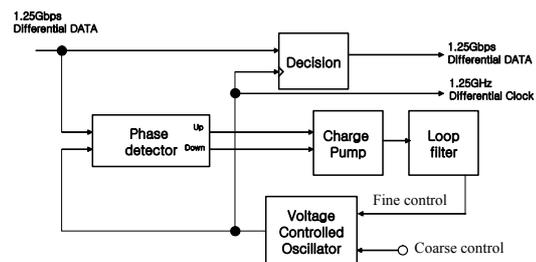


Fig. 1 Block diagram of CDR circuit

A. Phase Detector

PDs generally appear in two different forms, nonlinear and linear. Nonlinear PDs coarsely quantize the phase errors, producing either positive or negative values at output. Linear PDs, on the other hand, generate linearly proportional output that drops to zero when the loop is locked[1]. In the burst NRZ (Non Return to Zero) data recovery system, PD must operate only when there are data transitions so that error signal generation for consecutive data values are avoided. Consequently, the linear PD responding only to data transition has better jitter characteristics [1-3].

The linear PD used in the CDR circuit compares data with clock edges and generates control signals that are proportion to phase errors only when data transition is occurred. It is composed of two delay elements, two XOR gates and two AND gates, as shown in Fig.2. To detect input data transitions, data input is delayed to

generate Data-A, Data-B and Data-C. Note that unless incoming data make transition, there are no transition in Data-A, Data-B and Data-C.

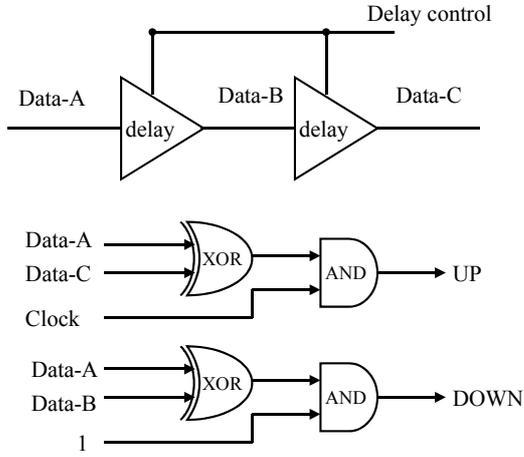


Fig. 2 Schematic diagram of proposed PD

The loop aligns the falling edges of the VCO clock signals with the zero-crossing time of the delayed input Data-B. For example, consider cases in which clock transition occurs either slightly earlier or later than the data transition point B, as shown in Fig.3. The DOWN pulse is high only when Data-A and Data-B are unequal, either Data-A is high or low. This means that a constant-width DOWN pulse is generated whenever incoming data make transitions. Therefore, the UP/DOWN pulses can be generated as

$$\begin{aligned} \text{UP} &= (\text{Data-A} \otimes \text{Data-C}) \cap \text{clock} \\ \text{DOWN} &= \text{Data-A} \otimes \text{Data-B} \\ (\otimes: \text{XOR}, \cap: \text{AND}) \end{aligned}$$

When the clock falling edge comes earlier than the data, the DOWN pulse stays high longer than the UP pulse, and the VCO frequency will decrease. Similarly, the late clock increases the VCO frequency. An equilibrium is reached if the UP and DOWN pulses are equal, and no charge is pumped when the static phase error is zero.

If the clock makes no transition inside the window formed between the Data-A and Data-C transitions, one of the UP or DOWN pulse pulls the VCO clock falling edge into the window. As shown in Fig. 4, PD operates linearly in range of $-\Phi \sim \Phi$, making the gate delay time critical. To optimize delay width, adaptive delay cells are needed. Optimized delay width(Φ) becomes $\pi/2$

because the window formed between the Data-A and Data-C should cover all the phase ranges ($-\pi/2 \sim \pi/2$). If delay cell has static delay width, the window cannot cover all the ranges, and PD linearity would be broken outside the range.

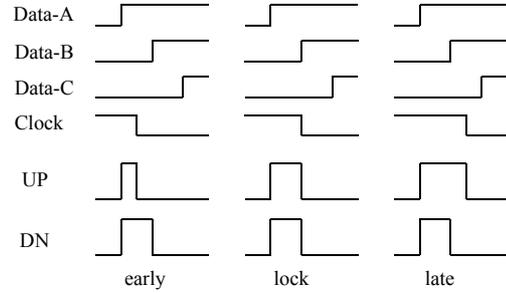


Fig. 3 Phase detector operation

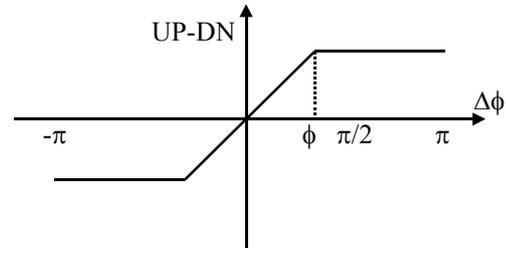


Fig. 4 Phase detector Characteristics

For the adaptive delay cell, we used the VCO inverter cell. Ring oscillator VCO is composed of even number differential inverters. If VCO is composed of four inverter cells, two serial inverters are delay cells that have the delay width of $\pi/2$. The VCO control voltage will tune delay cells while phase alignment is progressing.

B. Voltage Controlled Oscillator

Several parameters of the PLL, such as speed, timing jitter, spectral purity and power dissipation, strongly depend on the performance of the VCO. Ring oscillators usually have the advantages of small die size and simple structure, and are more suitable for integration on a standard process. The VCO core is a differential inverter circuit. The block diagram of the ring oscillator VCO is shown in Fig. 5. The inverter circuit has four types of loads. The VCO has both coarse and fine control voltages. The coarse control is provided externally in this prototype. The fine control exhibits a gain of 100MHz/V and the coarse control, 600MHz/V. The tuning range is 0.9GHz – 1.6GHz.

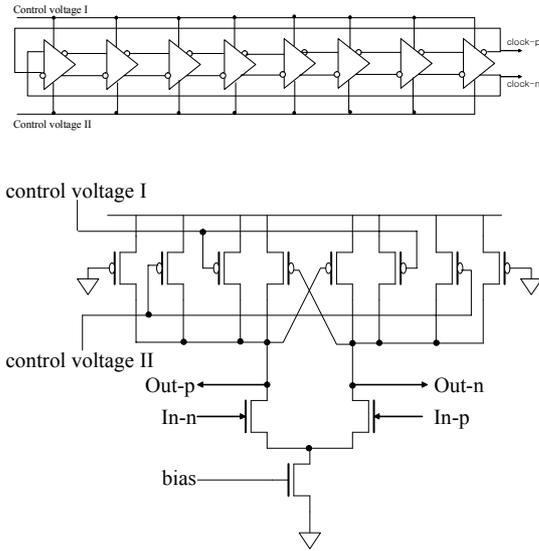


Fig. 5 Schematic diagram of VCO

C. Charge Pump and loop filter

Fig. 6 shows the implementation of the charge pump. For high speed and stable operation, the charge pump is composed of two current sources and four switches controlled by PD[4].

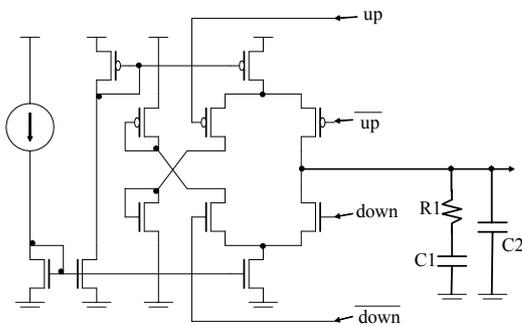


Fig. 6 Charge pump and loop filter

3. Experimental Result

The CDR circuit was fabricated in a $0.25\mu\text{m}$ CMOS process. Fig. 7 shows a photograph of the chip, which occupies an area of $2.7 \times 2.7\text{mm}^2$. Electrostatic discharge (ESD) protection diodes are included for all pads. In addition, several test circuits for in-out buffers and VCO are included. The CDR core including the loop filter occupies $0.8 \times 0.9\text{mm}^2$.

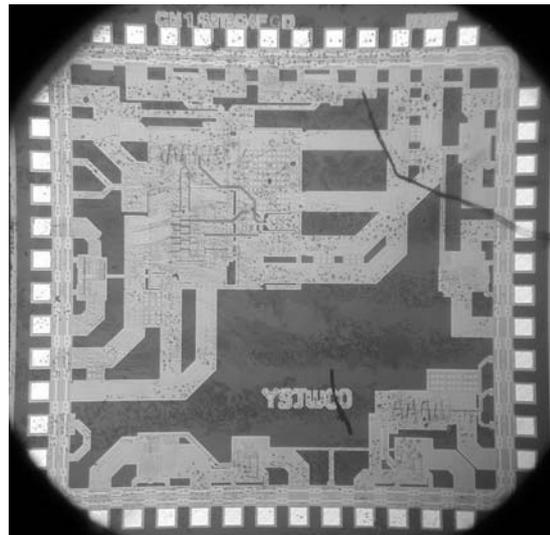


Fig. 7 Chip photograph

Fig. 8 depicts the recovered clock in the time domain in response to 1Gb/s Pseudo Random Bit Sequence (PRBS) with sequence length of $2^{15}-1$. The measured RMS jitter of the generated clock signal is 3.55ps. The eye diagram of retimed data is shown in Fig.9. The CDR circuit is error free for 0.9Gb/s – 1.4Gb/s $2^{15}-1$ PRBS. The total power consumed by the CDR circuit including in-out buffer is 490mW from a 2.5V supply. A performance summary of the chip is given in Table 1.

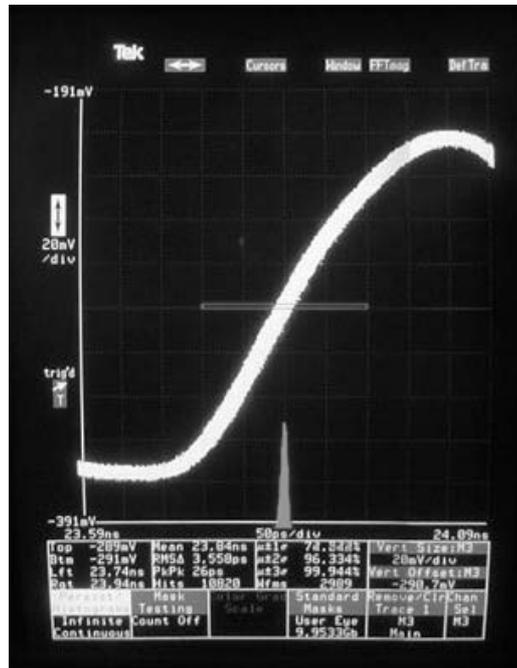


Fig. 8 Clock jitter (@1Gb/s $2^{15}-1$ PRBS)

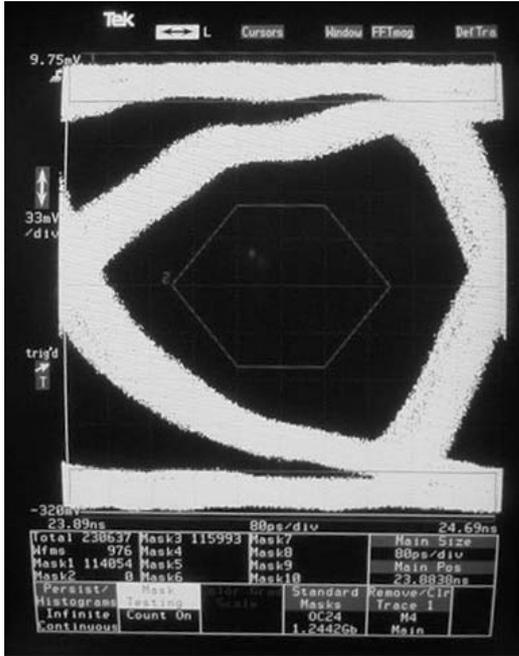


Fig. 9 Eye diagram (@1Gb/s $2^{15}-1$ PRBS)

Process	0.25 μ m CMOS technology
Power dissipation @VDD=2.5V	About 500mW (I/O include) About 200mW (core)
Chip size	0.8 x 0.9mm ² for CDR core including loop filter
Package	48pin TQFP plastic package
Jitter characteristics	RMS 3.55ps @1Gb/s $2^{15}-1$ PRBS P-P 26ps @1Gb/s $2^{15}-1$ PRBS
Lock range	0.9Gb/s – 1.4Gb/s

Table 1. Performance Summary

4. Conclusion

In this paper, a new clock and data recovery circuit is realized for the application of data communication systems requiring GHz-range clock signals. A novel phase detector is able to suppress high frequency noises, and stable clock generation is achieved. Furthermore, the phase detector has an adaptive delay cell removing the dead zone problem and has the optimal

characteristics for fast locking. The proposed circuit has a structure that can be easily extended to multi-channels. The circuit fabricated with CMOS 0.25 μ m process shows error-free operation in the range of 0.9Gb/s – 1.4Gb/s. With 1Gb/s random sequence of length of $2^{15}-1$, it produces very stable clock signals with RMS jitter of 3.55ps.

Acknowledgement

This work was supported by the System 2010 Project.

References

- [1] Jafar Savoj, Behzad Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector," *IEEE J. of Solid-State Circuits*, vol. 36, pp.761-768, May 2001.
- [2] C. R. Hogge, Jr., "A self correcting clock recovery circuit", *J. of Lightwave Technology*, vol. 3, No. 6, Dec. 1985.
- [3] Bang-Sup Song and David C. Soo, "Timing Recovery Technique for Band-Limited Channels", *IEEE J. Solid-State Circuits*, vol. 32, no. 4, pp. 514-520, 1997.
- [4] J. Maneatis, "Low-Jitter and Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. of Solid-State Circuits*, vol. 31, pp. 1723-1732, no. 11, Nov. 1996