A 622Mbps burst mode CDR with jitter reduction capability

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Abstract- This paper proposes new 622Mbps burst mode CDR(Clock and Data Recovery) circuit with jitter reduction capability. Using ZPS(Zero Phase Start) technique[1], the proposed circuits synchronize edges of the output clock and bursting data. The external control signal alters the locking reference of the output clock between 1/4 divided local clock(155.5MHz) and 622Mbps NRZ input data. It consumes three bits of preamble to lock at the incoming data. The circuits are designed with 0.25㎛ CMOS technology, and verified by post layout simulation. Estimated power consumption is 100 ㎽ without IO circuits.

1. Introduction

CDR circuits are one of the most essential building block of the burst mode systems such as ATM/Ethernet PONs. In such systems, burst mode CDR block has to extract clock information from a few number of preamble bits. A variety of structures have been reported and they can be categorized in two.

The first type of burst mode CDR uses somewhat complicated logic circuits to extract clock edges from data directly[2]. These circuits usually generate the clocks equally separated phases with the same frequency near the data rate and compares clock edges with data transition points, and select the nearest one among them. They CDR consume three or four of preamble bits to lock. It is relatively fast phase acquisition, and is capable of rejecting jitters. But for the heavy load of the logic circuits, these kind of CDRs can operate only at relatively low frequencies.

The second type uses gated oscillators to synchronize edges of the clock to the center of bit intervals of the data[3]. A gated oscillator has a gating stage(NAND, NOR, or MUX) among its inverter ring. The clock edge propagation along the ring can be stopped and restarted by the VCO enable signal, making it possible to synchronize the clock instantly.

This is called ZPS technique. This sort of CDR typically uses two gated VCOs, and requires anadditional replica PLL locked at the local reference clock to generate control voltages for gated VCOs. Because it is not a feed back system, it cannot provide jitter reduction. And in case that mismatches between the reference VCO and the clock-generating VCO are large, it cannot tolerate long sequences of continuous 1's or 0's.

In this paper, we propose a newly designed burst mode CDR circuits, which can handle up to 622Mbps data rate and provide jitter reduction.

2. Circuit operation

1. Basic ideas

The proposed CDR uses only one gated VCO, and the external control signal, BSTE(BurST Enable) alters the locking reference between the divided reference clock and the data. Simple control logic circuits control VCO, frequency divider, PD(Phase Detector), and PFD(Phase Frequency Detector) along the predefined sequence, abd only three bits are required to phase locking process. Once locked at data, it functions exactly like a PLL(Phase Locked Loop)-based continuous mode CDR. When the data burst ends, the loop alters back its locking reference to the local clock.

Fig.1 shows the block diagram of the circuit. There are virtually two phase locked loops.

Loop 1 consists of a VCO, a PFD, a charge pump, a loop filter and a frequency divider. When the BSTE goes to low, the reference loop is enabled and the PFD feeds back the frequency/phase error to the VCO, acquiring the lock. At this time, PD is disabled and the charge pump acts only according to the PFD output. Then the circuits act exactly like an ordinary PLL.

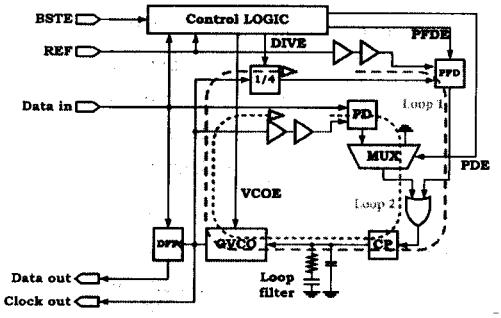

Fig.1 The block diagram

Loop 2 uses a PD instead of the PFD, and the frequency divider is disabled. This loop is activated when the BSTE goes to high. The PD used here generates up/down signal only when the data transition exists, removing the unnecessary charge pump activities.[4] The loop functions like an ordinary PLL based continuous CDR circuit after switching process is completed.

Fig.2 shows the control logic circuit state diagram. It is a simple FSM(Finite State Machine) that has 10 states. It controls other blocks as follows.

Once the system is powered on, and BSTE si kept low, the REF(local REFerence clock) signal forces the FSM to enter the state 0. At this state, like a common PLL, the PD generates frequency/phase error signals and the CP(Charge Pump) pumps up/down the VCO control voltage, then the loop locks at the REF. In other words, the circuit operate along the loop 1.

When BSTE goes to high, PFD is disabled, and the data signal is now allowed to toggle the states and the edges of the signal drive the FSM into the next states, state 1. The first rising edge stops VCO oscillating, and the following falling edge disables the divider, the next rising of the signal makes the VCO oscillate again, so the clock edge is aligned to the data bits. Finally at the state 5, PD is enabled and the loop 2 is activated. This process consumes three bits of preamble. See the timing diagram of fig.6 in section 3.

The time delay through the control logic can be a problem in this structure. Theoretically, assuming the delay is zero, this switching scheme will work well. But in real circuits, the delay will make initial phase errors when the circuit enters state 0 and 5, and they result in additional phase acquisition time. To compensate it, two delay states are added each to the REF and data signal paths.

Even a slight delay results in ripple on the VCO control signal. A delay calibration circuit can be the best remedy, but in the designed circuit, the delay was tuned manually.

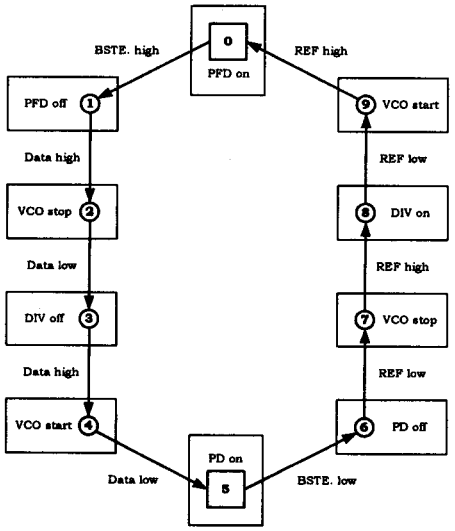

Fig.2 The state diagram

3. Circuit design

3.1 VCO

A parallel combination of a DC biased MOS and a diode connected MOS is called symmetric load, and the replica biasing scheme allows designers to use the most linear region of the I/V characteristic of the symmetric loads. The scheme used in VCO delay stage and bias circuits of Fig.3 are the same as those in [5].

As gating stage, a MUX is used among the

delay rings and the signals from the previous buffer are inverted. The second input terminal is tied with logical high. When VCOE(VCO Enable) is low, the MUX selects the second input. If VCOE signal goes to high, the oscillation begins.

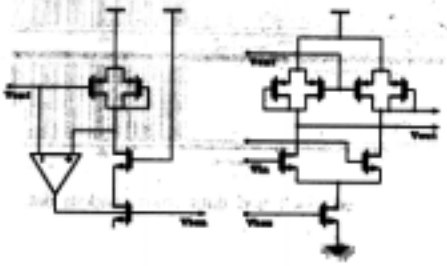

Fig VCO bias circuit and delay stage

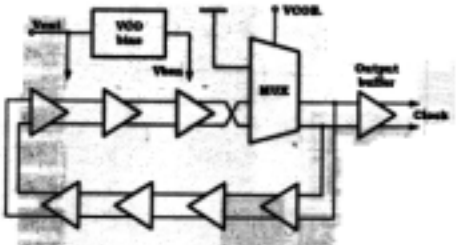

Fig.4 The gated VCO

3.2 Control logic circuit

The control logic circuit showed in fig. consists of 8 SR-latches and has 10-states.

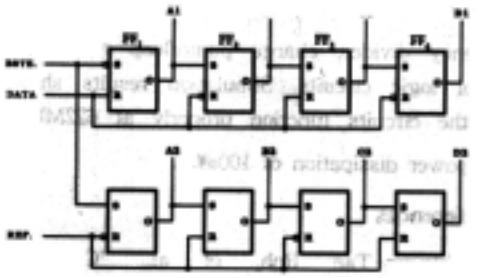

Fig. 5 Control logic circuit

For example, when the BSTE goes to high, the FF_1 becomes resettable. If the DATA signal goes to high, output of FF_1(A1) becomes low and FF_2 becomes resettable, and so on. The output signals of each latch translates into control signals using simple logic algebra shown in fig.6.

3.3 Other building blocks

All the logic circuits are designed with differential logic gates. Although differential signaling consumes more powers and is cumbersome to design, it is faster and less susceptible to noises.

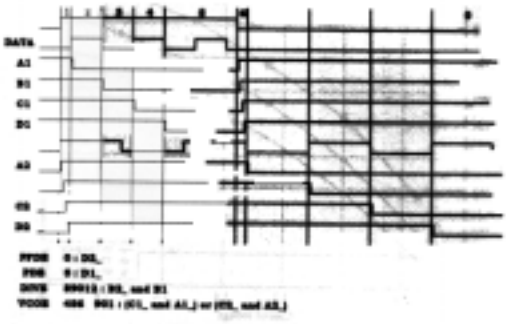

그림 6. Control signal timing diagram

PFD output terminals and PD's are tied by OR gates as shown in Fig.1. The control logic determines which phase detector can be used at each states and generates proper control signals. As described in section 2, the frequency divider in this design must be restartable as well as the VCO. Using SR-latch the frequency divider used here is designed to be resettable.

3.4 Loop dynamics

Loop bandwidth and damping factor describe the loop dynamics almost completely and they are calculated as follows:

loop bandwidth $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{C}}$

damping factor $\zeta = \frac{R}{2}\sqrt{K_{PD}K_{VCO}C}$

For our design, K_{PD} = 75μA/rad, K_{VCO}=500MHz/V, C=150pF, and R=500Ω, which provides:

ω_n = 15MHz and ζ = 0.6

4. Simulation results and layout

Designed circuits are simulated using CMOS 0.25μm parameter by HSPICE.

Fig.7 shows VCO gain curves and calculated VCO gain over process corners. Replica biased VCO delay stages provide a large range of delay variation.

Measured VCO gain is around 500MHz/V and all three curves covers 622MHz, the target frequency.

Fig.8 is the transition process from the reference loop to the data loop.

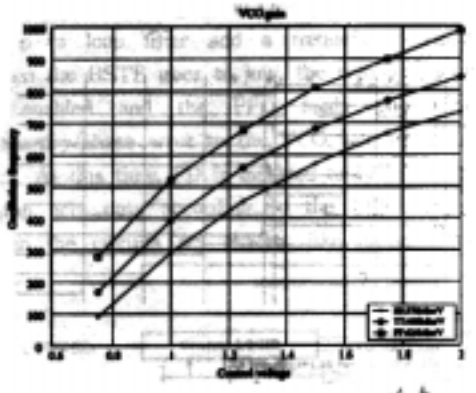

Fig.7 VCO gain

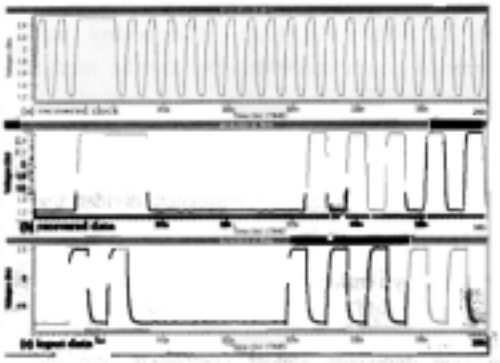

Fig. 8 Recovered clock and data from data burst

Fig.8-(c) shows the data burst starts with 3bit preambles followed by continuous eight 0's. This bit pattern shows that the phase lock occurs properly in the switching process from loop 1 to loop 2. If there are initial phase errors large enough or VCO control voltages are shifted a lot during the process, a bit cycle slip will be occurred. Fig.8-(a) shows recovered clock and Fig.8-(b) shows continuous bits are successfully recovered excluding preamble bits.

Fig.9 shows the initial phase acquisition and the recovered data output for the MATLAB generated random data. Fig.9-(a) shows the VCO control voltages.

Fig. 10 is the layout capture of the designed circuits.

5. Conclusion

New burst mode CDR circuits for 622Mbps NRZ data are designed with 0.25㎛ CMOS technology. Building block are also designed including fully differential gated VCO, PFD/PD,

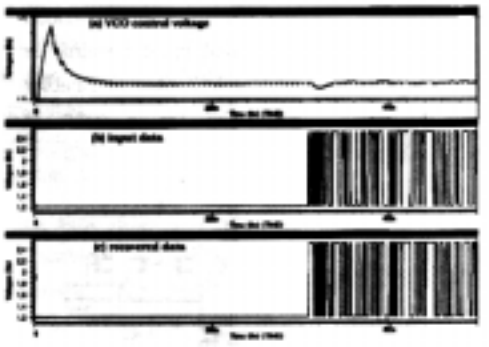

Fig. 9 Recovered clock and data from random data

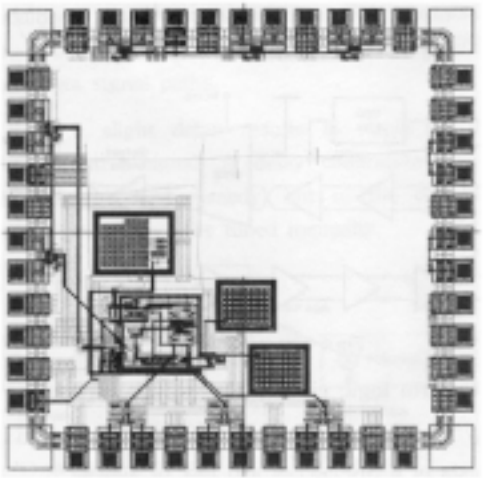

Fig. 10 Layout of the designed circuit

frequency divider, charge pump/loop filter and control logic circuits. Simulation results show that the circuits function properly at 622Mbps with power dissipation of 100㎽.

6. References

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