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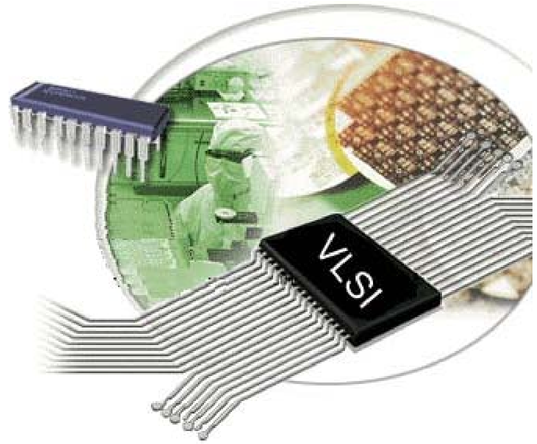

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1.25Gb/s Burst-mode CDR with Robustness to Duty Cycle Distortion

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Abstract – *With burst-mode optical receivers, duty cycle distortion appears inevitably. If CDR based on gated-oscillators is used in the burst mode receiver, its performance is seriously affected by duty cycle distortion. In this paper, we show why duty cycle distortion occurs, and how this distortion affects the CDR. And we propose a new CDR structure which is robust to duty cycle distortion.*

Keywords: burst-mode CDR, burst-mode optical receiver, duty cycle distortion, automatic threshold control, gated oscillator, phase interpolator, passive optical network

1 Introduction

In recent years, the speed of subscriber network is continuously increasing. With a phone line, the data rate is limited to several tens of megabits per second. The interest in FTTH (fiber to the home) is growing as a next step subscriber network technology.

Passive Optical Network (PON [1]) is one kind of FTTH services. As shown in Fig. 1, OLT is the service provider and ONU is the subscriber. For down-link (from OLT to ONU), data are broadcasted based on continuous-mode Time Division Multiplexing (TDM), and for up-link (from OLT to ONU), burst-mode Time Division Multiple Access (TDMA) is used. Up-link and down-link share same fiber with Wavelength Division Multiplexing (WDM). In down-link, each ONU receives its data from the broadcasted data at a set time. In up-link, OLT assigns a time slot for each ONU to send data. But characteristics of each channel between ONU and OLT are different, and, consequently, data received at OLT are not synchronized. Therefore, the uplink data stream is in burst mode.

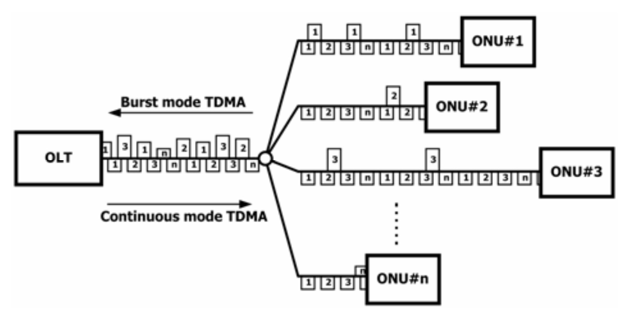

Fig 1. Up/Down link in PON

CDR using tracking algorithm (e.g. PLL) is not suitable for the burst mode application, because the tracking time is usually too long. Instead, two CDR architectures are commonly used; the instantaneous locking CDR based on gated-oscillators [2] and the phase-picking CDR with over-sampling and digital processing capability [3].

This paper first describes the duty-cycle distortion problem in burst-mode optical transmission and its effects on the gated-oscillator-based CDR (GO-CDR). Then the interpolating-gated-oscillator-based CDR (IG-CDR) is proposed and simulation results are presented.

2 Duty Cycle Distortion in Burst-mode Optical Receiver

The general architecture of an optical receiver is shown in Fig. 2 [4]. First, optical signals are converted to current signals at the photo-diode, which are then converted to voltage signals by TIA (transimpedance amplifier). The limiting amplifier decides the received data bit as 'high' or 'low' with the threshold voltage supplied by

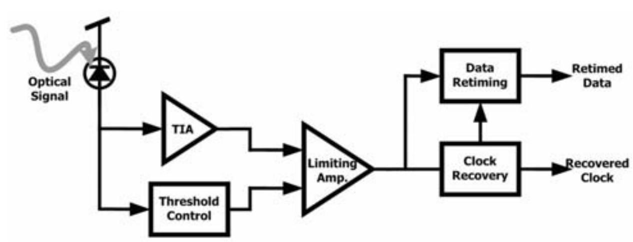

Fig 2. Optical receiver block diagram

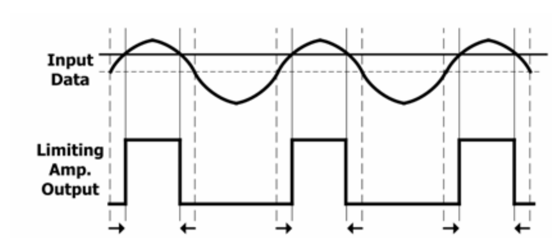

Fig 3. Duty cycle distortion in burst-mode receiver

the threshold control block. Then, CDR recovers the clock and the data.

In burst-mode, however, it is very difficult to obtain accurate threshold voltages, and inaccurate threshold voltages cause duty cycle distortion as shown in Fig. 3.

3 Gated Oscillator Based CDR

Fig. 4 shows the block diagram of a gated oscillator, in which an AND gate is added to a ring oscillator. The oscillator oscillates when the enable signal is 'high' and produces 'low' output when the enable signal is 'low'.

After the enable signal changes from 'low' to 'high', or at the rising edge of the enable signal, the output of the gated oscillator changes from 'low' to 'high'. Then after the propagation delay of 5 inverters and an AND gate, the output returns to 'low'. The output becomes 'high' after the same delay and oscillates continuously. This operation is essentially a phase reset.

The block diagram of GO-CDR is shown in Fig 5. There are two gated oscillators having enable signals with opposite signs. When the input data bit is 'high', the first gated oscillator starts to oscillate, and when the input data bit is 'low', the second gated oscillator starts to oscillate. When one gated oscillator oscillates, the other stops. Two output signals are combined in an OR gate, output of which is the clock signal that oscillates in synchronization with input data.

The control voltage generator is basically a PLL architecture. It provides control voltages for two gated oscillators to oscillate at the desired frequency.

Fig. 6 shows the operation of GO-CDR. Although not shown in Fig 6, the recovered clock passes through several gates resulting in phase difference with input data. An additional delay-cell is used in order to make input data experience the same amount of delay.

Since the gated oscillator resets its phase at the input data rising and gets synchronized to input data instantaneously, GO-CDR does not need any pre-amble bit sequence.

Now suppose that there is duty cycle distortion in input data as shown in Fig. 7. The duty cycle distortion is transferred to the recovered clock as shown in Fig. 7. Such clock signals cannot be used in other signal processing blocks. In addition, receiver BER can increase since sampling points (falling edges in clock for Fig. 7) for data retiming are not placed at the center of the data bit. Consequently, circuit techniques that can compensate this distortion must be considered.

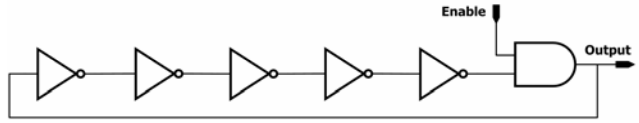

Fig 4. Gated oscillator block diagram

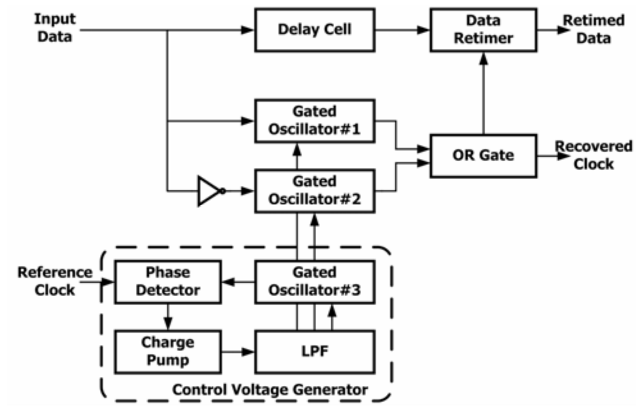

Fig 5. Block diagram for GO-CDR

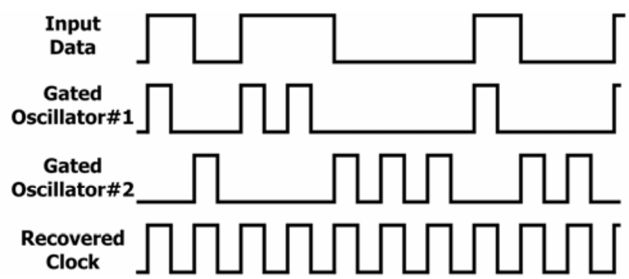

Fig 6. Operation of the clock and data recovery circuit using the gated oscillator

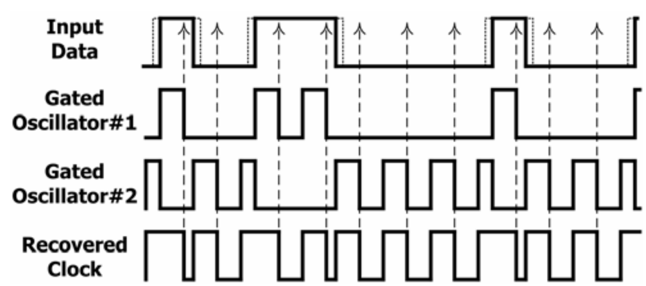

Fig 7. Effect of duty cycle distortion

4 Phase-Interpolating CDR

A new burst-mode CDR structure that is robust to duty-cycle distortion is proposed. As shown in Fig. 8, the interpolating-gated-oscillator-based CDR(IG-CDR) uses one of two outputs of the reset signal generator as the enable signal for each gated oscillator and the final clock

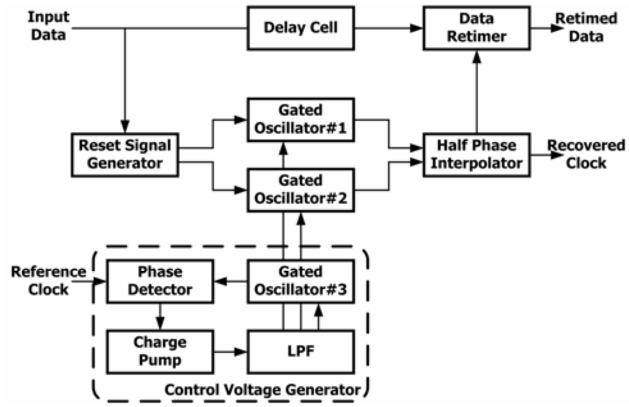

Fig 8. Block diagram for IG-CDR

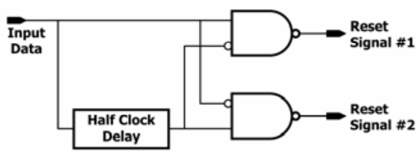

Fig 9. Block diagram for the reset signal generator

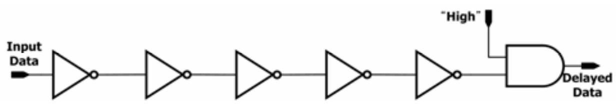

Fig 10. Block diagram for the half clock delay cell

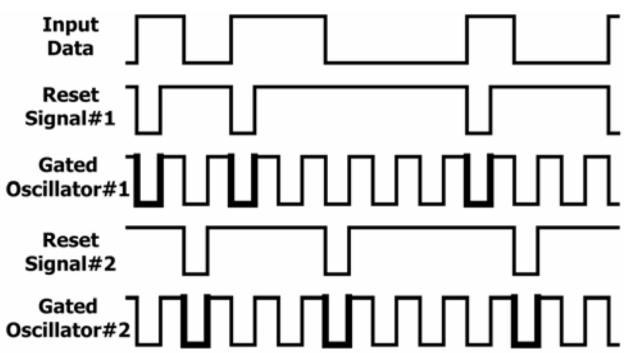

Fig 11. Operation of the reset signal generator

is realized with a half phase interpolator instead of an OR gate.

Fig 9 shows the reset signal generator which consists of a half clock delay cell and two NAND gates. The half clock delay cell (Fig. 10) is basically the gated oscillator with 'high' enable signal but without feedback loop. Input data pass through five inverters and an AND gate, duration of which is the half the oscillation period. The phase reset operation is marked as bold lines. CDRs using similar reset signals have been reported in [5], [6].

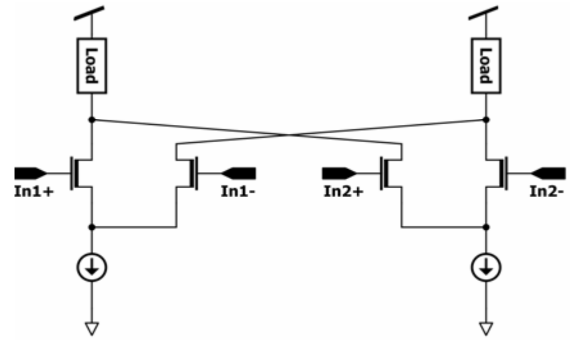

Fig 12. Half phase interpolator

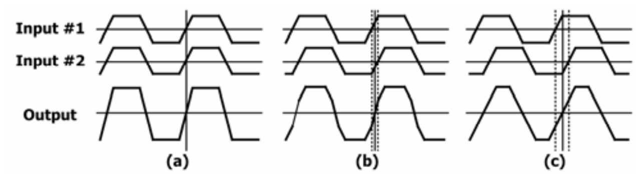

Fig 13. Operation of the half phase interpolator

As shown in Fig. 11, the reset signal generator produces two output signals having the duration of half the bit length. One is aligned with the rising edge of input data and the other is aligned with the falling edge.

The half phase interpolator is implemented with two differential pairs as shown in Fig. 12. The output of the half phase interpolator is equal to the sum of inputs. Fig. 13 shows two inputs and the output of the half phase interpolator. The phase is compared by the zero-crossing point where the sampling point is placed on. The zero crossing point of each clock is marked with dotted lines, and the zero crossing point of the output is marked with solid lines.

Fig. 13 (a) shows the case when there is no phase difference, and the sum of two inputs is just same as input. In Fig. 13 (b), there is a small phase difference between two inputs. In this case, first, at the rising of one input, the output starts to rise. When the second input starts to rise, the slope of the output becomes twice of the previous. When the first input stops rising, the slope of the output becomes same as the slope of one input. Finally, when the second input stops rising, the output also stops rising. At the falling cycle, similar changes in output signal occur. Consequently, the zero crossing point of the output is placed at the center between zero crossing points of two inputs.

The maximum phase difference that the half phase interpolator can interpolate is shown in Fig 13 (c). The interpolator doesn't work well if there is more phase difference because a flat section appears in the middle of the output of the interpolator.

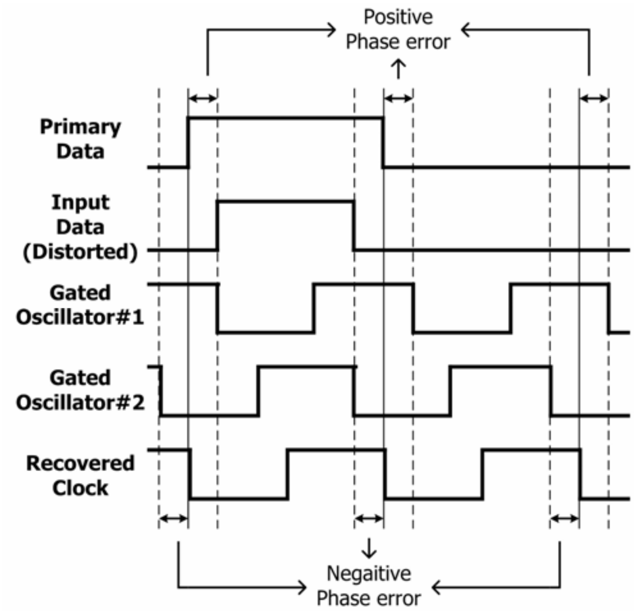

Fig 14. Operation of IG-CDR

Fig. 14 shows the schematic waveform of IG-CDR. The first gated oscillator resets its phase at the rising edge of the input data, and the second gated oscillator resets its phase at the falling edge of the input data. Then the first gated oscillator has positive phase error from the primary data and the magnitude of the error is equal to the amount of duty cycle distortion. The second gated oscillator also has same magnitude of negative phase error from primary data.

Since phase errors of two oscillator outputs have the same magnitude but the opposite sign, it is possible to make new clock with no phase error by summing them. The half phase interpolator achieves that. This new clock is not distorted by duty cycle distortion, and the BER decreases because the sampling point (the rising edge of the recovered clock in this figure) is placed on the center of the data bit.

GO-CDR doesn't need pre-amble because it always resets the phase at all transition of data. But IG-CDR needs the rising edge and the falling edge to reset the phase of each gated oscillators. So, IG-CDR needs two pre-amble bits, e.g. '1 0' or '0 1'.

5 Simulation Result

For comparison, we designed GO-CDR and IG-CDR for 1.25Gbps data rate by using 0.35 ㎛ CMOS process. The simulation was done by HSPICE.

Fig. 15 and Fig. 16 show eye diagrams for the recovered clock and the input data after passing the delay cell when duty cycle is 40% and 35 %, respectively. The top

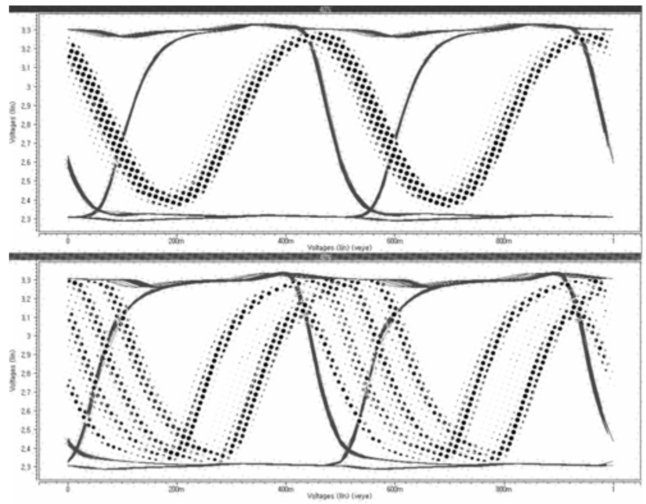

Fig 15. Data sampling point of (a) IG-CDR (b) GO-CDR with 40% duty cycle

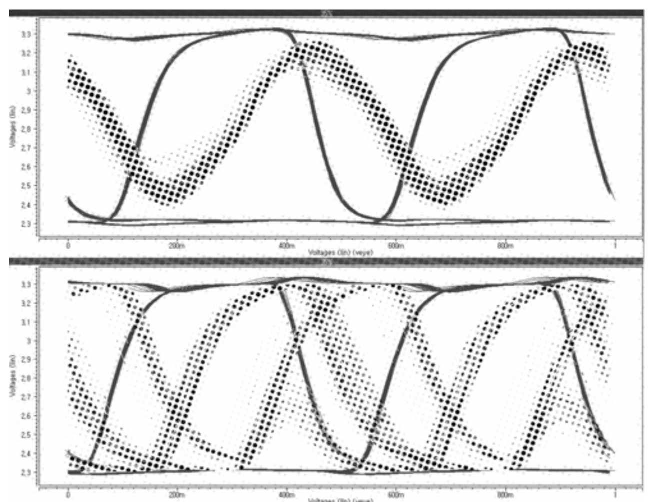

Fig 16. Data sampling point of (a) IG-CDR (b) GO-CDR with 35% duty cycle

figures (Fig. 15(a) and Fig. 16(a)) are for IG-CDR and the bottom figures (Fig. 15(b) and Fig. 16(b) are for GO-CDR. As shown, the clock recovered by GO-CDR is moving around the center of the data bit, and can miss a sample bit as shown in Fig 16(b). But the clock recovered by IG-CDR is always placed in the center of the data bit in both cases.

Fig. 17 and 18 are eye diagrams of the input data and the retimed data. The data retimed by GO-CDR is distorted like the input data because the recovered clock is also distorted. But the data retimed by IG-CDR is not affected by the input duty cycle distortion. The less than ideal duty cycle observed for IG-CDR is believed to be caused by internal blocks.

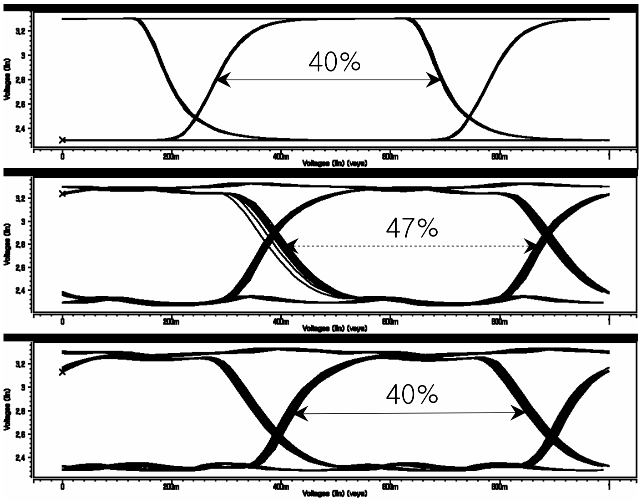

Fig 17. The eye diagram of (a) the input data (b) the retimed data by IG-CDR (c) the retimed data by GO-CDR with 40% duty cycle

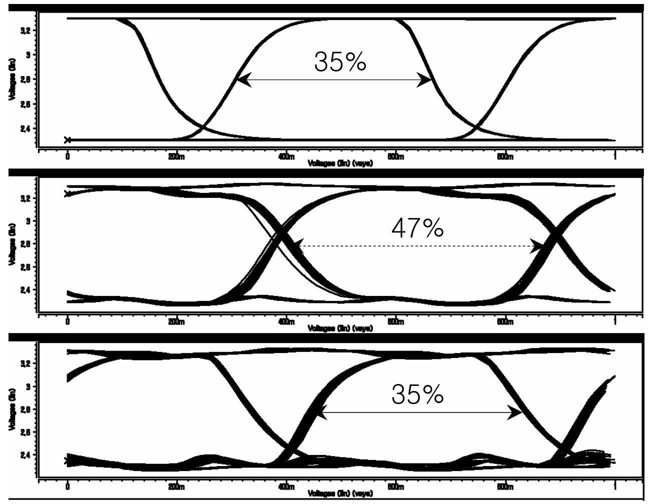

Fig 18. The eye diagram of (a) the input data (b) the retimed data by IG-CDR (c) the retimed data by GO-CDR with 35% duty cycle

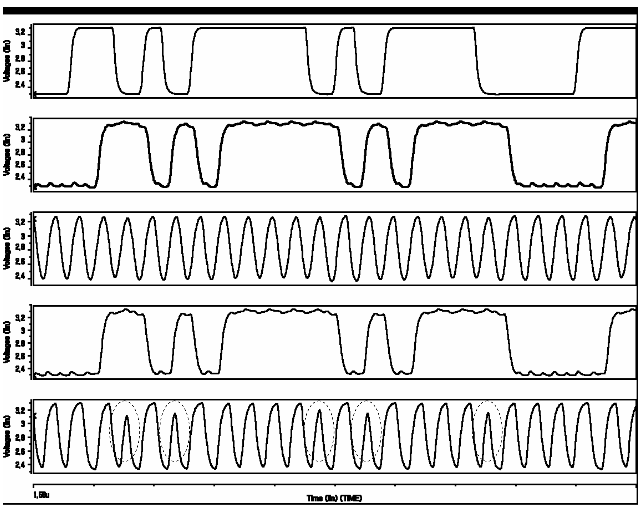

Fig 19. (a) The input data (b) The retimed data by IG-CDR (c) The recovered clock by IG-CDR (d) The retimed data by GO-CDR (e) The recovered clock by GO-CDR with 40% duty cycle

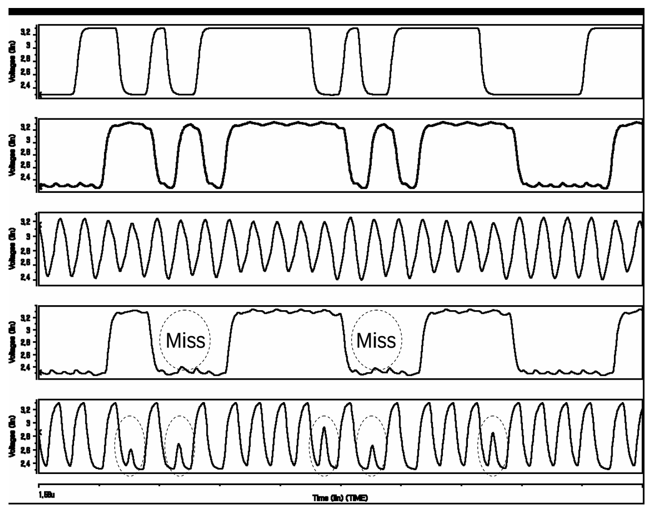

Fig 20. (a) The input data (b) The retimed data by IG-CDR (c) The recovered clock by IG-CDR (d) The retimed data by GO-CDR (e) The recovered clock by GO-CDR with 35% duty cycle

Fig. 19 and 20 show recovered clock and data for the random bit sequence. At the duty cycle of 40%, the clock recovered by GO-CDR is distorted seriously, and at 35%, the clock cannot be recovered. But IG-CDR recovers data well even with 35% duty cycle.

6 Chip Layout

IG-CDR layout is shown in Fig. 21. The area of CDR-core is $0.14\ \text{mm}^2$.

7 Conclusions

In burst mode optical receiver, duty cycle distortion occurs because the automatic threshold control block cannot work perfectly. If the gated oscillator based CDR is used, duty cycle distortion affects recovered clock and data directly, resulting in degraded system performance. A new CDR structure is proposed, which is robust to duty cycle distortion, and designed at 1.25 Gbps data rate by using $0.35\ \mu m$ CMOS process.

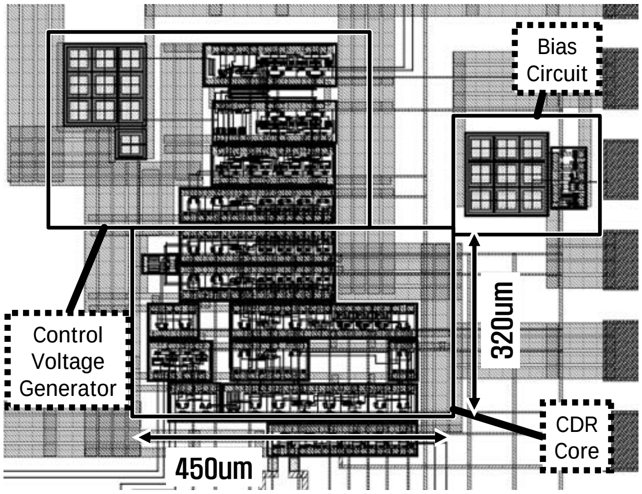

Fig 21. Layout of IG-CDR (450 ㎛ × 320 ㎛)

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