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Table of Contents

CD-ROM Help

Exit

Session 14	
	A Novel Gated-Oscillator CDR with Robustness to Duty Cycle Distortion Du-ho Kim, Pyung-su Han, Woo-Young Choi Department of Electrical and Electronic Engineering, Yonsei University
	* A Digital PWCL for Multi-Phase Clock Appliations Jun-Hyun Bae, Young-Chan Jang, Hong-June Park Department of Electronics and Engineering, Pohang University of Science and Technoloay
	Accurate Prediction of Jitter Tolerance in High-Speed Serial Links Ming-ta Hsieh, Gerald E. Sobelman Department of Electrical and Computer Engineering, University of Minnesota
	A 1.25Gb/s Digitally-Controlled Dual-Loop Clock and Data Recovery Circuit with an Improved Effective Phase Resolution Chang Kyung Seong, Seung-woo Lee*, Woo-young Choi Department of Electrical and Electronic Engineering, Yonsei University *Broadband Convergence Network Research Division, Electronics and Telecommunications Research Institute
	1.25/2.5-Gb/s Dual Bit-Rate Burst-Mode Clock Recovery Circuit Using Gated-Oscillators Pyung-Su Han, Woo-Young Choi, Department of Electrical and Electronic Engineering, Yonsei university

A 1.25Gb/s Digitally-Controlled Dual-Loop Clock and Data Recovery Circuit with an Improved Effective Phase Resolution

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Abstract - *A novel 1.25Gb/s digitally-controlled dual-loop clock and data recovery circuit (CDR) for multi-channel application is proposed. The CDR has a new configuration to improve the phase resolution. A prototype CDR was designed and fabricated in 0.18 ㎛ CMOS technology and its functions were verified with HSPICE simulation and chip measurement.*

Keywords: Clock and data recovery, phase interpolator , phase resolution

1 Introduction

As the demands for wideband networks and high-speed ICs grow, high-speed serial I/O systems become one of the most important blocks. In many cases, such as switch applications, dozens of transceivers have to be integrated on a single chip. Therefore, low power consumption and small chip area for data recovery circuits for such applications are very important issues.

A general phase-locked loop (PLL)-based clock and data recovery circuit (CDR) is not preferred in the multi-channel environments due to noise coupling problems between multiple transceiver modules [1]. Instead, dual-loop CDRs with a shared reference PLL and phase alignment blocks for each channel have been widely used. In the dual-loop CDR, the phase alignment block uses phase interpolator (PI) instead of voltage-controlled delay line (VCDL) to make continuous phase tuning in the range of 360°.

The dual-loop CDR using a PI can be classified in two categories, analog and digitally-controlled type. Due to the inherent characteristics of continuous phase generation capability, the CDR using analog PI has less jitter generation. However, it is sensitive to the supply and substrate noises, since all control behaviors are performed by analog signals. In the noisy environment due to switching noises from the adjacent digital logic core, analog controlled dual-loop CDR is not suitable. In the other hand, the digitally-controlled type is robust to the noise and easily controllable. However, it suffers from jitter performance degradation by self-dithering [2]. This is caused by the nature of inherent discrete phase generation of digitally-controlled PI. The phase resolution of the digitally-controlled dual-loop CDR is a critical parameter for the jitter performance.

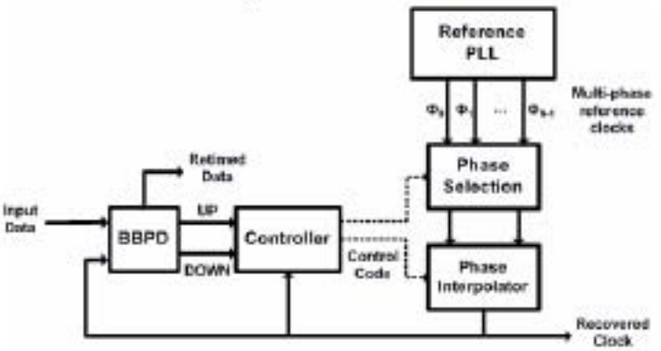

Figure 1. Block diagram of a conventional digitally-controlled dual-loop CDR

This paper presents a novel configuration with a digitally-controlled delay buffer (DCDB) to improve effective phase resolution of the digitally-controlled PI. In Section 2, we present an overview and problems in conventional digitally-controlled PI and CDR. A new structure of CDR to overcome these problems are described in Section 3. Behavioral, transistor-level simulation results and chip measurement results are given in Section 4 and 5, respectively.

2 Conventional Digitally-Controlled Dual-Loop CDR

2.1 Structure

Fig. 1 shows the block diagram of conventional digitally-controlled dual-loop CDR using a PI. The CDR contains a bang-bang phase detector (BBPD), controller, phase selection circuit and PI. Generally, the CDR accepts even numbers of multi-phase clocks, i.e. reference clocks,

from the reference PLL. The phase selection circuit selects two clocks having adjacent phases among them.

Two selected clocks are fed to the PI, which generates the interpolated clock with the target phase. In the phase selection and interpolation procedures, target phases are determined by the digital code from controller. The BBPD compares the phases of input data and recovered clock and generates UP or DOWN code. The controller decides the next states of phase selection circuit and PI using BBPD output. As a whole, the CDR forms a negative feedback loop and the phase of recovered clock tracks the phase of input data.

2.2 Phase resolution vs. CDR performance

The phase resolution of the CDR is related to three issues: jitter generation, jitter suppression and frequency offset tracking. Unlike the CDR with a continuous phase capability, the CDR with a discrete phase has non-zero jitter generation even for an ideally clean input data. Since the digitally-controlled dual-loop CDR generates quantized phase, the output clock phase dithers around the input data phase even in locked state. Moreover, some clock latencies in the loop degrade the jitter generation performance [3]. As one clock latency increases, additional two steps of peak-to-peak dithering occurs and the CDR loop becomes more unstable. In the aspect of jitter suppression, phase resolution is directly related to the loop bandwidth. For a higher resolution, the phase step that the CDR can jump in one clock cycle is small. Thus, the loop has narrow loop bandwidth and rejects high frequency jitter. However, this means that the CDR can not track a large frequency offset. The phase resolution of the CDR is lower-bounded by the frequency offset tracking ability and upper bounded by the jitter generation and jitter suppression performance.

2.3 Phase interpolator

The PI is a kind of analog multiplier and performs a phase mixing by taking the weighted summation of two clock signals with a certain phase difference. The resulting phase resolution is determined by the resolution of bias current DAC. The DAC can be divided into two categories by the control type: binary-weighted and thermometer type. In the binary-weighted type, high resolution current DAC is constructed with a few bits of code. But it suffers from bad dynamic characteristics and mismatching problems as the phase resolution increases. Although the thermometer type current DAC does not contain those problems, it is too bulky to implement high resolution. Therefore, it is difficult to realize high resolution PI. Generally, the phase resolution of PI is limited to about 4-bits in both cases.

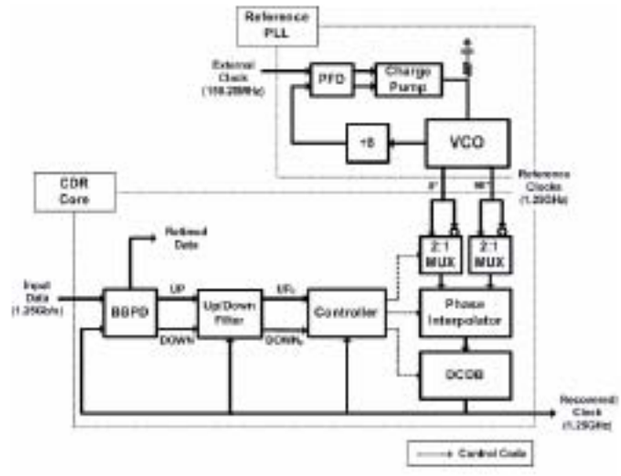

Figure 2. Block diagram of the proposed CDR

3 Proposed CDR

3.1 Structure

The block diagram of the proposed CDR is shown in Fig. 2. The CDR takes two differential quadrature phase clock from the reference PLL. Four-phase differential clocks are made from the quadrature phase clock by inverting the clock signals. Two quadrature clock signals are selected by 2:1 MUXs, relatively. They are interpolated by the PI and passed through DCDB for a higher phase resolution. Controller block contains MUX controller, PI controller and DCDB controller. The MUX controller and DCDB controller are a kind of 2-bits up/down counter, and PI controller is 15-bits bidirectional shift register to generate thermometer code. The generated clock is fed to the BBPD and the phase is compared. The UP or DOWN pulses from the BBPD is passed through Up/Down filter to reduce unwanted phase dithering [4]. The Up/Down filter counts the output sequence from the BBPD and outputs UP_F or $DOWN_F$ only when two consecutive UPs and DOWNs are occurred.

3.2 Digitally-Controlled Delay Buffer

The key idea is that the phase resolution can be easily increased using coarse and fine phase tuning methods. To insert more steps between each adjacent interpolated phase, the delay buffer with variable delay steps, i.e. DCDB, is used. The total phase resolution of CDR is multiplied by four by inserting the DCDB with a four-level, i.e. 2-bit, variable delay. Therefore, the proposed CDR has total 8-bits phase resolution with a 4-bit PI. Additional blocks of novel configuration are only DCDB and 2-bit counter as a DCDB controller. Fig. 3 shows simulated phase transfer characteristics of PI and DCDB combination using HSPICE. Although there are discontinuous points due to PI nonlinearity, total phase resolution is effectively increased to 256 levels.

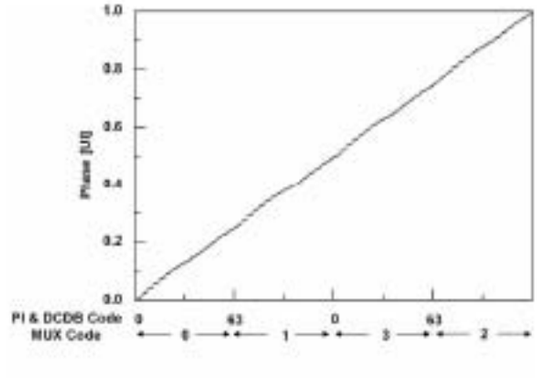

Figure 3. Phase transfer curve of the combination of 4-bits phase interpolator and 2-bits digitally-controlled delay buffer

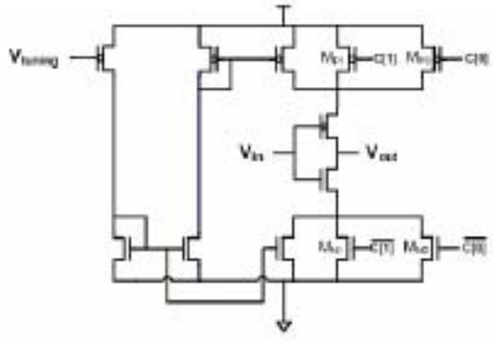

Figure 4. Schematic of the digitally-controlled delay buffer

As shown in Fig. 4, the DCDB is a simple current-steered CMOS inverter. The charging and discharging currents are digitally-controlled by $C_{[1]}$ and $C_{[0]}$ from the DCDB controller. By the binary-weighted control, the DCDB has four steps of variable delay. Since the DCDB and DCDB controller are simple CMOS gates, they consume only a negligible amount of power and occupy a small area.

The major problem of DCDB is unbounded phase characteristics. Therefore, it is not guaranteed that total phase transfer with the combination of PI and DCDB is monotonic for PVT variations. The amount of error by the PVT variation, Err_{DCDB}, can be defined as

$$Err_{DCDB}(\%) = \frac{\Delta\phi_{Error} - \Delta\phi_{Ideal}}{\Delta\phi_{Ideal}} \times 100 \qquad (1)$$

where $\triangle\Phi_{Ideal}$ is the target minimum delay of the DCDB and $\triangle\Phi_{Error}$ is slipped minimum delay of the DCDB due to the PVT variation, as shown in Fig. 5. In the prototype chip, the tuning voltage, V_{tuning}, is used as a bias voltage to control the DCDB error for the purpose of testing.

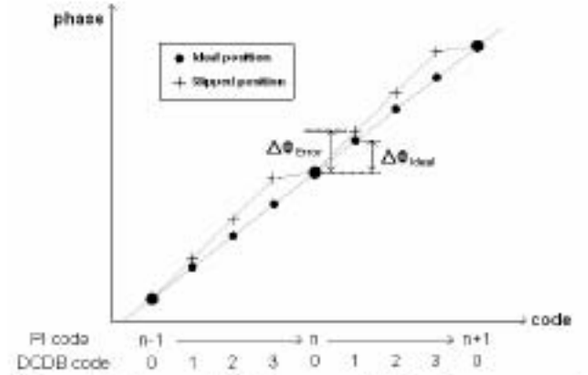

Figure 5. Concept of phase resolution improvement using DCDB and definition of the error of DCDB

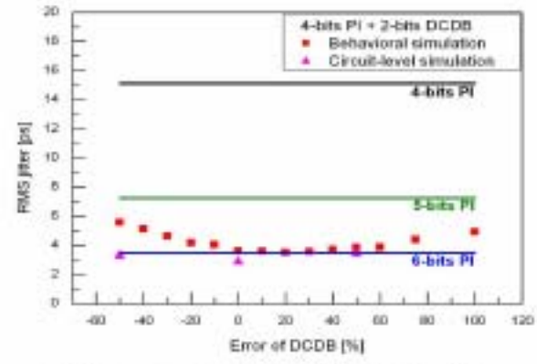

Figure 6. Behavioral and circuit-level simulation results

4 Simulation Results

Behavioral simulations were exercised by CPPSIM, C++-based time step simulator [5]. In the simulation, the degradation factors such as latency in the controller module, frequency offset and delay error of DCDB are considered. To verify the jitter generation performance of the CDR, simulation using an ideal random data input without jitter is tried for about 10000 clock periods. The frequency offset between the input data and reference clock is fixed at 200ppm. This value is a general specification in many standards. The peak-to-peak and RMS jitters are measured for the delay error of DCDB from -50% to 100%. To compare the jitter generation of the proposed CDR, the conventional configurations using only the PI with various phase resolutions are also simulated.

As shown in the Fig. 6, the jitter generation of the proposed CDR is close to the conventional CDR using only a 6-bits PI. As the error of DCDB increases, jitter generation performance is degraded and effective phase resolution is close to that of the CDR using 5-bits PI. However, the range in which jitter generation performance is better than the CDR using 5-bits PI is very wide.

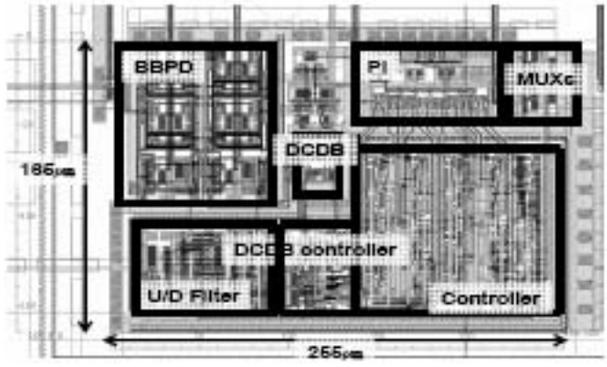

Figure 7. Layout of the prototype chip

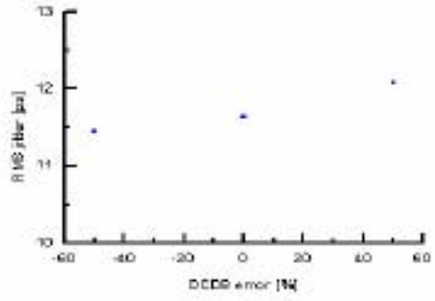

Figure 8. Measured jitter generation

The similar result is observed in the circuit-level simulation. Although the RMS jitter generated by the CDR is lower than the result of behavioral simulation, overall jitter performance is similar. The simulated power consumption is about 17.82mW with 1.8V supply, and chip area of CDR core is about 255×165 μm^2. The layout of the CDR core is shown in Fig 7.

5 Chip Measurement Results

The prototype chip operates at 1.25Gb/s in 2.0V supply. The CDR is able to track the input data which has ±400ppm frequency offset. The DCDB error is controlled with the tuning voltage, V_{tuning}. As shown in Fig. 8, the jitter generation level is almost flat for the DCDB error from -50% to 50%. Although the jitter level is higher than that of simulation result, it is observed that the jitter performance of the CDR is insensitive to the DCDB error.

To verify the jitter rejection ability, the input jitter was added by transmitting the input data through 2m PCB trace with 3.5m cable. As shown in Fig. 9, the CDR recovered a clean data and clock signal waveform from the eye-closed data.

6 Conclusions

This paper presents a novel configuration of digitally-controlled dual-loop CDR to improve phase resolution effectively. The phase resolution of the CDR is increased by a factor of 2-bits with the combination of PI and DCDB. It is verified that the effect of delay variation of DCDB is not critical in wide range. A prototype chip is designed in 0.18 μm CMOS technology and has 8-bits phase resolution effectively. The chip consumes 17.8mW and area was 255×165 μm^2.

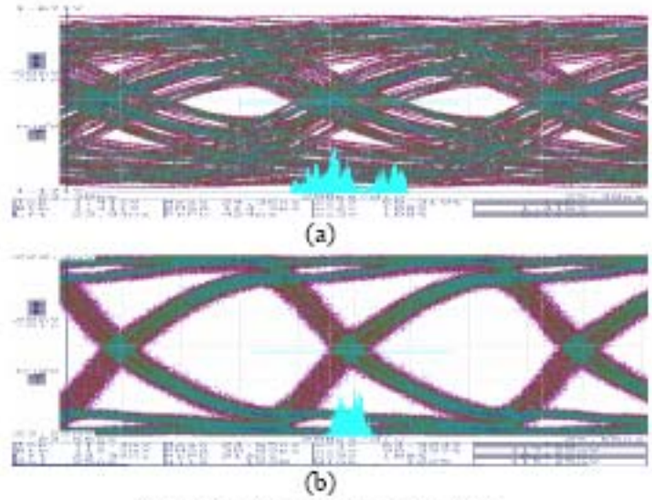

Figure 9. Measured eye diagram
(a) Input data : after 2m PCB trace and 3.5m cable, 0.53 UI_{p-p} eye closing (b) Recovered data : 0.265UI_{p-p} eye closing

Ackowledgment

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