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1.25/2.5-Gb/s Burst-Mode Clock Recovery Circuit with a Novel Dual Bit-Rate Structure in 0.18-μm CMOS

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***Abstract*—A burst-mode clock recovery circuit with a novel dual bit-rate structure is presented. It utilizes two gated-oscillators to align clock with data edges and can operate in half-rate clocking mode, doubling data throughput, as well as in full-rate clocking mode. The gated-oscillator reset-phase control scheme alters the starting phase of gated-oscillators repeatedly between 0° and 180° according to the current clock phase. A prototype chip was designed with 0.18-μm CMOS technology and 1.25/2.5-Gb/s dual-mode operation was verified in measurement.**

I. Introduction

Clock recovery techniques based on PLL (Phase-Locked Loop) or SAW (Surface Acoustic Wave) filters take a major portion of commercial clock recovery chip nowadays, because of their excellent jitter suppression performances. But they are not suitable for burst-mode receivers since it takes too much clock-acquisition time (long preamble bits) for them to acquire clock phases from data packets. Fast clock-acquisition is a major requirement for burst-mode receiver.

A number of fast clock-acquisition techniques [1], [2] for burst-mode clock recovery have been proposed so far. Among them, gated-oscillator approach [1] provides instantaneous locking and has a very simple structure. It is especially attractive for such burst-mode applications as LAN (Local Area Network) and PON (Passive Optical Network) in which jitter accumulation is not a major problem [3], since no repeaters are required. Besides, all-pass characteristics of gated-oscillator based clock recovery scheme offer decent jitter tolerance up to high frequency [4].

Recently published gigabit-rate PON standards (GPON, Gigabit PON and EPON, Ethernet PON) [5], [6] use burst-mode transmission at 1.25-Gb/s, and they are expected to be doubled to 2.5-Gb/s in near future. Therefore dual bit-rate clock recovery circuit that supports both 1.25-Gb/s and 2.5-Gb/s can be very useful. In this paper, we present a novel burst-mode clock recovery circuit which can operate in both half-rate and full-rate clocking mode.

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II. Gated-Oscillator Based Clock Recovery

GOCRC (Gated-Oscillator based Clock Recovery Circuit) was originally developed for magnetic drum data storage application in 1954 [7]. It is used for burst-mode receivers because of its instantaneous locking property. It is popular also in multi-channel receivers in which many receivers should be integrated on a single chip [8], because it takes small chip area and consumes low power.

Fig. 1 shows a schematic diagram of a gated-oscillator. A back-to-back connected delay stage chain and a gate stage (depicted as a NAND gate) form a ring oscillator. The gated stage turns on and off its oscillation. When the gate is closed ('Enable' is low), the feedback path is blocked and the oscillation stops.

When the gate is closed, the output of the oscillator is dominated by the gate stage and remains high (logic-value). This can be understood as the clock phase stuck at 0°.

Oscillator can be re-activated by setting 'Enable' high. Then, the clock phase is automatically synchronized with 'Enable' signal. It is because the blocked feedback path, node 'x', is loaded with the same logic-value (high) with the output, therefore it guarantees that oscillation always starts with falling edge (in terms of clock phase, 0°). GOCRC utilizes this property to align clock signals to data bits. Fig. 2 shows an example of a GOCRC.

Two gated-oscillators are turned on and off alternately by 'Burst data' acting as 'Enable' signal shown in fig. 1. The free-running oscillation frequencies of gated-oscillators are tuned in the vicinity of data-rate by sharing the VCO

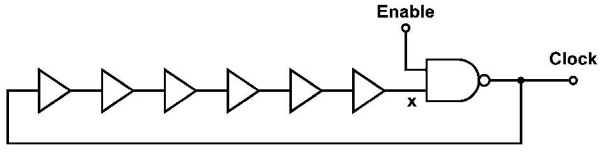


Figure 1. Schematic diagram of gated-oscillator

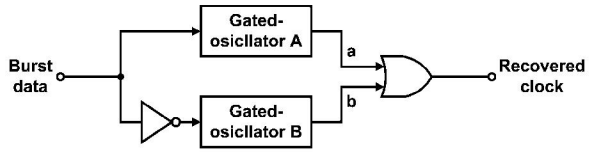


Figure 2. Example of a GOCRC

(Voltage Controlled Oscillator) control voltage of a reference PLL which is locked by the reference clock.

When 'Burst data' is high (logic-one), 'gated-oscillator A' is activated and it generates data-aligned clock. When 'Burst data' is low (logic-zero) and 'gated-oscillator B' is activated and it generates clock. Therefore each gated-oscillator covers half portions of 'Burst data'. Two outputs of gated-oscillators are combined by an OR gate to generate complete clock signal. An example of signal waveforms is shown in fig. 3.

Frequency mismatch between the gated-oscillator pair and the frequency biasing PLL may result in clock-phase-drift when a long CID (Consecutive Identical Digit) is applied. Therefore run-length limiting coding scheme such as 8b10b code is indispensable [4]. In our previous work [9], it was found that oscillation frequencies of identical oscillator circuits fabricated on the same die can vary up to two or three percent in typical CMOS process. Assuming that one oscillator is three percent faster or slower than the other, 8b10b code whose maximum length of CID is five gives clock-phase shift of 0.15UI at worst case. This should be is tolerable in most clock recovery applications.

III. Proposed Half-Rate Clock Recovery Principle

Half-rate clocking scheme is very popular especially for high-speed memory I/Os. It uses both rising and falling edges of clock signal for bit locations to relieve device speed requirements.

As described in section II, GOCRC utilizes clock-phase resetting ability of gated-oscillators. Since the GOCRC shown in fig. 2 has clock phase set at 0° (falling edge) at every data transition, the opposite clock phase of 180° (rising edge) which corresponds to the center position of data bits can be used for data sampling.

For half-rate clocking, clock phases at sampling points alter between 0° and 180° along data bit sequence, e.g., 0° for even bits and 180° for odd bits. In our design, a modified

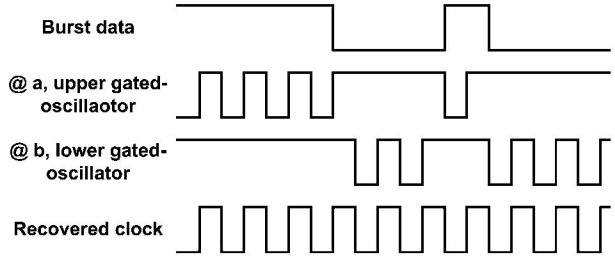


Figure 3. Clock recovery waveforms of GOCRC in fig.2

version of gated-oscillator is used for half-rate clocking as shown in fig. 4.

The gated-oscillator shown in fig. 4 uses two multiplexers as its gate stages. Terminal 'a's are selected to form a ring oscillator, and terminal 'b's are selected to turn it off. It has four possible internal states, clock phase 0°, 90°, 180 ° and 270 ° when turned off, according to the combination of logic-values of 'R0' and 'R1'. We may use 'R0' and 'R1' to make the oscillator have proper reset phase in half-rate clocking operation. In contrast, conventional type shown in fig. 1 has only one possible state, clock phase 0°.

Fig. 5 shows clock phase definition used in our design and four possible reset phases. Because 'R0' and 'R1' are the very output value that 'x0' and 'x1' have just before oscillation starts, Proper 'R0' and 'R1' values can be easily determined. For example, if we make both 'R0' and 'R1' logic-high, the gated-oscillator would make its output start at 0°. If we use logic-low for 'R0' and 'R1', oscillation will start at 180°.

Fig. 6 shows a half-rate clock recovery circuit realized with the modified gated-oscillator. 'R0' and 'R1' of each gated-oscillators are tied together because we need only two reset phases for half-rate clocking, 0° and 180°.

When, for example, 'Data' is logic-high and 'Gated-oscillator A' is activated, data-aligned clock is found at node 'Rb' and it is also used as reset-phase control signal of 'Gated-oscillator B', and vice versa. This configuration makes it possible for stopped gated-oscillator to determine

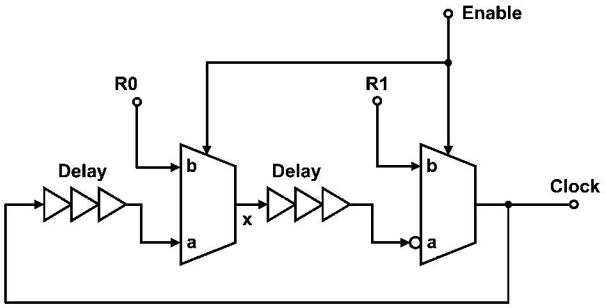


Figure 4. Proposed gated-oscillator circuit for half-rate clocking

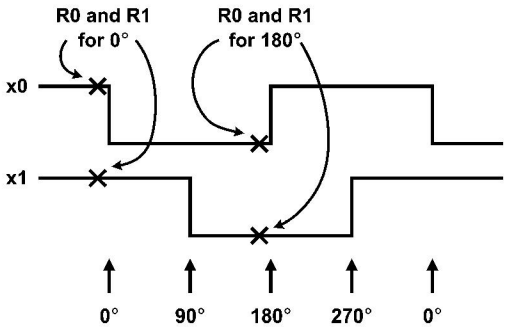


Figure 5. Clock phase definition

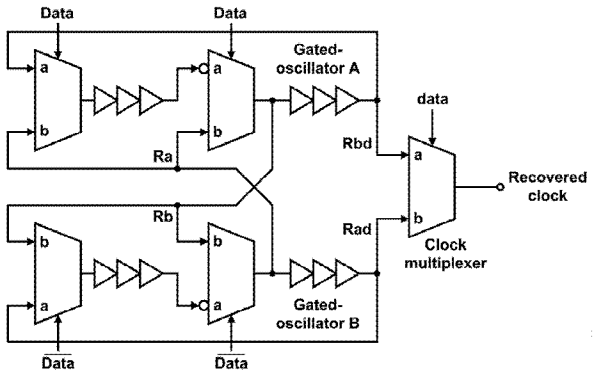


Figure 6. Proposed half-rate GOCRC

the right phase for next data transition.

Half portions of data-aligned clock are generated at each output terminal of gate stages, 'Ra' and 'Rb'. They are combined by 'Clock multiplexer' to produce complete recovered clock. Data signal can be used as selection signal of clock multiplexer because data polarity reflects which oscillator is active.

Finally, as can be seen in fig. 6, the delayed version of clock is used for output because clock should be shifted by a half of bit interval (or 90° of clock phase) for proper decision in half-rate clocking mode. Therefore 'Rad' and 'Rbd' are applied to clock multiplexer instead of 'Ra' and 'Rb'. After clock multiplexer, 'Recovered clock' lags by a fourth of clock period, which equals a half of bit interval.

IV. Dual Bit-Rate Operation

Modified gated-oscillator in fig. 4 can be also used for full-rate clock recovery by fixing 'R0' and 'R1' to a constant logic value, e.g. logic-high. Then it would operate in the same way as the conventional one shown in fig. 1.

By utilizing this programmability of reset phase, the clock recovery circuit shown in fig. 6 can be used for full-rate clock recovery as well as half-rate clock recovery. In our design, this was implemented by adding two multiplexers with a constant value on their one input (not shown in fig. 6) in reset-phase control signal ('Ra' and 'Rb' in fig. 6) path. The additional multiplexers are controlled by external mode-selection signal.

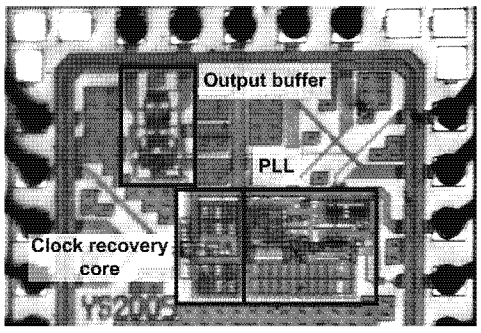
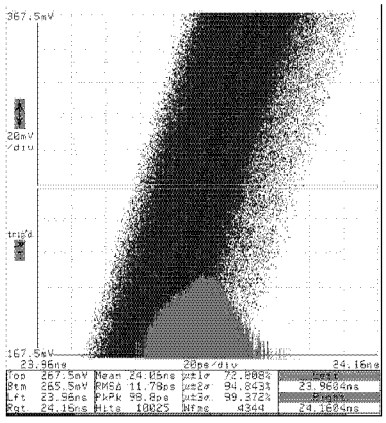
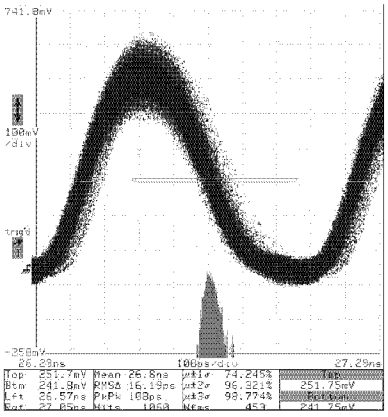


Figure 7. Die photograph of prototype chip



a) Recovered clock and histogram of mid-crossing points from 1.25-Gb/s 2^7-1 PRBS pattern



b) Recovered clock and histogram of mid-crossing points from 2.5-Gb/s 2^7-1 PRBS pattern

Figure 8. Recovered clock from 1.25-Gb/s 2^7-1 PRBS pattern

V. Prototype Chip and Measurement Results

Designed circuit was laid out and fabricated with 0.18-μm CMOS technology. Prototype chip was directly attached to test board assembly using COB (Chip On Board) technique, because lack of high-speed package available to us. Fig. 7 shows microscopic photograph of fabricated prototype chip. Clock recovery core occupies only 160-μm x 250-μm and frequency biasing PLL requires 310-μm x 250-μm.

Fig. 8 shows recovered clock waveforms and histograms of clock mid-crossing points from 2^7-1 PRBS pattern at 1.25-Gb/s and 2.5-Gb/s. The measured clock jitters were around 100-ps peak-to-peak for both cases. Because the data source is virtually jitter-free, observed jitters are entirely from the clock recovery circuit.

The lightly shaded region in the right side of fig. 8-a) is caused by clock-phase drift due to frequency mismatch described in section 2. In this case, clock-recovering gated-

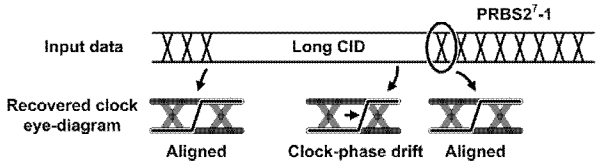


Figure 9. Instantaneous phase acquisition after a long CID interval in case of the gated-oscillator pair leads frequency biasing PLL

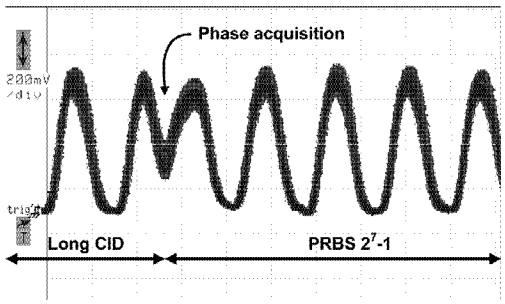


Figure 10. Instantaneous phase-acquisition

oscillator pair is slightly leads the frequency biasing PLL. In case of lagging, it would appear in the left side.

For verifying instant phase alignment, intentional phase-drift was made by data sequence having long CID, and fig. 9 describes what it affects recovered clock. If oscillating frequencies of clock-recovering gated-oscillators are not equal to that of frequency biasing PLL, recovered clock edge drifts out of the center of data eye-diagram during long CID interval where there is no data transition. After the CID, GOCRC brings clock edge to the center of data eye, therefore an abrupt phase jump would be observed. Fig. 10 shows instantaneous phase-acquisition was performed successfully.

Frequency mismatch was calculated. Data pattern having all 1's used as data input and output clock frequency was measured with the spectrum analyzer. Data having all 1's make only 'Gated-oscillator A' active. The same measurement was performed with all 0's data pattern for 'Gated-oscillator B', too. Calculated frequency mismatch between gated-oscillator A and B in clock recovery circuit was less than two-percent over the entire operational frequency range.

TABLE I. MEASUREMENT RESULTS SUMMARY

Technology	0.18-μm CMOS
Nominal data-rate	1.25-Gb/s and 2.5-Gb/s (dual bit-rate)
Operational freq. range	1.1-Gb/s ~ 1.35Gb/s and 2.2Gb/s ~2.7Gb/s
Chip area	160-μm x 250-μm for core 310-μm x 250-μm for freq. biasing PLL
Max. tolerable CID	More than 7bits
Jitter generation	Around 100-ps (p2p) for 1.25-Gb/s and 2.5-Gb/s
Power supply	1.8V
Power consumption	60-mW for core, 50-mW for Output buffer

VI. CONCLUSION

A novel structure of dual bit-rate burst-mode clock recovery circuit was demonstrated. It can operate in half-rate clocking mode with doubled operation speed, as well as in full-rate clock recovery mode. Two operation modes can be easily selected by an external selection switch. The circuit was designed and laid out with 0.18-μm CMOS technology, and prototype chip was fabricated.

Some PWD was observed in simulation, which was caused by clock-phase-drift due to frequency offset between oscillators in clock recovery circuit and frequency biasing PLL. This problem can be mitigated by using limited-CID coding scheme, e.g., 8b10b code that limits maximum run-length of CID to 5bits.

Calculated frequency mismatch between clock recovery gated-oscillators is less than two percent over the entire operational frequency range, which agrees well with our previous work and expectation. Careful design and lay-out would minimize the undesirable frequency mismatches.

For clock recovering tests, PRBS 2^7-1 pattern was used which has maximum run length of 7bits. Prototype chip successfully recovered full-rate and half-rate clock from each 1.25-Gb/s and 2.5-Gb/s PRBS patterns. Finally, Table 1 sums up the measurement result.

ACKNOWLEDGEMENT

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