Equivalent Circuit Model of CMOS-based Single-Photon Avalanche Diodes: Device Analysis and Optimization

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Yonsei University
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감사의 글

최고의 회로를 설계하겠다는 큰 꿈을 안고 서울로 올라와 연구를 시작한 게 엊그제 같은데, 벌써 2 년이라는 시간이 지나 이렇게 감사의 글을 쓰고 있자니 감회가 새롭습니다. 석사 과정 동안 도움을 주신 분들이 너무나도 많기에, 이 글로 감사의 마음을 전하고자 합니다.

먼저, 연구의 방향을 제시해 주시고 항상 아낌없는 지도와 격려를 보내주신 이명재 교수님께 진심으로 감사의 말씀을 드립니다. 부족한 저를 믿고 새로운 도전의 기회를 주신 덕분에 이 논문을 완성할 수 있었습니다. 교수님의 가르침은 연구자로서뿐만 아니라 한 사람으로서도 한 단계 성장하는 데 큰 힘이 되었습니다. 또한, 처음 연구를 시작할 기회를 주시고 지원해주신 최우영 교수님, 심사위원으로 참여해주신 채영철 교수님께도 감사의 말씀드립니다.

함께 고민하고 성장하며 연구실에서 기쁨과 어려움을 나눈 ADS 연구실 동료 분들께도 감사의 인사를 전합니다. 선배 연구자로서, 좋아하는 형으로서 존경하는 은성 형님, 함께 회로를 꿈꾸던 효성 형님, 따뜻한 말로 챙겨주던 현승 형님, 고민이 있으면 언제든 들어주던 주현 형님, 분위기를 밝게 만들어주는 도윤 형님, 첫 후배 세영씨, 그리고 두희씨, 진심을 다해 감사드립니다. 여러분 덕분에 힘든 시간도 이겨낼 수 있었습니다.

마지막으로, 동생 예온과 멀리 거제도에서 저를 믿어 주시고 응원해주시는 아버지, 어머니께 무엇보다 가장 큰 감사의 마음을 전합니다.

앞으로도 초심을 잃지 않고, 꿈을 향해 꾸준히 정진하며 연구자로서 성장해 나가겠습니다.

2025년 1월, 석사생활을 마치며

김 어 진 올림

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ABSTRACT

Equivalent Circuit Model of CMOS-based Single-Photon Avalanche Diodes: Device Analysis and Optimization

Single-photon avalanche diodes (SPADs) are highly sensitive detectors capable of capturing single photons, even in the near-infrared (NIR) range. Additionally, advancements in CMOS technology enable SPAD to be integrated with electronics in a cost-effective and customizable manner. Due to their capabilities and compatibility, SPADs have been widely applied in fields, including time-of-flight (ToF) systems, light detection and ranging (LiDAR), augmented reality (AR), virtual reality (VR), medical imaging, and positron emission tomography (PET). Additionally, they are increasingly used in quantum technologies, such as quantum key distribution, quantum random number generators (QRNG), quantum computing, and integrated quantum photonics. The photon detection probability (PDP) and noise factors—comprising the dark count rate (DCR) and afterpulsing are critical factors in determining the performance of these applications. A comprehensive understanding of a SPAD's intrinsic properties is essential for optimizing its design and improving performance. This thesis proposes an equivalent circuit model for CMOS-based SPADs, comprising key device parameters, including parasitic components, obtained through a de-embedding process. The modeling results demonstrate that the conventional high-voltage P-well (HVPW) guard-ring structure contributes to high internal series resistance. Based on this model, an optimized guard-ring structure has been proposed.

Furthermore, as interest in SPAD miniaturization continues to grow, this work analyzes the impact of size variation on device parameters. Finally, the equivalent circuit model, which accurately reflects impedance characteristics, is incorporated into a conventional Verilog-A model to enhance accuracy regarding static and dynamic behaviors. This integration facilitates the optimization of analog front-end (AFE) designs in a commercial circuit simulator.

Keywords: CMOS image sensor (CIS), direct time-of-flight (d-ToF) sensor system, equivalent circuit model, guard-ring optimization, optical sensor, photodiode, photodetector, single-photon avalanche diode (SPAD), size optimization, SPAD miniaturization, SPAD modeling, SPAD optimization, Verilog-A model

1. Introduction

1.1. SPAD

Single-photon avalanche diodes (SPADs) operate in Geiger mode when a reverse bias voltage exceeding the breakdown voltage (V_{BD}) is applied. If photons enter the SPAD, they generate carriers in this state that can trigger avalanche multiplication, resulting in a high current flow. This breakdown is quenched by a quenching transistor, allowing the SPAD to recharge to its original state. The SPAD produces a digital output pulse for each photon detected, as shown in Fig. 1-1.

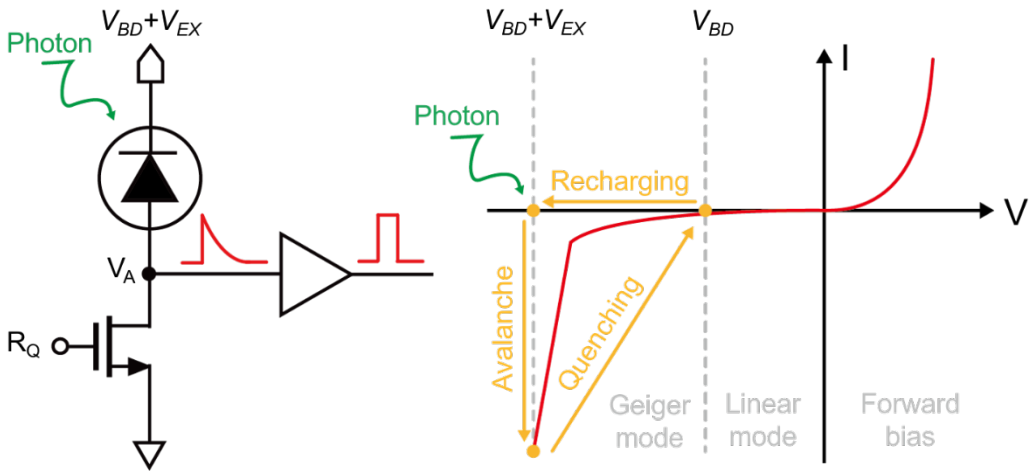


Fig. 1-1. SPAD operation.

1.2. Motivation

Due to their ability to detect single photons, SPADs are widely used in arrays for sensor systems in time-of-flight (ToF) applications, including light detection and ranging (LiDAR) [1], [2], [3], [4], [5], [6], [7]. They are also extensively utilized in medical fields, such as fluorescence lifetime imaging and positron emission tomography (PET) [8], as well as in quantum applications [9], [10] like quantum computing [11] and quantum random number generators (QRNG) [12]. Despite the widespread applications of SPADs, research on the intrinsic device parameters and parasitic components within SPAD devices remains limited. This thesis addresses this gap by extracting the intrinsic properties of CMOS-based SPADs through detailed modeling of the development of an equivalent circuit. This equivalent circuit provides a deeper understanding of the SPAD by revealing the correlation between its parameters and characteristics. It also enables the comparison and analysis of different SPADs within the same framework, facilitating modeling-based optimization to enhance SPAD performance. Furthermore, integrating these findings into a Verilog-A model that accurately represents the RC components of the device enables circuit-level simulations, contributing to analog front-end (AFE) optimization.

1.3. Outline

This thesis proceeds as follows:

- Chapter 2 introduces the equivalent circuit model of the SPAD through parameter extraction encompassing S-parameter measurements, TCAD simulations, and Advanced Design System (ADS) analysis.
- Chapter 3 proposes modeling-based guard-ring optimization and examines performance improvements.
- Chapter 4 discusses the trade-offs of SPAD miniaturization, analyzed through modeling parameter comparisons based on variations in SPAD size.
- Chapter 5 presents the Verilog-A model of the SPAD and analyzes the results of circuit simulations.
- Chapter 6 summarizes the thesis and proposes future work based on the significance of the modeling.

2. Equivalent circuit model of the SPAD

2.1. Device structure and model of the SPAD

The SPAD used for modeling was a PN-type SPAD with a P + / N-well (NW) junction fabricated using a GF 55 nm bipolar-CMOS-DMOS (BCD) process. The device structure is depicted in Fig. 2-1. A Deep NW layer was employed to isolate the junction from leakage caused by substrate defects and to extend the carrier absorption region [13]. The diameter of the junction's active area and the guard-ring (GR) size are designed to be 13.5 μm and 1.8 μm, respectively. Due to the significant doping concentration difference near the edge of the P + / NW junction, premature edge breakdown (PEB) may occur, leading to a degradation in photon detection probability (PDP). To mitigate PEB, a guard ring (GR) layer with a lower doping concentration than the junction was introduced. This GR layer utilized a deeply doped high-voltage P-well (HVPW) layer to perform the GR function effectively. Based on these layers in the SPAD structure, the equivalent circuit model was constructed as a first step. For the equivalent circuit model, a lumped model reflecting its impedance characteristics was used to accurately determine the physical device parameters for a deeper understanding.

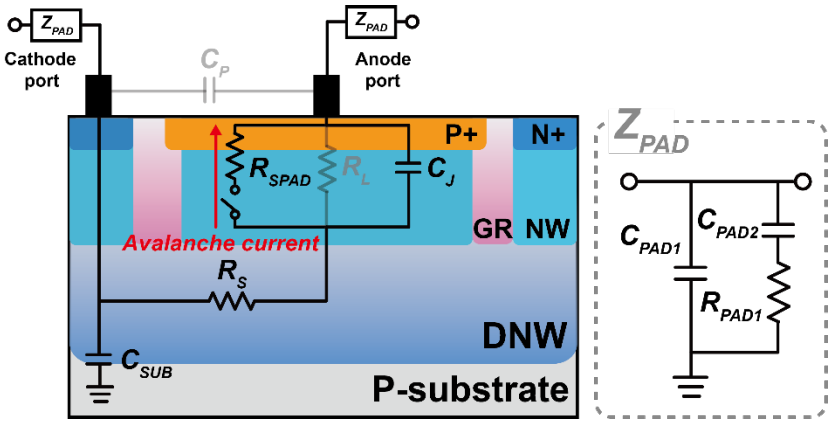


Fig. 2-1. Device structure and equivalent circuit model of the PN-type SPAD under excess bias conditions.

Fig. 2-1 presents the equivalent circuit model of the SPAD under excess bias conditions. This marks the first introduction of a SPAD model that includes the space-charge resistance [14] with accurate values extracted through S-parameter measurements. The depletion region formed at the junction is modeled using the parallel resistance R_L and capacitance C_J. The resistance R_L represents the leakage current and typically has a high value compared to other components, making it negligible considering impedance characteristics. When the breakdown voltage (V_{BD}) is exceeded, the electric field intensity in the depletion region becomes strong enough to accelerate free electrons, causing them to collide with atoms and generate electron-hole pairs. This phenomenon, known as impact ionization, allows even a single photon to produce a significant number of carriers. Assuming that the generated carriers move at saturation velocity, a saturation current flows

in the space-charge region (depletion region). The flow of these carriers alters the electric field, leading to a voltage distribution. Using the relationship between the saturation current and the voltage distribution in the space-charge region, the space-charge resistance can be defined [14]. The resistance R_{SPAD} represents the space-charge resistance and is only observed under excess bias conditions. This resistance demonstrates why the current resulting from avalanche multiplication has a limited value. The series resistance R_S corresponds to the resistance of the drift region of the NW and the inactive region of the DNW. C_P represents the parasitic capacitance between the electrodes, which is negligible due to its low value of only a few femtofarads (fF). Similarly, C_{SUB} denotes the parasitic capacitance between the DNW and the P-substrate.

Additionally, the parasitic components of the SPAD pads can be modeled. In Z_{PAD}, C_{PAD1} is the parasitic capacitance of the pad's bottom metal layer, while C_{PAD2} and R_{PAD1} are the leakage and parasitic components between the PAD and substrate. R_{PAD1} accounts for the parasitic components from the slit in the shield metal.

2.2. Parameter extraction

First, a ground-signal-ground (GSG) pad for the SPAD was designed to facilitate the extraction of parameter values in the equivalent circuit model, as shown in Fig. 2-2. The GSG pad provides stability in high-frequency impedance characteristic measurements for

lumped model construction and enables de-embedding by allowing independent measurement of the pad itself [15], [16]. Next, calibration was performed to eliminate errors arising from the experimental system, such as probe effects, excluding the device under the test (DUT). Subsequently, two-port S-parameter measurements of the GSG pad for the SPAD were conducted up to 20 GHz using a vector network analyzer to extract its impedance characteristics. The extracted impedance parameters of the pad were then subtracted from the measured impedance characteristics of the DUT to isolate the intrinsic properties of the SPAD. The initial values of each device parameter were determined based on known equations. These values were then fine-tuned by comparing the simulation results from the ADS tool with the measured S-parameter data.

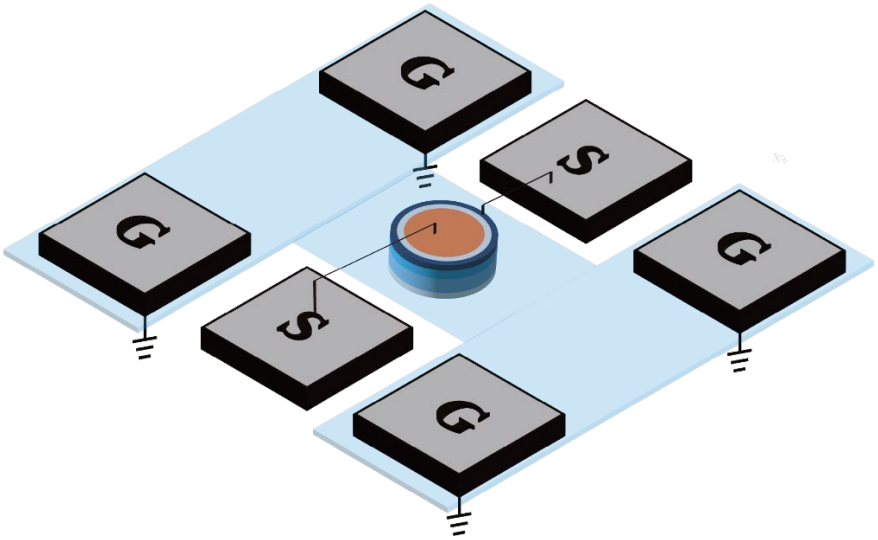


Fig. 2-2. Conceptual design of the GSG pad for the SPAD.

S-parameters were measured at the V_{BD} and V_{EX} 3 V, after which parameter extraction was performed. It was reported that both R_S and C_J do not vary significantly with changes in bias [17], [18]. Therefore, parameter values were initially extracted based on known equations and adjusted using the ADS tool, excluding R_{SPAD}, which is only observed under the excess bias condition. Subsequently, without altering the values of other parameters, the value of R_{SPAD} was determined and finely tuned using the same process at V_{EX} 3 V. Each of the parameters, C_J and R_{SPAD}, was calculated using the following equations [14]. In these equations, W_D is the thickness of the depletion region, A is the cross-sectional area of the active area, χ_A is the avalanche width, ε_s is the permittivity of the material, and ν_s is the saturation velocity of the carriers. The values for W_D, χ_A were obtained using TCAD simulation.

$$C_j = \frac{\varepsilon_s A}{W_D}, R_{SPAD} = \frac{(W_D - \chi_A)^2}{2A\varepsilon_s \nu_s} \quad (1)$$

The impedance equation (4), which shows a dominant correlation with R_S and C_J, was plotted using the ADS tool to adjust the values finely. For this purpose, the equivalent circuit model, configured in a two-port network, was assumed to be a π-network for calculating the Y-parameters, as shown in Fig. 2-3. Under this assumption, the Y-parameter at the Y3 section is represented as Y_{12}. Consequently, it was determined that the real part

of Y_{12} primarily represents R_S, while the imaginary part predominantly represents C_J. The calculation process for this adjustment is detailed below.

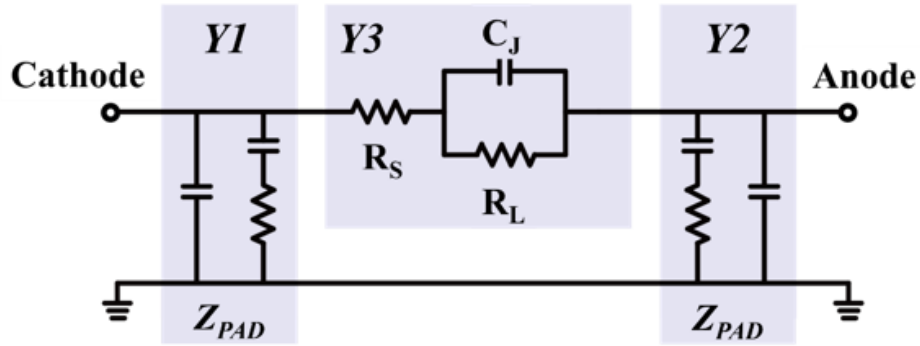


Fig. 2-3. Schematic of the equivalent circuit model at V_{BD} with a π network assumption.

$$j\omega C_j + \frac{1}{R_L} \approx j\omega C_j, \qquad Y_{12} \approx j\omega C_j \parallel \frac{1}{R_S} \tag{2}$$

$$Y_{12} \approx \frac{j\omega R_S C_j}{R_S + j\omega C_j} = \frac{\omega^2 R_S {C_j}^2 + j\omega {R_S}^2 C_j}{{R_S}^2 + \omega^2 {C_j}^2} \tag{3}$$

$$\therefore Y_{12} \approx \frac{\omega^2 {C_j}^2}{R_S} + j\omega C_j \ (\because {R_S}^2 \gg \omega^2 {C_j}^2) \tag{4}$$

Fig. 2-4 presents the measured and simulated Y_{12} results at V_{BD} following the adjustment process. The extracted parameter values are shown in Table 1.

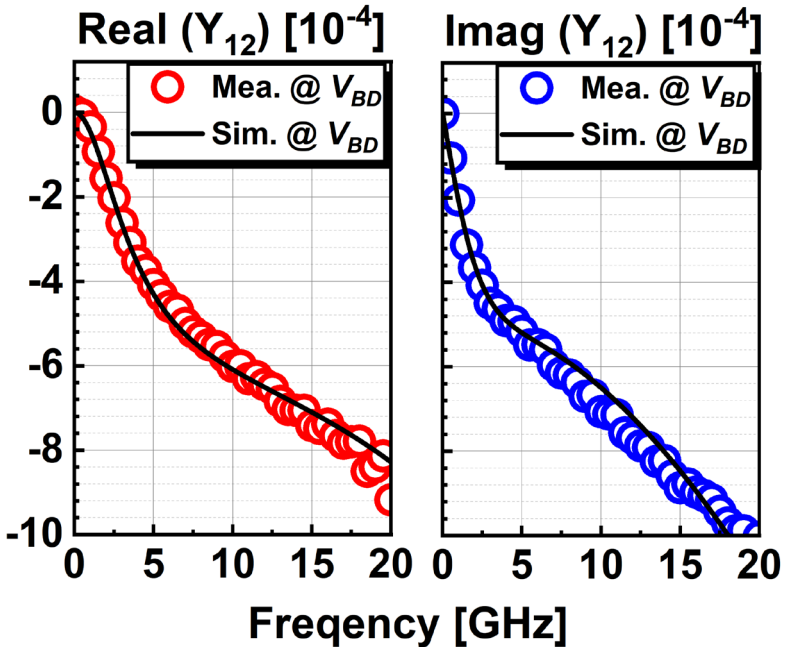


Fig. 2-4. Comparison of the measured and simulated Y_{12} results at V_{BD}.

Table. 1. Extracted parameter values of the equivalent circuit model.

PAD Model		Device Model	
C_{PAD1} [fF]	45	R_S [kΩ]	1.9
C_{PAD2} [fF]	225	R_{SPAD} [Ω]	130
R_{PAD1} [Ω]	110	C_J [fF]	28

2.3. Modeling results

The simulation and measurement results for the impedance characteristics of the SPAD at both V_{BD} and V_{EX} 3 V are shown in Fig. 2-5. The good agreement between the measured and simulated S_{22} characteristics at V_{BD} and V_{EX} 3 V confirms the accuracy of the modeling. It demonstrates that the equivalent circuit model effectively reflects the SPAD's behavior.

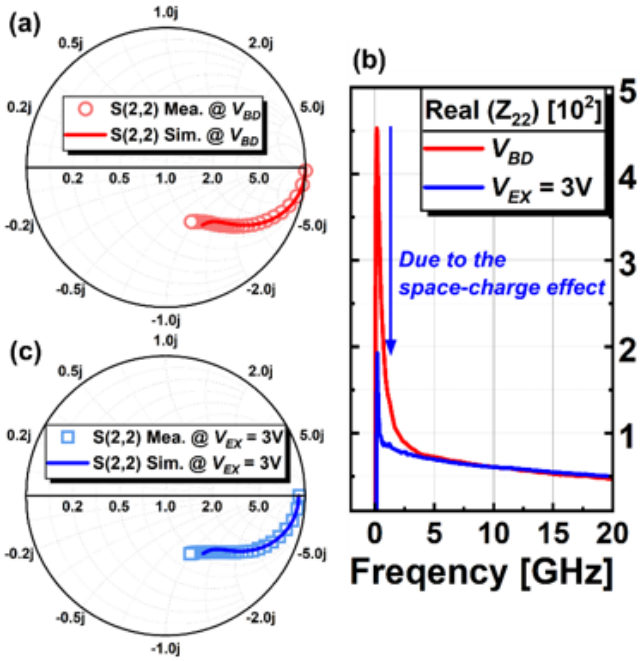


Fig. 2-5. Comparison of the measured and simulated impedance characteristics. (a) Measured and simulated S_{22} at V_{BD}. (b) Comparison of the measured real part of Z_{22} at V_{BD} and V_{EX} 3 V. (c) Measured and simulated Z_{22} at V_{EX} 3 V.

The difference in S_{22} between V_{BD} and V_{EX} 3 V can be attributed to the space-charge resistance, R_{SPAD}, which arises under excess bias conditions. By simply adding R_{SPAD} to the circuit model at V_{BD} without making any other changes (as other parameters show negligible variation with bias), the S_{22} measured at V_{EX} 3 V aligns closely with the simulated results. This validates the reliability of R_{SPAD}, which has been introduced into the SPAD model for the first time.

In Fig. 2-5 (b), the decrease in the real part of Z_{22} highlights the influence of space-charge resistance. The overall resistance decreases as R_{SPAD}, which has a smaller value, is added in parallel to the large value of R_L. The Z_{22} calculations for V_{BD} and V_{EX} 3 V follow the pi-network assumption from Fig. 2-3. First, Y_{22} is computed as the sum of Y2 and Y3. Since Y2 remains unchanged between V_{BD} and V_{EX}, it is excluded from the calculation, and the inverse is taken to derive the Z_{22}.

At V_{BD}, the real part of Z_{22} is calculated as follows:

$$Y_{22} \approx \frac{1}{R_S} \parallel \left(j\omega C_j + \frac{1}{R_L}\right) = \frac{1 + j\omega C_j R_L}{R_S + R_S R_L + j\omega C_j R_S R_L} \tag{5}$$

$$real(Z_{22}) = real\left(\frac{1}{Y_{22}}\right) \approx R_S + R_S R_L \tag{6}$$

At V_{EX}, the real part of Z_{22} is calculated as follows:

$$Y_{22} \approx \frac{1}{R_S} \parallel \left(j\omega C_j + \frac{1}{R_L} + \frac{1}{R_{SPAD}}\right) = \frac{1 + j\omega C_j R_L}{R_S + \frac{R_S R_L R_{SPAD}}{R_L + R_{SPAD}} + \frac{j\omega C_j R_S R_L R_{SPAD}}{R_L + R_{SPAD}}} \quad (7)$$

$$real(Z_{22}) = real\left(\frac{1}{Y_{22}}\right) \approx R_S + \frac{R_S R_L R_{SPAD}}{R_L + R_{SPAD}} \quad (8)$$

For comparison of the real part of Z_{22},

$$\therefore (R_S + R_S R_L) > \left(R_S + \frac{R_S R_L R_{SPAD}}{R_L + R_{SPAD}}\right) \ (\because R_L \gg R_S > R_{SPAD}) \quad (9)$$

As a result, the calculation confirms that the small value of R_{SPAD} leads to a smaller real part of Z_{22} at V_{EX} compared to V_{BD}.

Although the series resistance R_S, which causes a voltage drop, also influences the current gain, the space-charge resistance R_{SPAD} serves as the pathway for the avalanche current [14] and exhibits a strong correlation with it. Since this SPAD has a low R_{SPAD} value of 130 Ω, it is associated with a relatively high saturation current of 1.3 mA at V_{EX} 3 V, as shown in Fig. 2-6. This current gain could impact the SPAD's efficiency, making it essential to account for its R_{SPAD} value in the design process.

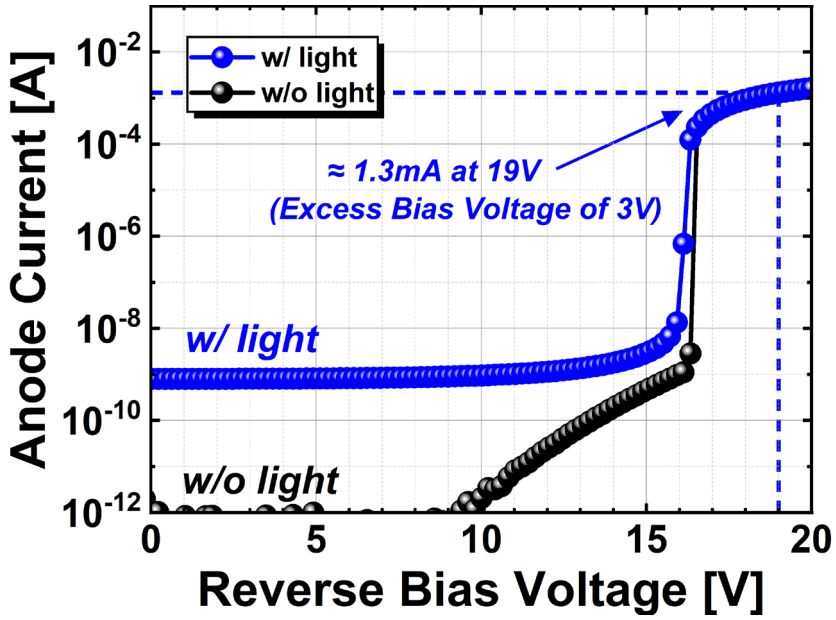


Fig. 2-6. Avalanche saturation current of the SPAD from the I-V characteristics measured under light and dark conditions.

3. Guard-ring optimization of the SPAD

3.1. Device structures

Thanks to the equivalent circuit model of the SPAD proposed in Chapter 2, the device parameters for a PN-type HVPW GR structure SPAD have been determined. As shown in Table 1, the series resistance R_S is relatively high due to the deep formation of the HVPW GR layer, which increases the current path length. This chapter introduces a modeling-based optimization approach by proposing a GR-optimized SPAD. To shorten the current path and the internal series resistance, the GR layer is optimized to be formed at a shallower depth. This optimization is also aimed at expanding the avalanche multiplication region to improve PDP while still preventing PEB.

Avalanche multiplication due to impact ionization occurs only in regions where the electric field exceeds the critical field, typically around 3E + 5 V/cm or higher. This region is referred to as the avalanche multiplication region. The avalanche multiplication region extends into the GR by using a non-physical GR, specifically a p-type epitaxial (P-EPI) layer, in the GR-optimized SPAD. This adjustment results in approximately a 20 % enlargement of the cross-sectional area of the avalanche multiplication region, promising a higher PDP. The device structures of the conventional HVPW GR SPAD and the optimized P-EPI GR SPAD are illustrated in Fig. 3-1. Except for the GR layer, the remaining

structures are identical, featuring an active area diameter of 13.5 μm, a GR size of 1.8 μm, and the use of a DNW layer for the P + / NW junction.

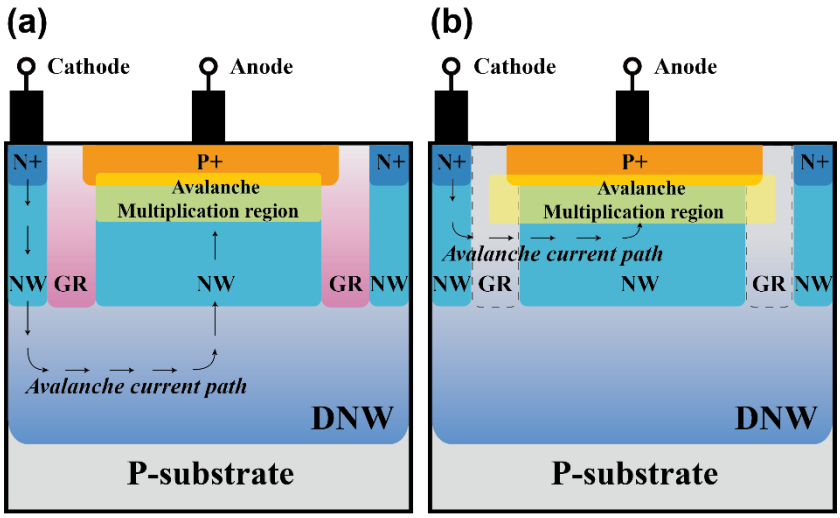


Fig. 3-1. Comparison of the device structures. (a) HVPW GR SPAD. (b) Optimized P-EPI GR SPAD.

3.2. Modeling results

In this section, the optimized P-EPI GR SPAD underwent the same modeling process outlined in Chapter 2. The comparison between the simulated impedance characteristics of the equivalent circuit model and the measured data is shown in Fig. 3-2, demonstrating

good agreement, which indicates that the extracted values are accurate. Table 2 compares the extracted device parameters at V_{EX} 3 V between the HVPW GR SPAD and the optimized P-EPI GR SPAD. Compared to the HVPW GR structure, the shallower P-EPI GR formation shortens the current path from the cathode to the anode, reducing the internal series resistance R_S, which is expected to increase the current gain. Furthermore, the 1.2-fold increase in the C_J value indirectly confirms the expansion of the avalanche multiplication region into the GR area, approximately 1.2 times larger. The use of a non-physical GR (P-EPI GR) enables this extension of the avalanche region. Additionally, the wider electric field distribution is evidenced by the 1.2-fold decrease in the space-charge resistance R_{SPAD}. As a result, the modeling parameter analysis confirms the success of the optimization.

Table. 2. Comparison of the extracted device parameters of the HVPW GR SPAD and the optimized P-EPI GR SPAD at V_{EX} 3 V.

GR Layer	R_{SPAD} [Ω]	R_S [Ω]	C_J [fF]	C_{SUB} [fF]
HVPW	130	1.9k	28	6
P-EPI	108	350	33.6	6

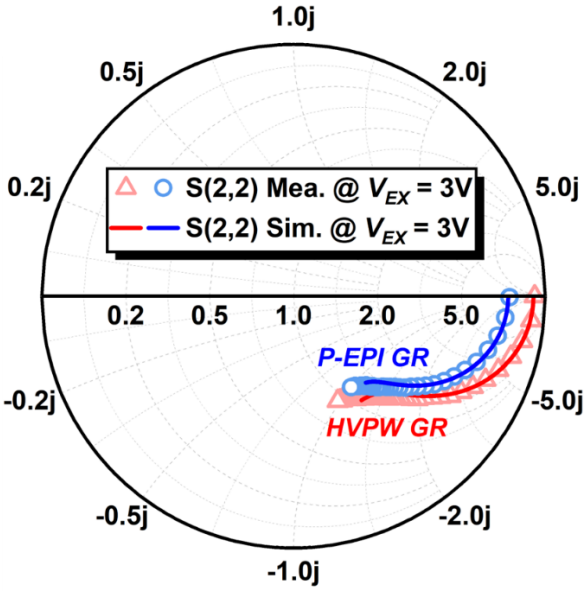


Fig. 3-2. Comparison of the simulated and measured impedance characteristics for the HVPW GR SPAD and the optimized P-EPI GR SPAD.

3.3. TCAD simulation

Through TCAD simulation, we confirmed that the expected reduction in series resistance and the enlargement of the avalanche multiplication region, both achieved through GR optimization, were successfully realized. Fig. 3-3 illustrates the electron current density at V_{EX} 3 V, with arrows indicating carrier movement. Notably, the current path is visibly shortened with the optimized P-EPI GR, further validating the effectiveness of the modeling-based optimization.

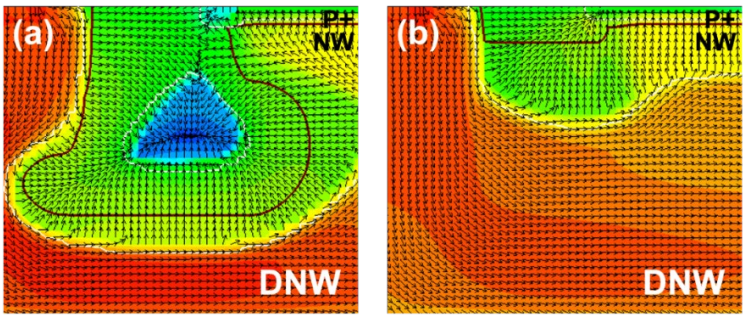


Fig. 3-3. TCAD simulation results of the current density at V_{EX} 3 V. (a) HVPW GR SPAD. (b) Optimized P-EPI GR SPAD.

Fig. 3-4 presents the TCAD simulation results at V_{EX} 3 V, showing the electric field for the HVPW GR SPAD and the optimized P-EPI GR SPAD. As shown in Fig. 3-4 (b) and (d), using the optimized P-EPI GR enlarges the avalanche multiplication.

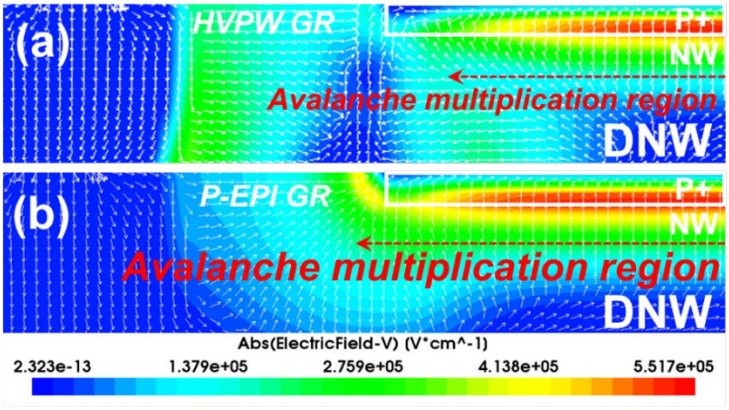


Fig. 3-4. TCAD simulation results at V_{EX} 3 V. (a) Electric field distribution of the HVPW GR SPAD. (b) Electric field distribution of the optimized P-EPI GR SPAD.

Fig. 3-5 presents a 3D distribution comparison of the avalanche multiplication between the HVPW GR SPAD and the optimized P-EPI GR SPAD, simulated at V_{EX} 3 V. At a depth of 0.2 µm, the avalanche multiplication region was observed to have expanded by approximately 1.2 times.

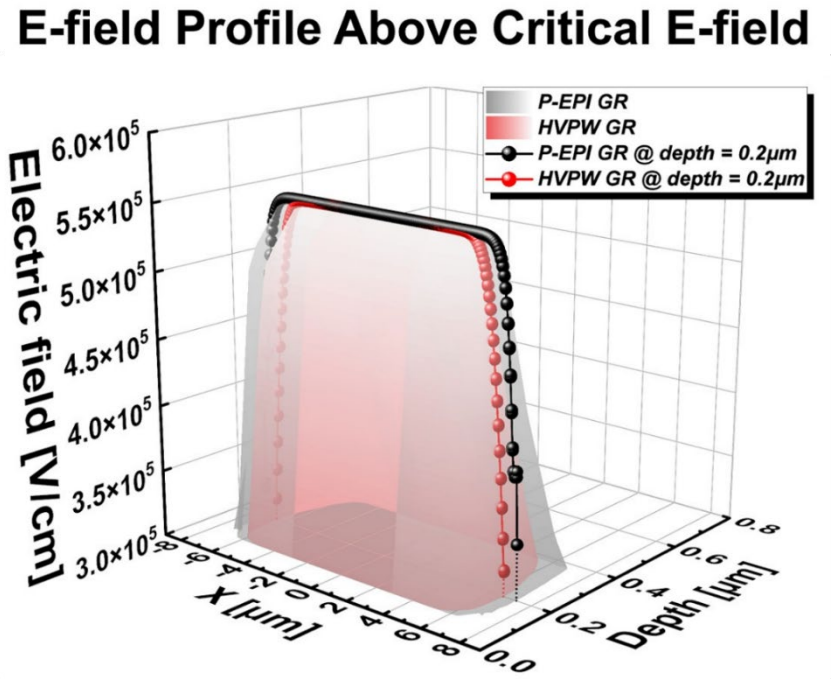


Fig. 3-5. Comparison of the 3D electric field profiles above the critical field (3E + 5 V/cm) between the HVPW GR SPAD and the optimized P-EPI GR SPAD at V_{EX} 3 V.

3.4. Experimental results

We aimed to characterize the optimized P-EPI SPAD through experimental results and evaluate its performance improvements over the conventional HVPW GR SPAD. Additionally, from a modeling perspective, we sought to verify these improvements. The experiments involved measurements of the current-voltage (I-V) characteristics, light emission test (LET), dark count rate (DCR), afterpulsing, and the variation of the breakdown voltage (V_{BD}) and DCR with temperature to assess thermal resilience. Furthermore, PDP and timing jitter were measured for comparative analysis.

3.4.1. I-V characteristics

The I-V characteristics were measured using DC analysis, where the current at each reverse bias point accumulated over a set period under dark and light conditions. Under dark conditions, a lower dark current before avalanche multiplication indicates a higher likelihood of stable operation. V_{BD} can be estimated by identifying the voltage at which avalanche multiplication occurs, and the device's operational stability can also be evaluated through the I-V characteristic measurement. Fig. 3-6 presents the measured I-V characteristics of the HVPW GR SPAD and the optimized P-EPI GR SPAD. As shown, the dark current for both devices is relatively low, in the picoampere range, and the V_{BD} is

nearly identical. However, the leakage current appears in the HVPW GR SPAD due to defects that can arise during the layer implantation process of the HVPW GR layer. The higher saturation current in the optimized P-EPI GR SPAD validates the modeling analysis, which suggests that the increased current gain is due to the reduced resistance (R_S and R_{SPAD}) resulting from the shortened current path. The higher current gain provides the advantage of achieving quenching with lower resistance.

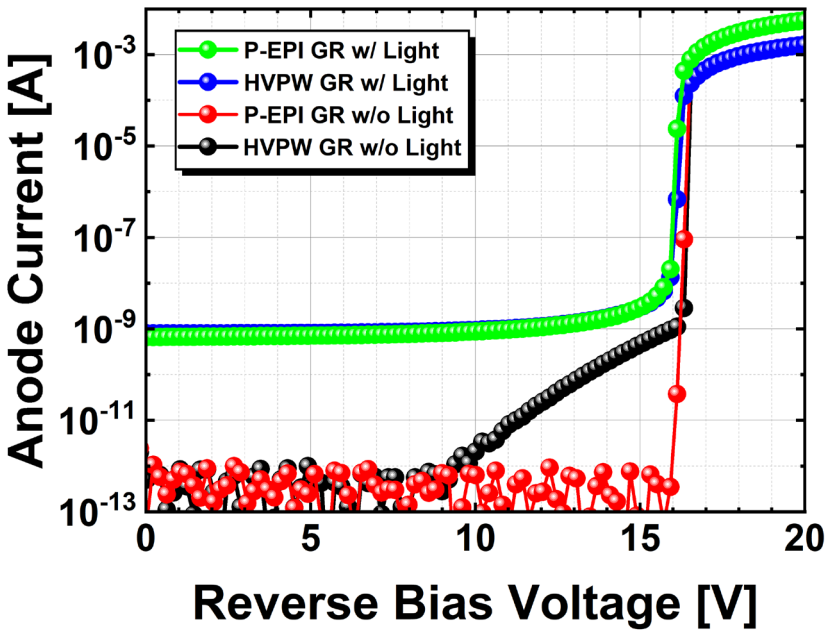


Fig. 3-6. I-V characteristics of the HVPW GR SPAD and the optimized P-EPI GR SPAD under dark and light conditions.

3.4.2. LET

The LET enables observation of the size of the SPAD's light-emitting region and facilitates visual comparison of the avalanche multiplication regions. As shown in Fig. 3-7, LET measurements were taken at room temperature for V_{EX} 1 V and V_{EX} 3 V. Both devices effectively prevent PEB and exhibit brighter, more uniform light as V_{EX} increases. When comparing the cross-sectional area, the optimized P-EPI GR SPAD shows approximately a 20% enlargement of the light-emitting region compared to the HVPW GR SPAD. This result aligns well with modeling results, indicating that the P-EPI GR SPAD has a 1.2 times larger C_J value. When GR optimization is applied to devices with the same junction, it is expected that those with a higher C_J value will have a wider multiplication region.

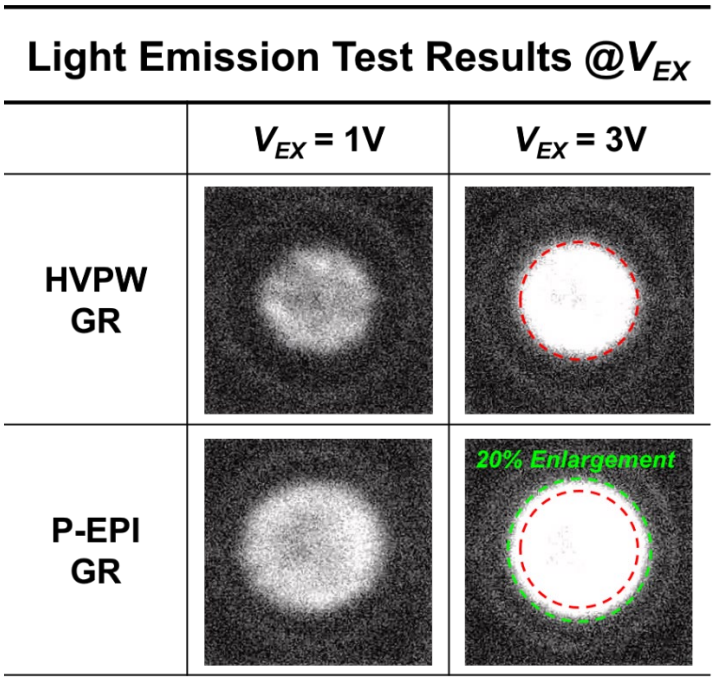


Fig. 3-7. Comparison of the LET results for the HVPW GR SPAD and the optimized P-EPI GR SPAD at room temperature *at* V_{EX} 1 V and 3 V.

3.4.3. DCR

The DCR measures the number of output signals generated under conditions without external signals. The components of the DCR can be classified into primary and secondary contributions. The primary DCR includes thermally generated noise, tunneling noise, trap-assisted thermal generation, and trap-assisted tunneling (TAT). Secondary DCR originates from afterpulsing, a phenomenon where charge carriers generated by photons are trapped

in defect states within the device and subsequently released. This release generates output signals that are independent of any external optical input. A high DCR can obscure genuine signals by introducing excessive noise into the output, which also results in higher power consumption.

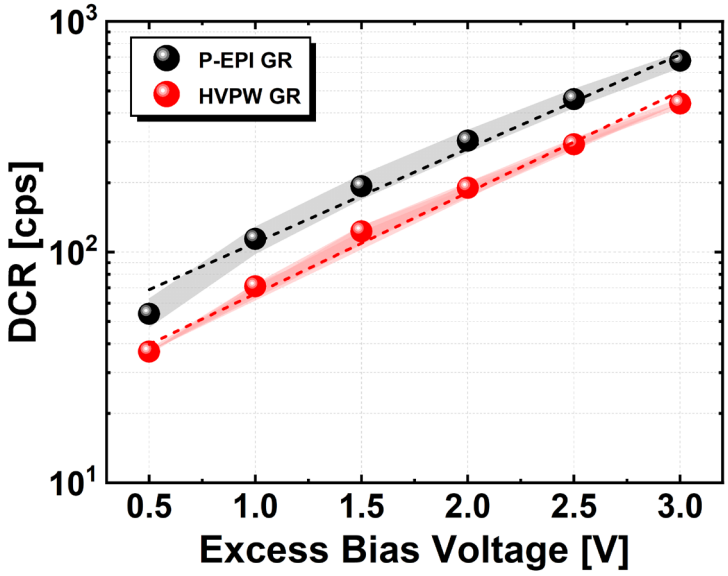


Fig. 3-8. DCR comparison between the HVPW GR SPAD and the optimized P-EPI GR SPAD with V_{EX} ranging from 0.5 to 3 V at room temperature.

Fig. 3-8 presents the DCR measurement results for the HVPW GR SPAD and the optimized P-EPI GR SPAD at room temperature. Measurements were conducted from V_{EX} for 0.5 V to 3 V in 0.5 V increments. Five dies per device were measured to account for die

variations, and the average value was plotted as markers. The shaded region in the figure indicates the degree of variation among the dies. At the same time, the dotted line represents the overall trend of the DCR as the excess bias voltage increases. Upon comparing the trend lines of the two devices, similar trends are observed in the increase of DCR with excess bias voltage, as the only difference between them is the GR layer, with their junction structures remaining the same. Although the optimized P-EPI GR shows a slightly higher DCR due to its larger active area, where DCR occurs, it still achieves a very low DCR level of 3.9 cps/μm².

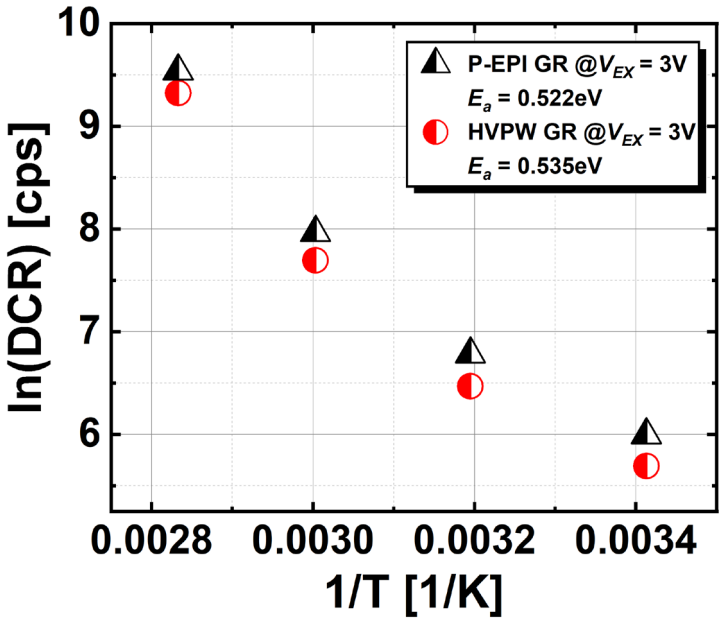


Fig. 3-9. Arrhenius plot for the HVPW GR SPAD and the optimized P-EPI GR SPAD at V_{EX} of 3 V.

Fig. 3-9 and Fig. 3-10 illustrate the characteristics of the devices under varying temperatures. Fig. 3-9 presents the DCR results plotted as an Arrhenius plot, measured from 20°C to 80°C at 20°C intervals for V_{EX} 3 V. The results indicate that the optimized P-EPI GR SPAD and HVPW GR SPAD exhibit nearly identical activation energies (E_a) of 0.535 eV and 0.522 eV, respectively. This confirms that TAT is the dominant component contributing to DCR in both devices [19]. This result indicates that the devices exhibit similar noise characteristics due to their identical junction structure.

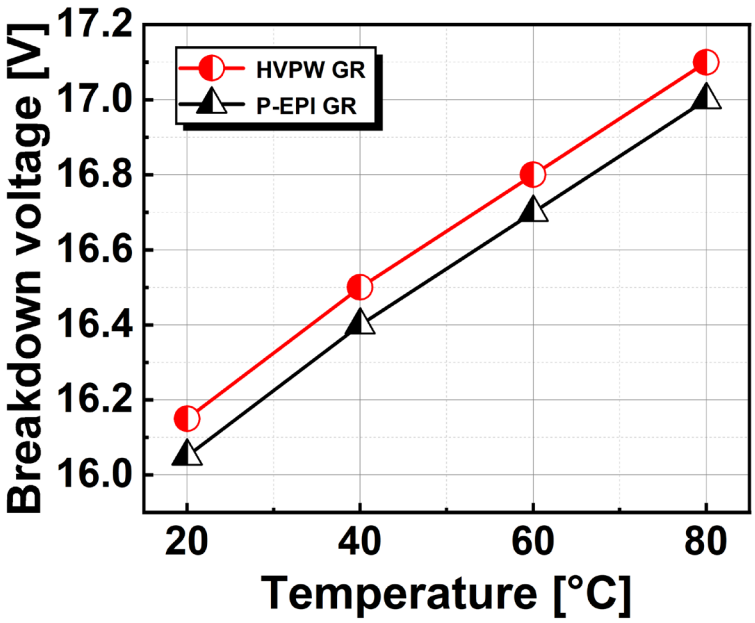


Fig. 3-10. V_{BD} variation comparison between the HVPW GR SPAD and the optimized P-EPI GR SPAD with temperature variation from 20°C to 80°C.

Fig. 3-10 presents the measurements of V_{BD} changes with temperature. The HVPW GR SPAD exhibited a slightly higher V_{BD} of approximately 0.1 V compared to the P-EPI GR SPAD; however, this difference is negligible and can be attributed to die variation. Both devices displayed similar trends, with a temperature coefficient of 15 mV/K, indicating stable performance even under high-temperature operation.

Secondary DCR, or afterpulsing, occurs consecutively following avalanche events. The interval time between avalanche events was measured to evaluate the afterpulsing probability. An exponential fitting curve was drawn based on pulse counts at relatively long interval times, with any deviations from this curve in the short interval time region considered indicative of afterpulsing. Fig. 3-11 shows the results of the inter-avalanche event measurements at V_{EX} 3 V and room temperature, demonstrating that both devices exhibit no evidence of afterpulsing. This is attributed to high-quality processing, as there are no significant defects present at the operating voltage (V_{EX} 3 V) that would trap electrons.

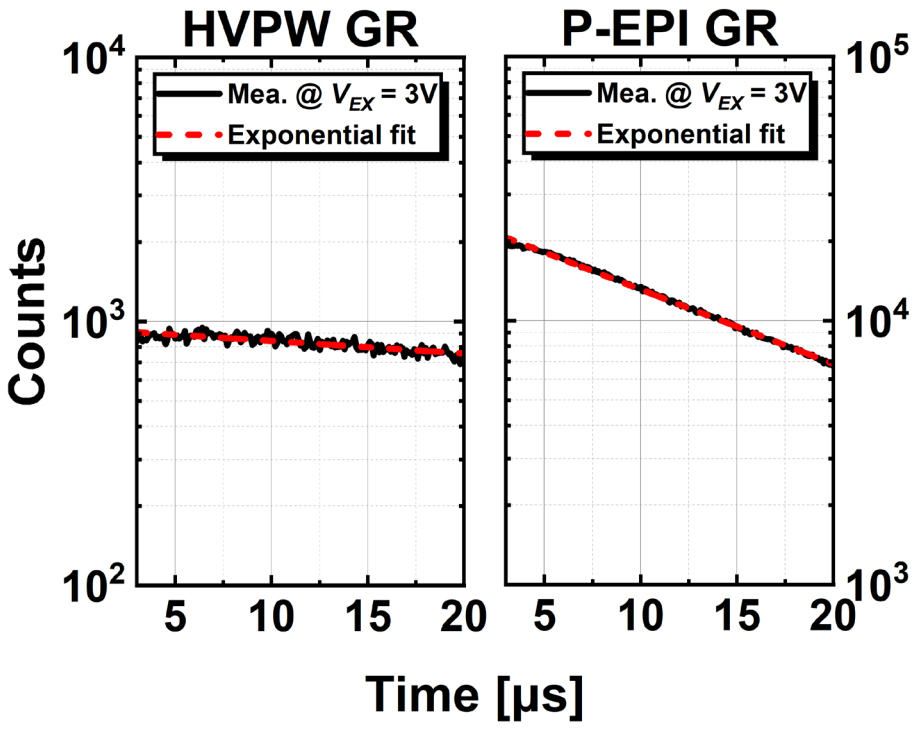


Fig. 3-11. Measured inter-avalanche events for the HVPW GR SPAD and the optimized P-EPI GR SPAD at V_{EX} 3 V and room temperature.

3.4.4. PDP

PDP is one of the most crucial performance indicators for SPADs, as it directly influences their effectiveness in various applications as detectors. The PDP is evaluated using the following equation, which measures how many output pulses are generated in response to incident photons, excluding the DCR. The incident photons were quantified

from the optical power, and the active area size of the SPAD was considered in comparison to the reference photodetector's active area.

$$PDP\ [\%] = \frac{counts - DCR}{\left\{Popt/\frac{hc}{\lambda}\right\} \times \frac{SPAD\ active\ area}{reference\ PD\ area}} \quad (10)$$

Fig. 3-12 and Fig. 3-13 show the measured PDP results for the HVPW GR SPAD and optimized P-EPI GR SPAD, respectively, taken at room temperature across wavelengths ranging from 400 nm to 950 nm, with measurements recorded at 25 nm intervals. Both devices exhibit the highest PDP at V_{EX} 3 V, with peaks near the 425 nm wavelength, closer to the blue spectrum. This peak behavior is attributed to the shallow junction formation in both devices, which were designed with a P + / NW junction, resulting in a strong electric field at shallow depths. The HVPW GR SPAD demonstrates a peak PDP of 34.13 % at 425 nm and V_{EX} 3 V, while the optimized P-EPI GR SPAD achieves a peak of 50.63 % at the same wavelength and bias voltage, representing a 48 % improvement in PDP due to GR optimization. This enhancement is attributed to the expanded avalanche multiplication region, which facilitates the detection of more photons. After normalizing for the enlarged active area, the device shows a value of 35.16 % at 425 nm and V_{EX} 3 V, similar to that of the HVPW GR SPAD. The slightly higher value is due to the participation of additional carriers collected in the expanded carrier collection region. The 20 % increase in the

modeling parameter C_J explains the PDP improvement resulting from the enlarged active area.

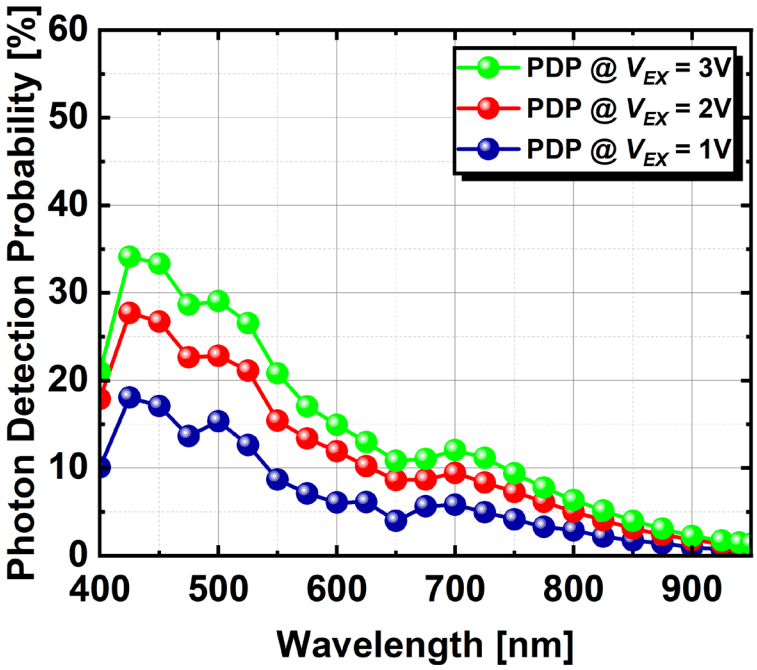


Fig. 3-12. PDP results of the HVPW GR SPAD.

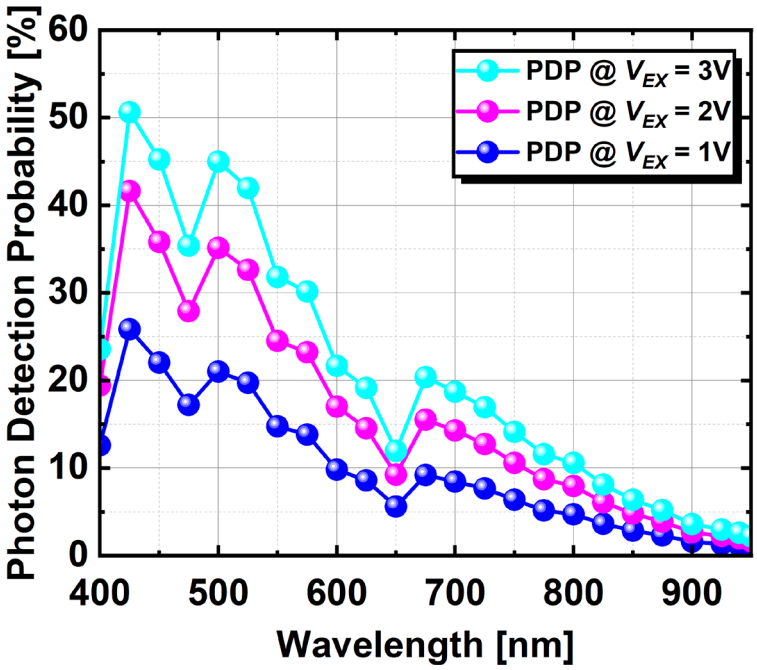


Fig. 3-13. PDP results of the optimized P-EPI GR SPAD.

3.4.5. Timing jitter

Timing jitter represents the response speed of a SPAD and is a critical characteristic in applications such as integrated quantum photonics and LiDAR, where fast response is essential. In this chapter, the optimized P-PEI GR SPAD addresses the limitations of the conventional HVPW GR SPAD by reducing the high internal series resistance caused by the long current path. This optimization results in a reduced quenching time constant (τ_q)

and an improved slew rate. The quenching time constant (τ_q) and the recharge time constant (τ_r) can be expressed as follows [20]:

$$\tau_q = (C_D + C_L) \times \frac{R_L R_D}{R_L + R_D} \approx (C_D + C_L) \times R_D \quad (11)$$

$$\tau_r = (C_D + C_L) \times R_L \quad (12)$$

C_D and R_D represent the diode's capacitance and resistance, C_L is the load capacitance, and R_Q is the quenching resistor. A larger quenching resistor increases the recharge time, leading to a longer dead time. In this optimization, although C_D decreased, its contribution is combined with C_L, making R_D the more dominant factor. As a result, R_D, along with the increased internal resistance (R_S and R_{SPAD}), had a greater influence on extending the quenching time constant and slowing the slew rate.

As reported in [21], the root-mean-square (RMS) timing jitter is inversely proportional to the slew rate. The RMS timing jitter, assuming a Gaussian distribution of measurement results, can be expressed as:

$$RMS\ Timing\ Jitter = \frac{FWHM}{2\sqrt{2ln2}} \quad (13)$$

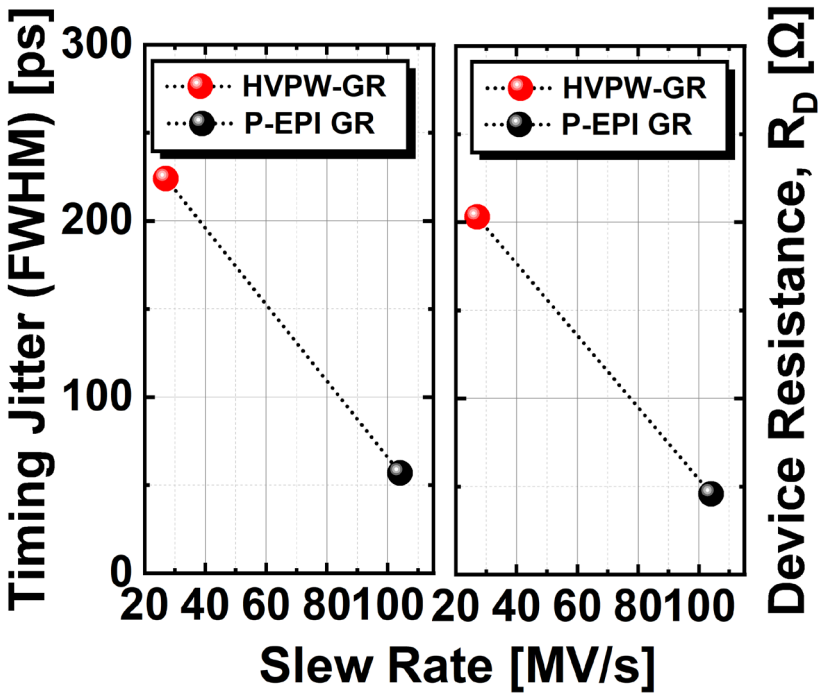


Fig. 3-14. Measured slew rate vs. timing jitter and device resistance of the HVPW GR SPAD and the optimized P-EPI GR SPAD at V_{EX} 3 V.

Thus, the reduced series resistance achieved through optimization leads to an increased slew rate, subsequently improving the timing jitter. Fig. 3-14 illustrates the relationship between the measured slew rate, timing jitter, and device resistance (R_D) at V_{EX} 3 V for the HVPW GR SPAD and the optimized P-EPI GR SPAD. As device resistance decreases, timing jitter also decreases, exhibiting an inverse relationship similar to that of slew rate. Timing jitter measurements were conducted at 510 nm, near the peak PDP of each SPAD. The optimization resulted in a significant improvement in slew rate, increasing from 27

MV/s to 105 MV/s (a 3.85 x improvement), and a corresponding reduction in FWHM timing jitter from 224 ps to 57 ps (approximately a 3.92 x improvement).

Operating at room temperature [19], [22], SPADs have the potential to replace SNSPDs [23], which require cryogenic cooling [24], [25], [26], [27], [28], [29], [30], [31], as receivers in integrated quantum photonics. However, performance gaps still exist compared to SNSPDs, necessitating further optimization. The GR-optimized SPAD presented in this chapter, with its improved detection efficiency and fast timing response, demonstrates strong potential for applications in integrated quantum photonics.

4. Size optimization of the SPAD

Recent research has focused on SPAD miniaturization [32], [33], which offers advantages such as improving pixel resolution by increasing the number of SPADs within a limited area [34], as well as enabling their use in portable devices like smartphones and spatial computing systems [35]. Miniaturized SPADs not only improve spatial resolution but also reduce power consumption due to lower RC values, which is anticipated to enhance timing jitter performance. However, contrary to expectations, our modeling of the optimized P-EPI GR SPAD (discussed in Chapter 3) reveals that timing jitter does not improve with reduced size. Instead, miniaturization increases the SPAD's space charge resistance, leading to a higher slew rate and adversely impacting timing jitter. This chapter

explores the trade-offs of SPAD miniaturization using modeling-based device analysis, emphasizing the need for size optimization tailored to specific target applications.

4.1. Modeling results

The P-EPI GR SPADs with active area diameters of 4.5 μm, 9 μm, and 13.5 μm were modeled using the process described in Chapter 2, and the results are summarized in Table 3. As the size decreased, the R_{SPAD} increased according to equation (1), while the C_J decreased. Notably, R_S shows slight variation between the 9 μm and 13.5 μm SPADs but increases significantly for the 4.5 μm device. Based on these modeling results, we can infer that as SPADs are miniaturized, the capacitance decreases while the R_{SPAD} increases, resulting in a lower current saturation gain. Although this lower current gain reduces power consumption, this necessitates using a larger quenching resistor to quench the device effectively.

Table. 3. Comparison of the extracted device parameters of the P-EPI GR SPAD in size variation.

Diameter of AA [μm]	R_{SPAD} [Ω]	R_S [Ω]	C_J [fF]
13.5	108	350	33.6
9	240	400	15.5
4.5	986	1864	3.8

4.2. TCAD simulation

The variation in R_S was verified through electron current density simulations. As shown in Fig. 4-1, despite the size reduction, there is no significant difference in the current density profile between SPADs with active area diameters of 13.5 µm and 9 µm. However, for the SPAD with a 4.5 µm active area, the current path becomes narrower, and the length is insufficient to maintain a similar current density. This causes the vertical component of the current path to become more dominant, leading to an increase in the series resistance due to the reduced active area. Consequently, the 4.5 µm active area SPAD exhibits a lower current density profile.

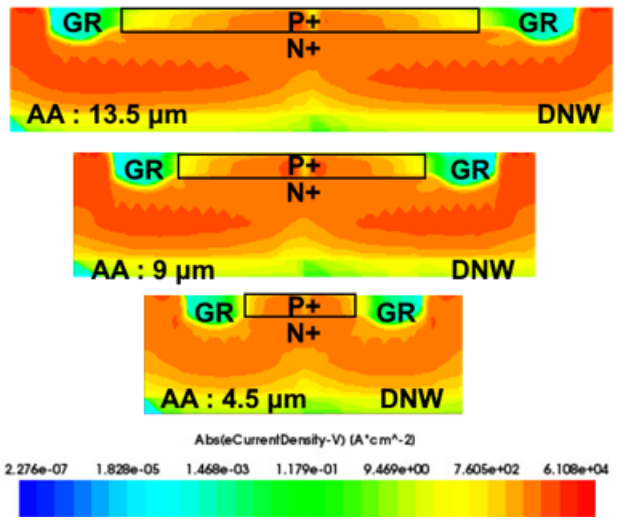


Fig. 4-1. TCAD current density simulation results of the SPADs in size variation.

4.3. Experimental results

4.3.1. I-V characteristics

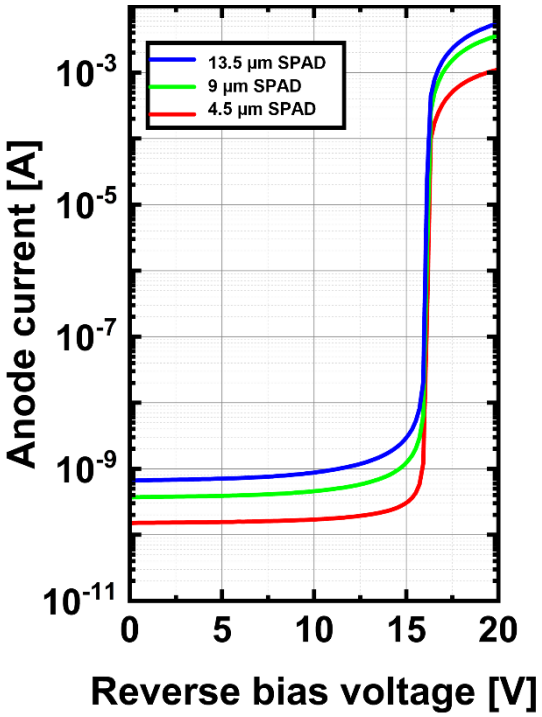


Fig. 4-2. I-V characteristics of the SPADs in size variation.

According to Table. 3, as the P-EPI GR SPAD is miniaturized, the increase in R_{SPAD} is expected to decrease the current saturation gain. The measured I-V characteristics shown in Fig. 4-2 validate this trend. For the P-EPI GR SPAD with a diameter of 4.5 μm, the series resistance R_S is also significantly high, leading to a lower gain of about 0.95 mA at V_{EX} 3 V compared to the other two devices.

4.3.2. LET

The LET was measured for the three SPAD devices with different active area sizes, each having a consistent GR size of 1.8 μm. As shown in Fig. 4-3, the LET results, conducted at room temperature with V_{EX} 3 V, indicate that three devices exhibit uniform light emission areas, with clear differences in light emission areas corresponding to the variations in active area size.

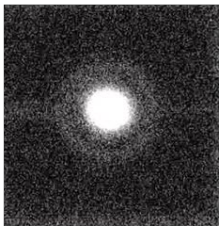
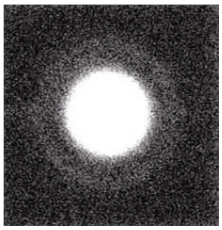
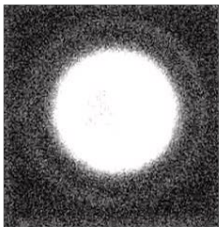
Diameter of AA	4.5 μm	9 μm	13.5 μm
P-EPI GR			

Fig. 4-3. LET results of the SPADs in size variation.

4.3.3. DCR

In Fig. 4-4, the DCR results measured at room temperature from 1 V to 3 V reveal a consistent trend: as the excess voltage increases, the DCR rises correspondingly., Notably,

smaller SPAD sizes exhibit lower DCR, as the DCR is proportional to the active area size. This demonstrates that miniaturizing the SPAD can reduce the DCR, thereby improving the signal-to-noise ratio.

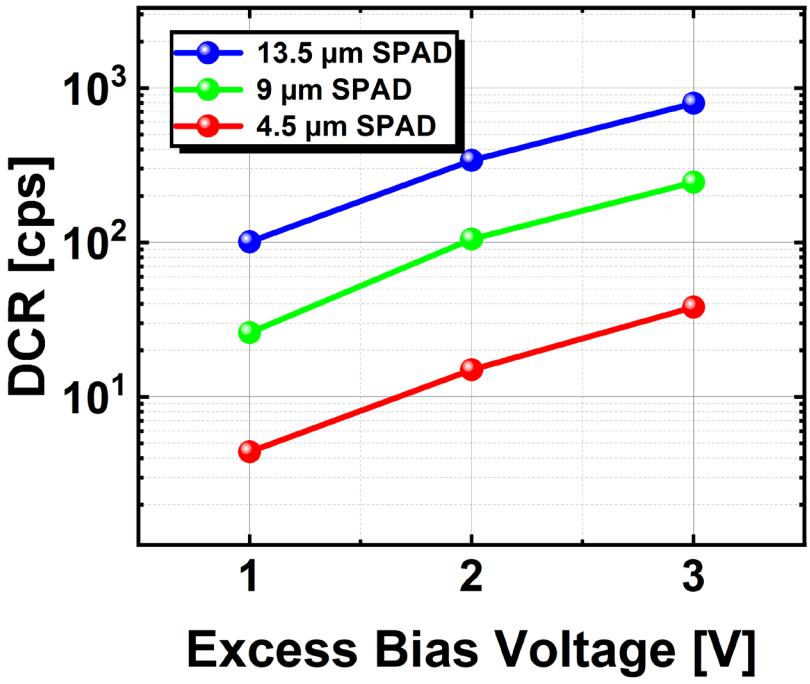


Fig. 4-4. DCR results of the SPADs in size variation.

4.3.4. PDP

In Chapter 2, we observed that changing the GR layer from the HVPW GR to the optimized P-EPI GR led to increased PDP. This was attributed to the enlargement of the

avalanche multiplication region. To investigate how the active area size affects PDP, measurements were taken across a wavelength range of 425 nm to 950 nm at 25 nm intervals and V_{EX} values ranging from 1 V to 3 V. The results are presented in Fig. 4-5.

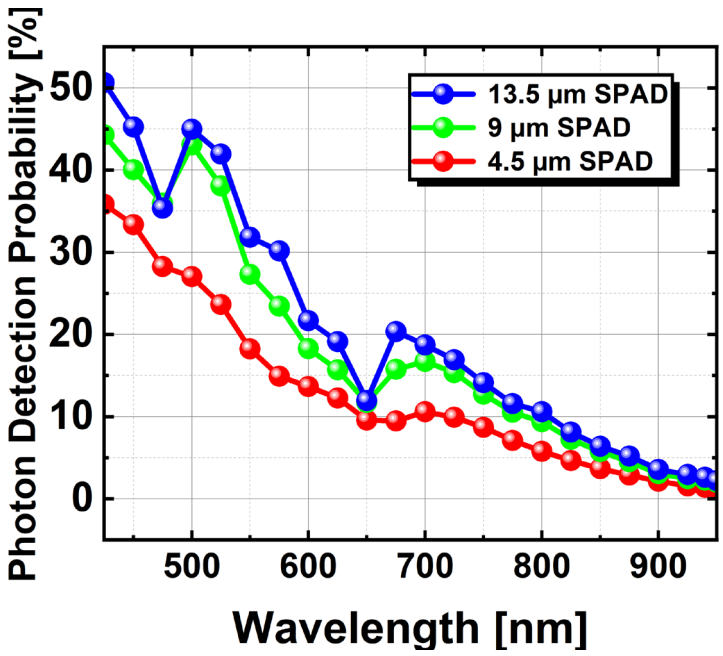


Fig. 4-5. PDP results of the SPADs in size variation measured at V_{EX} 3 V.

According to equation (10), since the active area size is normalized by dividing it by the reference photodetector size, the three SPAD devices are expected to exhibit similar PDP values. However, the PDP results in Figs. 4 and 5 indicate that larger SPAD sizes exhibit higher PDP values. This is likely because, as the active area size increases, the

carrier collection region at the SPAD periphery expands, enabling the absorption of more carriers.

4.3.5. Power consumption

Through the I-V characteristic measurements, we observed that smaller SPAD sizes offer advantages in terms of power consumption, as they exhibit lower current gain. To quantify the differences in power consumption across various sizes, we measured the output current pulse of each SPAD using a current probe. We calculated the area under the pulse to determine the current per pulse. The current investigation operates on the principle of electromagnetic induction, allowing for indirect current measurement without direct electrical contact. The measurement results are shown in Fig. 4-6. Fig. 4-7 compares the measured output current pulses for three devices with active area diameters of 4.5 μm, 9 μm, and 13.5 μm, which exhibit charges per pulse of 225 pC, 258 pC, and 272 pC, respectively. These values include parasitic components from the current probe, requiring additional corrections to determine the precise charge per pulse. The difference between the devices is approximately 25 pC, showing about a 14 % variation corresponding to the size differences. These results, as presented in Fig. 4-7, confirm that SPAD miniaturization provides a significant advantage in terms of power consumption.

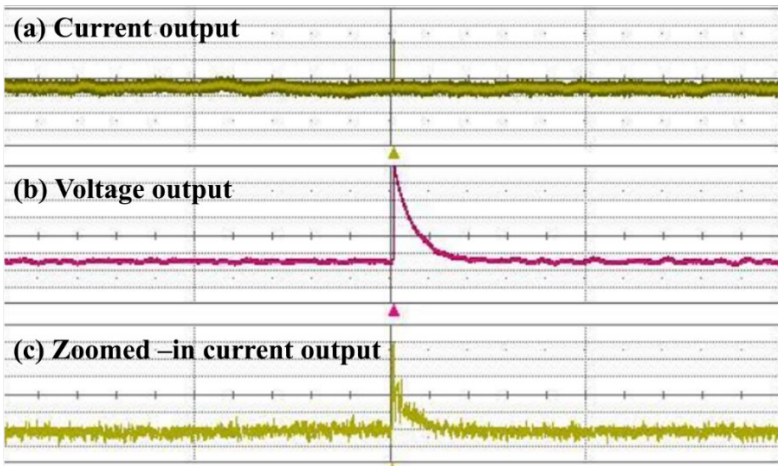


Fig. 4-6. Measured output of the P-EPI GR SPAD with a 9 μm diameter active area.

(a) Current output pulse. (b) Voltage output pulse. (c) Zoomed-in view of (a).

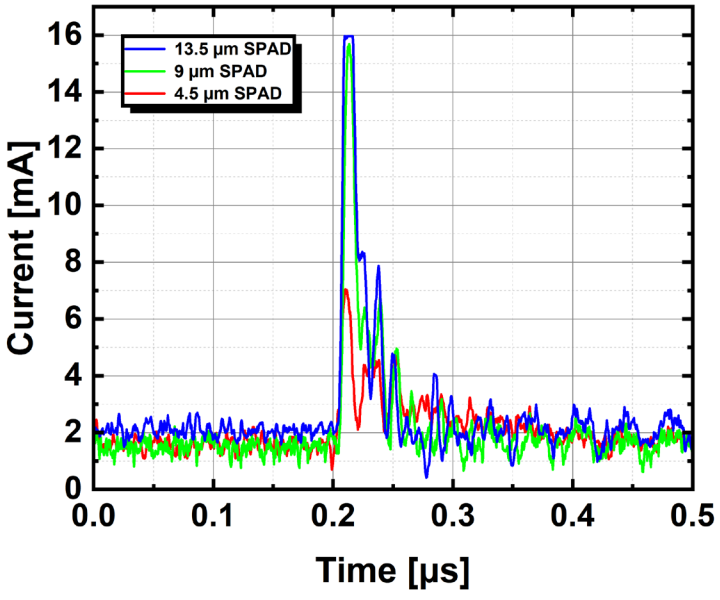


Fig. 4-7. Measured current pulses from the SPADs with varying sizes at V_{EX} 3 V.

4.3.6. Slew rate

A known trade-off of SPAD miniaturization is the fill factor. This thesis identifies timing jitter as another significant trade-off. As shown in Table. 3, as the SPAD size decreases, the internal resistance increases, which, in turn, slows down the quenching time or slew rate. Since the slew rate is directly related to timing jitter, we can conclude that smaller devices exhibit worse timing jitter performance. The slew rate measurement results, calculated as the mean slew rate between 20% and 80% of each pulse, were recorded as 31 MV/s, 76 MV/s, and 104 MV/s for the SPAD devices with active area diameters of 4.5 μm, 9 μm, and 13.5 μm, respectively. A clear linear relationship between device size and slew rate is observed, indicating that the increase in resistance with reduced size directly contributes to the degradation of the slew rate. Figures 4-8, 4-9, and 4-10 show the timing jitter measurement results at V_{EX} 3 V for SPADs with active area diameters of 4.5 μm, 9 μm, and 13.5 μm, respectively. The timing jitter values, based on the FWHM, were measured as 160.8 ps, 85.3 ps, and 57.4 ps, showing a similar proportionality to the slew rate differences among the devices. These results confirm that smaller device sizes exhibit worse jitter performance. Through experimental and modeling analysis, it was demonstrated that SPAD miniaturization increases R_{SPAD}, slows down the slew rate, and reduces the current saturation gain. While a slower slew rate leads to increased timing jitter and, consequently, reduced accuracy, the lower internal capacitance and decreased current saturation gain provide advantages in terms of power consumption. Although conventional

SPAD miniaturization research generally predicts improved timing jitter due to reduced RC values, this work is the first to demonstrate that an increase in R_{SPAD} negatively impacts timing jitter performance. Thus, miniaturization involves a trade-off between power consumption and timing jitter. Moreover, an inverse correlation between current saturation gain and timing jitter has been identified. Furthermore, our analysis shows that for high-count rate applications where power consumption is critical, the optimal SPAD pixel size is an active area diameter of 4.5 μm with the lowest power consumption. In contrast, for long-range detection applications, including LiDAR, where timing jitter is more critical for accurate range detection, the optimal SPAD pixel size is 13.5 μm with the best timing jitter performance. These results highlight that the optimal size of SPAD pixel should vary based on the application's specific requirements, suggesting that future designs can achieve better performance by tailoring SPAD pixel sizes to the needs of each application.

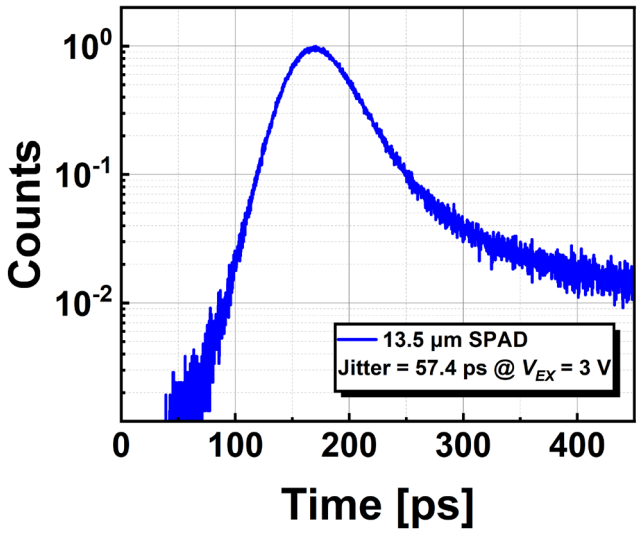


Fig. 4-8. Timing jitter results of the optimized P-EPI GR SPAD with an active area diameter of 13.5 μm at V_{EX} = 3 V.

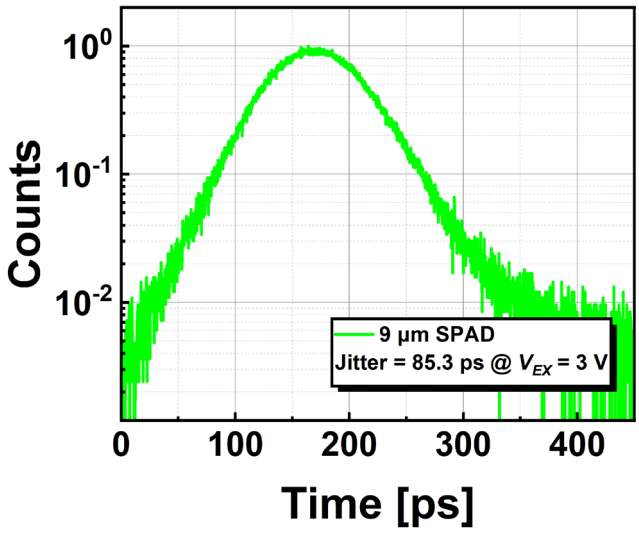


Fig. 4-9. Timing jitter results of the optimized P-EPI GR SPAD with an active area diameter of 9 μm at V_{EX} = 3 V.

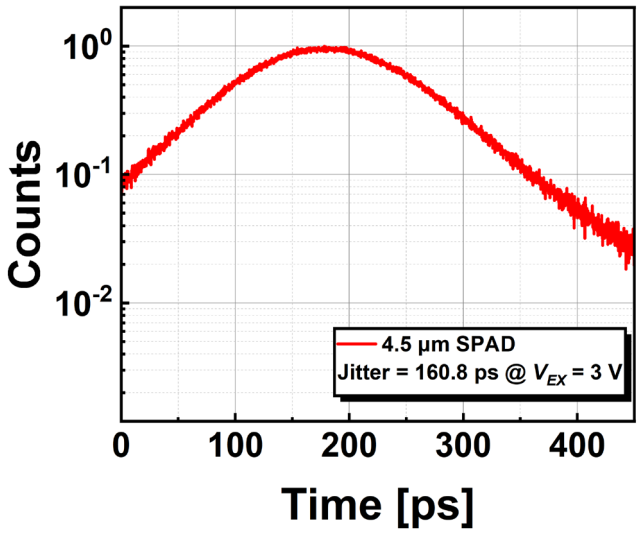


Fig. 4-10. Timing jitter results of the optimized P-EPI GR SPAD with an active area diameter of 4.5 μm at V_{EX} = 3 V.

5. Verilog-A model of SPAD

5.1. Conventional Verilog-A model

In applications utilizing SPADs, such as direct time-of-flight (dToF) sensor systems based on SPAD ICs, designing circuits that include detectors requires a Verilog-A SPAD model to optimize the overall system performance. However, the lack of an equivalent circuit model that accurately reflects the device parameters of SPADs poses a significant challenge. Conventional Verilog-A models merely mimic SPAD operation without

accounting for the precise RC components of the device [36], [37], [38]. This limitation is critical because the RC characteristics of SPADs significantly influence the design and optimization of directly connected circuits, mainly the analog front end (AFE). Therefore, an accurate Verilog-A model incorporating these RC components is essential for proper system optimization. This chapter introduces an advanced Verilog-A model that integrates the equivalent circuit model of the SPAD proposed in the previous chapter, accurately reflecting the device's parameters for the first time. Through this integration, the advanced Verilog-A model enables more precise simulations of both the static and dynamic behavior of SPADs compared to conventional models.

5.2. Advanced Verilog-A model

The initial Verilog-A model simplified the internal resistance of the SPAD into a single series resistance [36]. This version of the Verilog-A model determined the series resistance value based on the slope near V_{BD} in the SPAD's I-V characteristic curve during avalanche multiplication. However, since the slope near V_{BD} continuously changes as V_{EX} increases, this approach had limitations in accurately simulating the SPAD's static behavior. To address this, the model was later modified to subdivide the slope near V_{BD}, allowing the series resistance value to vary dynamically with changes in the voltage applied to the SPAD [37], [38]. While this adjustment reduced the error to some extent, the accuracy remains limited due to a lack of detailed research on SPAD device parameters. Specifically, the

model still conflates the space-charge resistance, which defines the avalanche current path, with the inner series resistance responsible for voltage drops. As a result, further research on SPAD device is required to improve the model's accuracy.

The advanced Verilog-A model proposed in this thesis integrates the equivalent circuit model of the SPAD device's intrinsic properties, as presented in the previous chapter, into the existing Verilog-A framework. This enhancement not only separates the space-charge resistance, which defines the avalanche current path, from the inner series resistance but also utilizes precisely extracted values for each parameter. This modification ensures that the DC (static behavior) operation closely aligns with the measured I-V characteristics. As illustrated in Fig. 5-1, the conventional Verilog-A model derived the series resistance from the slope near V_{BD}. However, as summarized in Table 2, significant discrepancies persist, with errors reaching up to 261 % in the case of the HVPW GR SPAD.

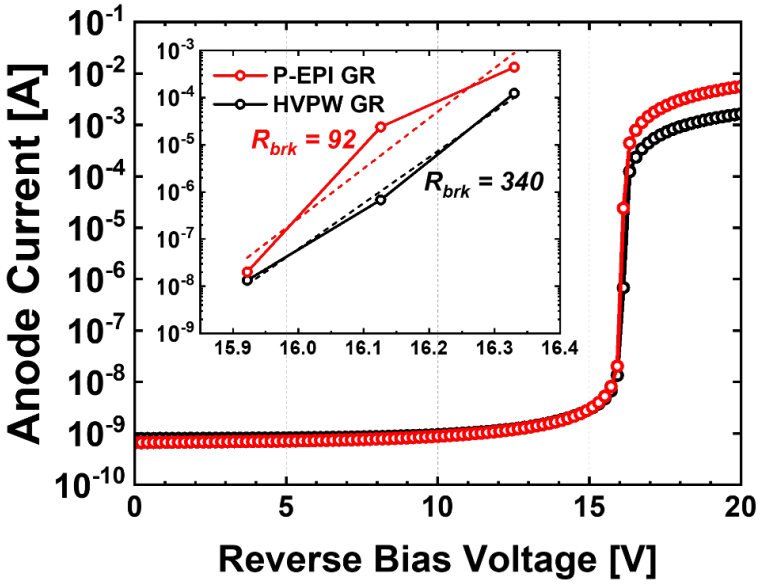


Fig. 5-1. Conventional method for determining the series resistance value of the HVPW GR SPAD and the P-EPI GR SPAD with 13.5 μm diameter active area.

5.2.1. Verilog-A code

The Verilog-A code for the proposed Verilog-A model is presented below. In this model, the avalanche current flows through R_{SPAD}, while the voltage drop occurs across R_S.

Electrical a, k, photon, gnd, N, Z;

Branch (k,gnd) KSUB;

Branch (k,N) RS;

Branch (N,a) CJ;

Branch (N,Z) ISPAD;

Branch (Z,a) RSPAD;

Analog begin

Qks = Cks * V(KSUB);

I(KSUB) <+ ddt (Qks);

Qj = Cj * V(CJ);

I(CJ) <+ ddt(Qj);

V(RSPAD) <+ (ISPAD) * Rspad;

V(RS) <+ RS * I(RS);

// If avalanche multiplication occurs

Ibrk = (Vn/Rspad) * ln(1 + exp((V(k,a)-VB))/Vn));

Ispad <+ Is + aval * Ibrk;

I(ISPAD) <+ Ispad;

5.2.2. Avalanche current model (static model)

In the original Verilog-A model, the avalanche multiplication was implemented using the differentiable pseudo-max function equation. In the advanced Verilog-A model, as shown in Fig. 5-2, by accounting for the voltage drop across R_S and utilizing the accurate value of R_{SPAD}, where the avalanche current flows, the advanced avalanche multiplication equation, referred to as the avalanche current model, is proposed in equations (13) and (14). For the DC analysis, C_J is treated as an open circuit.

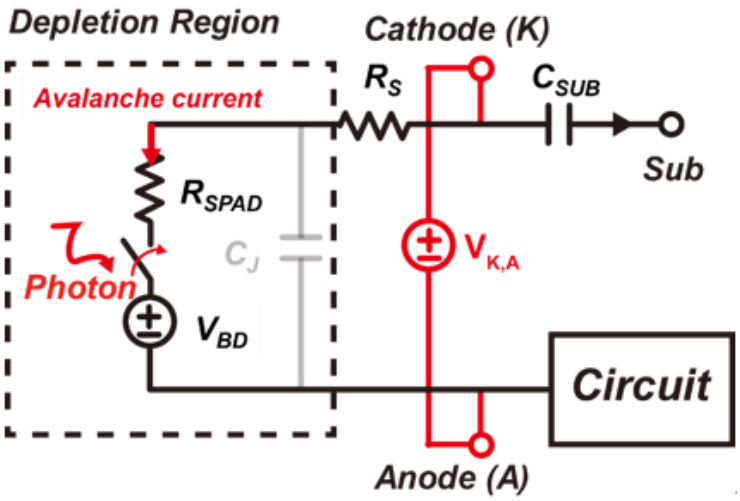


Fig. 5-2. Schematic of the proposed Verilog-A model.

$$V_{R_{SPAD}} = (V_{K,A} - V_{BD}) \times \frac{R_{SPAD}}{R_{SPAD} + R_S} \tag{13}$$

$$I_{R_{SPAD}} = \frac{0.01}{R_{SPAD}} \ln\left(1 + e^{\frac{V_{R_{SPAD}}}{0.01}}\right) \quad (14)$$

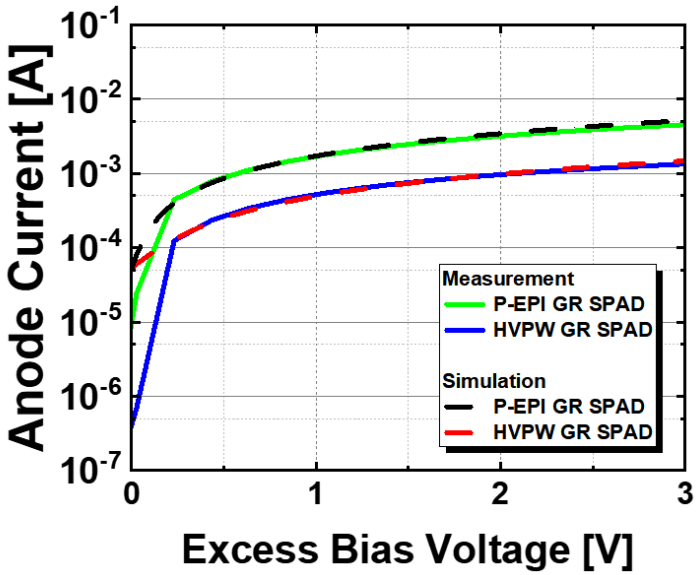


Fig. 5-3. Comparison of the DC avalanche current between the measurement and simulation based on the proposed equation.

In Fig. 5-3, by applying the device parameters of both P-EPI GR SPAD and HVPW GR SPAD to equations (13)-(14), the resulting avalanche current closely aligns with the measured avalanche saturation current obtained from the I-V characteristics. This alignment demonstrates that the proposed Verilog-A model accurately captures the unique avalanche current characteristics of each SPAD, facilitating further system optimization during circuit simulation. In the dynamic behavior of the SPAD, the accuracy of the

charge accumulation and discharge is improved by utilizing the precise values of parasitic capacitance.

5.2.3. DCR model (statistical model)

The inherent noise characteristic of SPADs, known as DCR, has been incorporated into the Verilog-A model. The primary DCR is categorized into two components: one caused by thermal noise and the other by band-to-band tunneling (BTBT). The carrier generation rate equation for the thermal noise component includes TAT, with lifetimes extracted from TCAD simulations to account for TAT effects. Temperature-dependent changes in carrier lifetime and avalanche probability were also derived using TCAD simulations. The distribution of avalanche probability is shown in Fig. 5-4, demonstrating that avalanche events occur only in regions exceeding the critical electric field. The equations used to model the DCR in the proposed Verilog-A model are as follows:

$$CGR_{Thermal} = \frac{n_i AW}{\tau_{eff}}\left(1 - e^{\frac{-qV}{2kT}}\right) \tag{15}$$

$$\tau_{eff} = \frac{\tau_{n_0}(p_0 + p_1 + \Delta n) + \tau_{p_0}(n_0 + n_1 + \Delta n)}{n_0 + p_0 + \Delta n} \tag{16}$$

$$CGR_{BTBT} = BF^{2.5} D\, e^{(\frac{-F_0}{F})} \tag{17}$$

Regarding afterpulsing, it was negligible as it was not observed in any of the SPAD devices discussed in this thesis, owing to advancements in fabrication processes. This DCR model focuses on the P-EPI GR SPAD, which features a previously introduced 13.5-μm diameter active area.

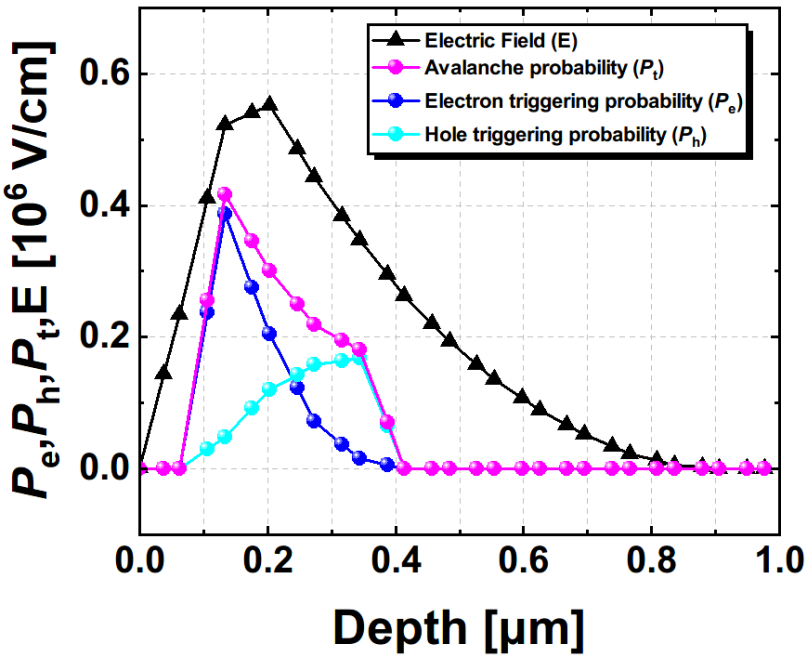


Fig. 5-4. TCAD simulation results of the avalanche probability distribution.

Fig. 5-5 compares the Verilog-A simulation results with the measured data for various DCR components as V_{EX} increases. As V_{EX} increases, the contribution from BTBT becomes more significant than thermal noise. The strong electric field narrows the bandgap,

increasing the BTBT-related DCR. The close match between the simulation and measured results demonstrates the accuracy of the DCR modeling.

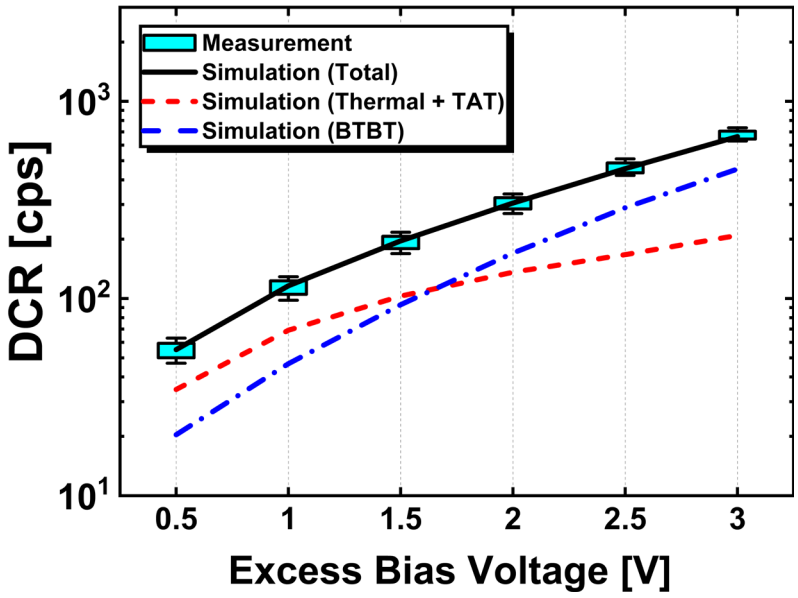


Fig. 5-5. Comparison of the DCR between the measurement and simulation as a function of V_{EX}.

The proposed Verilog-A model also accounts for variations in DCR with temperature. Fig. 5-6 compares the simulation results and the measurements of each DCR component as the temperature increases from 20 °C to 80 °C. The results closely align with the measured data, demonstrating that the DCR modeling is accurate and that system design optimization can account for the devices' differing temperature sensitivities. As the temperature increases, thermal noise becomes the dominant component of the DCR.

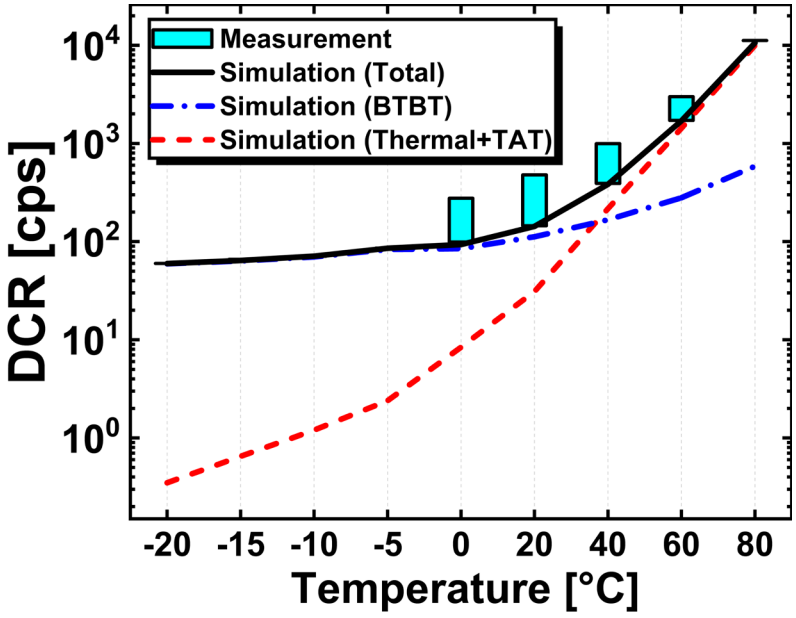


Fig. 5-6. Comparison of the DCR between the measurement and simulation as a function of temperature.

Fig. 5-7 illustrates how the DCR changes as V_{EX} increases, with measurements taken at 20 °C intervals from 0 °C to 80 °C. A close agreement between the measured and simulated data was observed, indicating that the DCR variation due to increasing V_{EX} diminishes as the temperature rises.

By incorporating the DCR characteristics into the Verilog-A SPAD model, the proper operation of the circuit system can be verified, even for devices with significant DCR. Additionally, when designing an on-chip histogram, the DCR can be integrated into the histogram to optimize circuit performance during simulation, as well as enabling

simulations that account for the changes in SPAD's DCR under various temperature conditions.

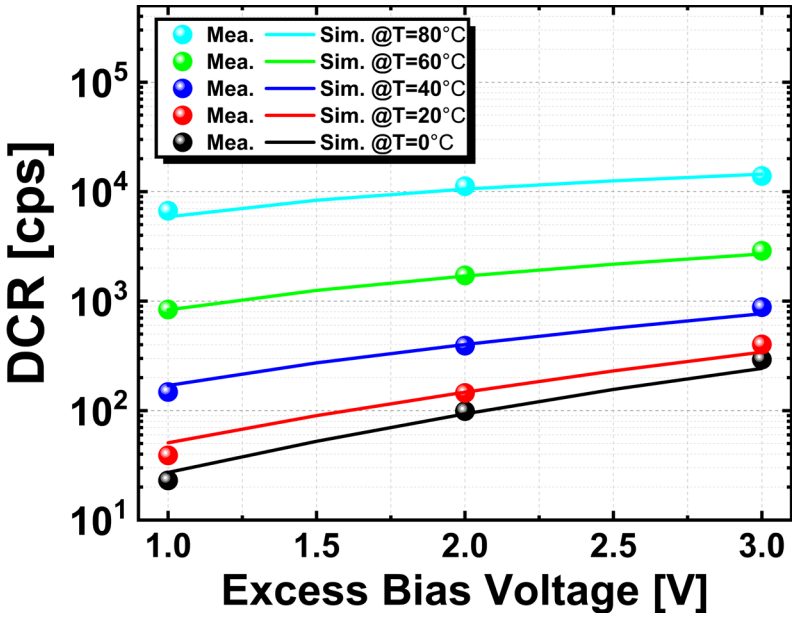


Fig. 5-7. Comparison of the DCR between the measurement and simulation as a function of V_{EX} and temperature.

5.3. Circuit simulation

In Fig. 5-8, it can be observed that the advanced SPAD Verilog-A model presented in this thesis generates output pulses in response to photon input. Circuit simulations were also conducted to verify that the SPAD's DCR properties were accurately reflected, as shown in Fig. 5-9. An equivalent circuit model of the probes and oscilloscopes was incorporated to account for the parasitic components under real measurement conditions.

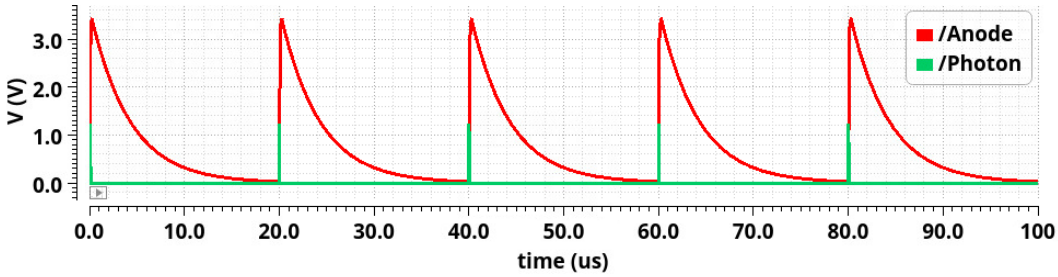


Fig. 5-8. Pulse simulation results from the advanced Verilog-A model.

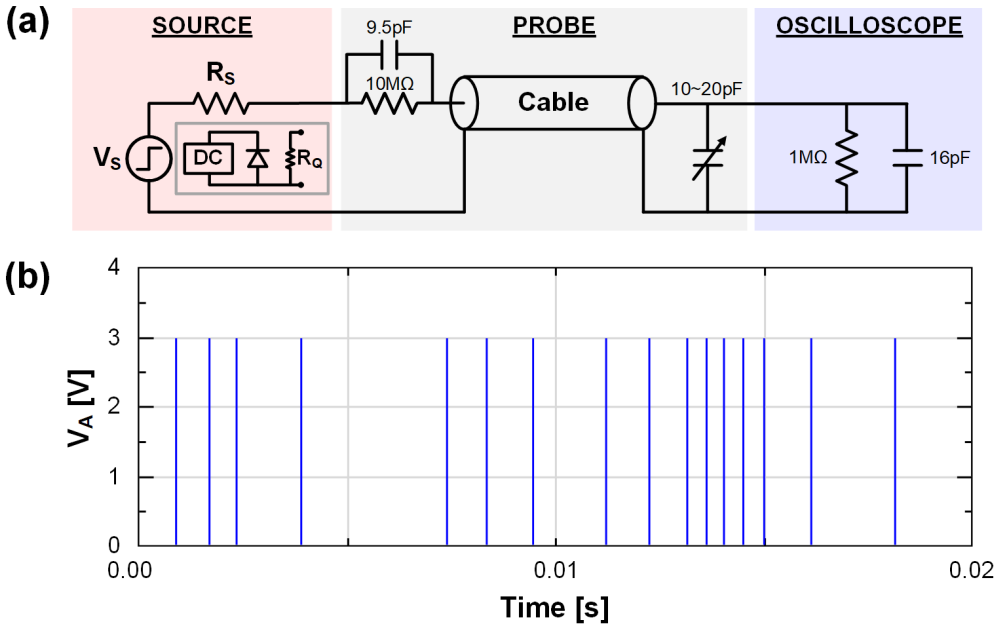


Fig. 5-9. (a) Schematic of the equivalent circuit model for the parasitic components under measurement conditions. (b) Simulation results from the proposed Verilog-A model.

Subsequently, simulations were conducted using two different approaches: a conventional approach that did not account for the voltage drop due to R_S, employing a resistance of several kΩ as the avalanche current path, and an advanced approach that incorporated a model with well-reflected device parameters, as illustrated in Fig. 5-10. The simulation results for the optimized P-EPI GR SPAD with a diameter of 9 μm, based on the device parameters discussed in Chapter 4, revealed significant differences between the two models. The measured slew rate was 63 MV/s, while the conventional model yielded a simulated value of 152 MV/s, resulting in a 140 % error. In contrast, the advanced Verilog-A model achieved a simulated value of 76 MV/s, reducing the error to 20 %. This demonstrates the improved accuracy of the advanced modeling approach in capturing the device's actual performance.

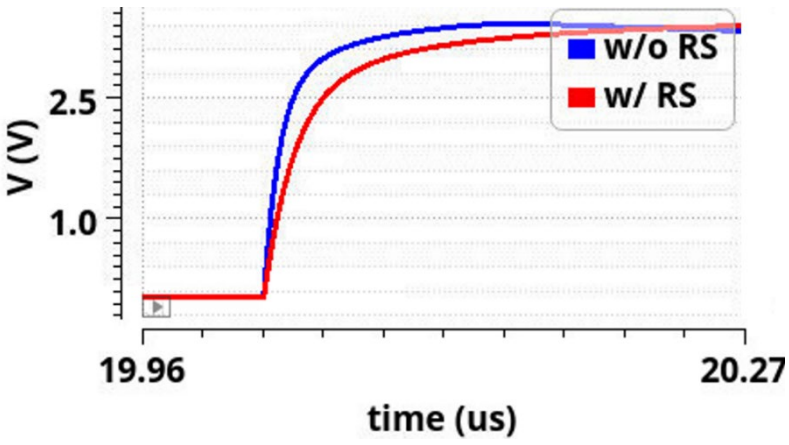


Fig. 5-10. Comparison of the pulse simulation results between the conventional Verilog-A model and the advanced Verilog-A model.

The AFE gate is directly connected to the SPAD's anode output, making optimization critical. Fig. 5-11 presents the simulation results conducted without AFE optimization, using the same AFE transistor size and voltage conditions for SPADs with active area diameters of 13.5 µm and 4.5 µm. The smaller SPAD did not quench effectively due to its low current gain. In such cases, AFE optimization requires modifications, such as adjusting the quenching transistor's gate operating voltage or altering the transistor size. In circuits like analog-digital counters, SPADs with a pitch of approximately 60 µm are commonly used due to fill factor considerations. Despite the difference in active area diameters between 4.5 µm and 13.5 µm, AFE optimization is still necessary due to device parameter differences. As the size increases, these differences become more significant, making AFE optimization using the advanced Verilog-A model essential.

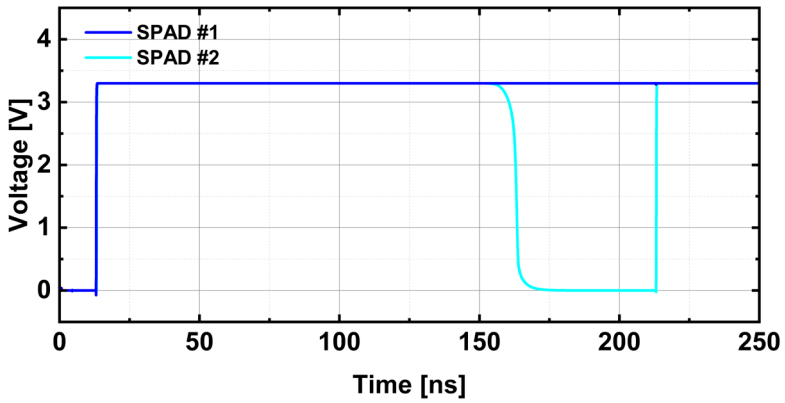


Fig. 5-11. AFE simulation results using the advanced Verilog-A model for SPADs with active area diameters of 13.5 µm (SPAD #2) and 4.5 µm (SPAD #1) before optimization.

6. Conclusion

This thesis presents the first-ever equivalent circuit model of a SPAD, incorporating the space-charge resistance. This model provides a deeper understanding of SPAD devices and elucidates the relationship between device parameters and performance characteristics. Through modeling, it was revealed that the HVPW GR SPAD exhibits a high inner series resistance due to the extended current path caused by the heavily doped HVPW layer. To address this issue, the GR structure was optimized to create a shorter current path. Simultaneously, to enhance the photon detection probability (PDP), an optimized P-EPI GR layer—a virtual guard ring rather than a physical layer—was adopted. As a result, the avalanche multiplication region was extended into the designed GR area. Modeling results confirmed that the optimization successfully achieved its objectives, as validated through the comparison of device parameters. Experimental results were consistent with the modeling outcomes, further substantiating the findings.

This equivalent circuit model is anticipated to play a significant role in modeling-based device optimization. For further analysis, the optimized P-EPI GR SPAD was modeled for active area diameters of 4.5 μm, 9 μm, and 13.5 μm to study the effects of size variation on device parameters and explore the trade-offs in SPAD miniaturization. Contrary to conventional expectations that smaller SPADs would exhibit reduced timing jitter due to decreased RC values, the study revealed that timing jitter worsens with miniaturization. This is because the space-charge resistance inversely scales with the active

area, increasing the device resistance and thereby reducing the slew rate. These results highlight a trade-off between power consumption and timing jitter in SPAD miniaturization.

Finally, this model was integrated into a conventional Verilog-A framework capable of simulating the static, dynamic, and statistical behavior of SPADs in commercial circuit simulators. By incorporating accurate device parameters, this approach overcame previous limitations, enabling simulations of static behavior that closely matched measured I-V characteristics. Dynamic behavior was also improved by accurately reflecting parasitic capacitance, leading to enhanced precision.

The accurate integration of the SPAD's RC components into the Verilog-A model not only improved the static and dynamic behavior of the SPAD but also facilitated the optimization of the entire circuit system, including the AFE. This advanced Verilog-A model is expected to be actively employed in applications such as on-chip histogram design, AFE optimization, circuit design considering temperature-dependent DCR, and quenching resistor optimization in analog SiPMs.

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Abstract in Korean

CMOS 공정 기반 단일 광자 애벌랜치 다이오드의 등가 회로 모델을 통한 소자 분석 및 최적화

단일 광자 애벌랜치 다이오드 (SPAD)는 근적외선 파장대역에서도 단일 광자를 감지할 수 있는 고감도 검출기이다. CMOS 공정 기술의 발전으로 SPAD는 비용 효율적인 대량 생산이 가능 해졌을 뿐만 아니라, 사용자 맞춤형 설계 방식으로 전자 회로와 통합할 수 있게 되었다. CMOS 공정에서 제작된 SPAD는 고효율 특성과 호환성 덕분에 시간비행 시스템, 라이다, 증강현실 및 가상현실, 의료 장치, 양전자 방출 단층촬영, 양자 컴퓨팅과 같은 양자 기술 분야 등 다양한 분야에 널리 응용되고 있다. 이러한 응용에서 전체 시스템의 성능을 좌우하는 SPAD의 성능을 향상시키기 위해 설계 최적화가 필요하며, 이를 위해서는 소자 구조에 따른 물리적 특성을 정확히 이해하는 것이 필수적이다.

본 논문에서는 CMOS 공정 기반 SPAD의 등가 회로 모델을 제안하며, 기생 성분을 포함한 주요 소자 구조의 물리적 특성을 표현하는 파라미터를 GSG pad를 이용한 디임베딩 과정을 통해 추출하였다. 이 과정에서 S 파라미터 측정, 수식 기반 파라미터 값 도출, TCAD 시뮬레이션, ADS를 이용한 측정값과 시뮬레이션 값의 비교 과정이 동반되었다. 모델링 결과, 기존의 high voltage P−well (HVPW) 가드링 구조가 높은 내부 직렬 저항 성분을 야기하는 것을 확인하였고, 이를 기반으로 최적화된 가드

링 구조를 제안하였다. 또한, 소자의 크기 변화가 소자 파라미터에 미치는 영향을 분석하기 위해 각각 active area 지름 13.5 um, 9 um, 4.5 um을 가지는 SPAD를 모델링하였고, 그 결과 소자의 크기가 작아질수록 RC 성분 또한 작아져 좋은 타이밍 지터를 가질 것이라는 기존의 기대와 달리 공간 전하 저항 값의 증가로 타이밍 지터 성능이 감소하는 것을 확인하였다. 이를 통해, SPAD 소형화 시 타이밍 지터와 전력 소모량의 상충관계를 확인하였다. 이후 소자의 임피던스 특성을 정확히 반영하는 해당 등가 회로 모델을 기존의 Verilog-A 모델에 통합하여 SPAD의 정적 및 동적 동작 특성 시뮬레이션에 대한 정확도를 향상시켜, 상용 회로 시뮬레이터에서의 아날로그 프론트 엔드 설계의 최적화를 가능하게 했다.

위와 같은 연구 결과를 통해, CMOS 공정 기반 SPAD의 구조에 따라 달라지는 물리적 특성에 대한 정확한 이해가 가능 해졌으며, 향후 지속적인 등가 회로 모델 기반의 소자 설계 최적화를 기대할 수 있다.

핵심되는 말 : 광소자, 단일 광자 검출 소자, 단일 광자 애벌랜치 다이오드, 등가 회로 모델, 모델링 기반 소자 최적화, 표준 CMOS 공정, 포토다이오드