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The 14th International Conference on Advanced Materials and Devices

ICAMD 2025

December 8–12, 2025 | BEXCO, BUSAN, KOREA

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Applied Physics Division, The Korean Physical Society

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December 10 (Wed), 2025

Poster Session 3

18:15~20:15

1F & 2F Lobby

Materials and Devices for Advanced CMOS Technology

WED-MA25-208 **Work function modulation of electrodes inducing self-rectification in HfZrO2-based FTJ for crossbar array**
Hyeon Jin Ahn, Jung Ho Yoon
(Sungkyunkwan University)

WED-MA25-267 **Emergence of ferroelectricity in annealing-free Hf0.5Zr0.5O2 with MoO3 interlayer driving oxygen ion migration**
Moonseek Jeong, Min Hyuk Park, Geun Hyeong Park, Dong Hee Han, Taegyu Kwon, Yong Hyeon Cho, Dong In Han
(Department of Materials Science and Engineering, College of Engineering, Seoul National University)

WED-MA25-324 **Enhanced NiSi formation via template effect and suppression of Ni channeling by employing Mo2N interlayer**
Jiwan Hong, Seoeun Yoon, Woojin Jeon
(Kyung Hee University)

WED-MA25-335 **Suppressing residual Cl-induced defect from TiCl4-based ALD TiN into ZrO2 by introducing an In2O3 capping layer for MIM capacitors**
Hunseok Son, Seoeun Yoon, Seungwoo Lee, Soo Min Yoo, Woojin Jeon
(Kyung Hee University)

WED-MA25-443 **Switching Dynamics of MIS, MFM, and MFMIS Capacitors under Pulsed Voltage Operation**
Minu Kang, Cheol Jun Kim, Teahee Noh, Hyeon Su Seong, Seung Jin Kang, Bo Soo Kang
(Hanyang university)

WED-MA25-470 **Optoelectronic Charge Trap Memtransistor for Vision Explainable Artificial Intelligence Hardware**
Min Gu Lee, Kyung Min Kim
(Korea Advanced Institute of Science and Technology)

WED-MA25-524 **Development of Si-Photonics IP Bank and Monolithic Coherent Optical Transmitter for Energy-Efficient Interconnects**
Kangyeob Park*, Hyun-Do Jung**, Junhyeok Seo*, Wonseok Oh*
(*Korea Electronics Technology Institute, **OE Solutions, Co., Ltd.)

WED-MA25-539 **MoS_2 Channel-based Charge Trap Flash Memory with Optimized Sensing Methodologies for In-Memory Computing**
Ki Han Kim*, Ju Han Park*, Khang June Lee**, Ji-Won Seo***, Yeong Kwon Kim*, Junhwan Choi****, Min-Jae Seo***, Byung Chul Jang*
(*Kyungpook National University, **The University of Suwon, ***University of Seoul, ****Dankook University)

WED-MA25-558 **High-Speed 64-GBd PAM4 Driver with Passive On-Chip Coplanar Waveguide Equalizer Integrated with MZI-Based Optical Modulator**
Junhyeok Seo*, Kangyeob Park**, Wonseok Oh**, Woo-Young Choi*
(*Yonsei University, **Korea Electronics Technology Institute)

WED-MA25-586 **Large-Area Application of Nanocrystalline Ni-Co-Fe Alloy-Carbon Composite for Electromagnetic Interference Shielding**
Jihun Lee, Joohoon Kang
(Yonsei University)

WED-MA25-589 **Two-dimensional template-assisted conversion for ultrathin indium oxide-based single-gate reconfigurable transistors**
Jinhong Min*, Myeongjin Jung**, Joohoon Kang*
(*Yonsei university, **Sungkyunkwan University)

WED-MA25-602 **Symmetry-guided property optimization of Pca2_1 Hf-based fluorite ferroelectrics**
Jinhyeong Jo*, Pawan Kumar**, Chang Hun Kim**, Jun Hee Lee**
(*Korea Institute of Science and Technology, **Ulsan National Institute of Science and Technology)

WED-MA25-612 **Interfacial Defect Control of ZrO2/TiN-Based DRAM Capacitors Using TiO2 Buffer Layer**
Hyeongjun Kim, Seungmin Jo, Woongkyu Lee
(Soongsil University)

WED-MA25-614 **Atomic Layer Etching of ZrO2 Using SF6 Plasma and TiCl4 for DRAM Capacitors**
Juhyeong Kim, Sangyeon Jeong, Woongkyu Lee
(Soongsil University)

WED-MA25-616 **Enhanced Switching Uniformity in HfO2-Based RRAM via Control of TiN Deposition and TiOxNy Formation**
Seokho Cho, Juan Hong, Woongkyu Lee
(Soongsil University)

High-Speed 64-GBd PAM4 Driver with Passive On-Chip Coplanar Waveguide Equalizer Integrated with MZI-Based Optical Modulator

Junhyeok Seo[1,*], Kangyeob Park[2], Wonseok Oh[2], and Woo-Young Choi[1,**]

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This paper presents the design and integration of a high-speed 64-GBd four-level pulse amplitude modulation (PAM4) driver co-optimized with a Mach–Zehnder interferometer (MZI)-based optical modulator for next-generation optical interconnects. The proposed driver architecture employs a passive feed-forward equalizer (FFE) realized with on-chip coplanar waveguides (CPWs), which function as tunable delay elements. This approach eliminates the need for clocked equalization circuits, enabling fully asynchronous operation across a wide frequency range from DC to the 3-dB bandwidth limit of 55 GHz. The driver incorporates a high-swing transconductance (Gm) cell enhanced by an external gate impedance network, thereby ensuring improved linearity and sufficient modulation depth required for high-order PAM4 signaling. The integrated silicon MZI modulator, fabricated with 2-mm-long upper and lower arms, achieves an electro-optical (E-O) bandwidth of 35 GHz and an extinction ratio exceeding 6 dB. Post-layout simulation results confirm high-speed operations at 64-GBd PAM4 signals with a 3-Vpp differential output swing, achieving an eye opening of 0.55 UI with minimized inter-symbol interference (ISI) and a bit-error rate of 2.4×10^{-4} after modeled fiber transmission. The effect of CPW-based passive equalization and MZI integration enables superior bandwidth extension, reduced energy consumption, and enhanced scalability. The proposed driver can be applied in next-generation optical interconnect systems with low-power, high-capacity, high-linearity capabilities.

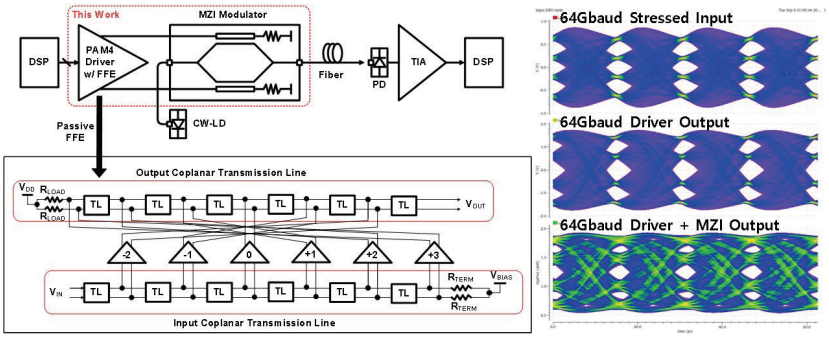

Fig 1. Proposed 64Gbaud PAM4 driver and post-layout simulation results

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