1 Gbps gated-oscillator burst mode CDR with half-rate clock recovery

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Abstract A new burst mode clock and data recovery circuit is realized that improves the previously-known gated-oscillator technique with half rate clock recovery. The circuit was fabricated with 0.25um CMOS technology, and its functions were confirmed up to 1 Gbps.

Keywords: Burst mode, PON, clock and data recovery, gated oscillator;

1 Introduction

In Passive Optical Network (PON) systems [1], Optical Line Termination(OLT) in the central station does not know exactly when data packets arrive from various Optical Network Units (ONUs) located at the subscriber side as shown in Fig. 1. Consequently, OLT receiver has to align the receiver clock to each burst data packet.

In this paper, we propose a new circuit configuration that has half-rate clock recovery capability thus improving the speed performance of gated-oscillator clock recovery circuits.

2 Gated-oscillator CDR

Fig. 2 shows a gated ring oscillator. An AND gate acts as the gate and can turn on and off the oscillation. If Enable is low, the oscillation stops and if Enable is high, the oscillation starts again. In addition, the oscillation always begins with the signal falling from high to low. Consequently, output clock phase can be set to a desired value by the Enable signal.

In gated-oscillator CDR, input data are used as Enable signals for two gated oscillators as shown in Fig. 3 and output clock is generated whose phase is always aligned with the input data.

The conventional PLL-based clock recovery circuit cannot be used for burst mode application since it requires a long sequence of overhead bits to reach the lock condition. In addition, the clock frequency can drift away during the silent times, which require another phase-locking process.

The above problem can be solved with the gated-oscillator clock recovery technique[2], in which “gate stage” is added in the signal path of ring oscillators, making it possible to instantly align the clock phase with data. This technique is simple and requires low power but has limited high-speed operation.
An alternative way to overcome the device speed limitation is to use multi-phase clock technique, in which more than two identical operations are performed within one clock cycle as in DDR (Double Data Rate) memory using both rising and falling edges to read and write the data, doubling the bandwidth. Recently, many researchers have used this idea for continuous-mode clock recovery applications [3,4] but no attempt has been made for gated-oscillator burst mode applications. We propose a new circuit structure in which the output clock phase can be selectively set to either 0 or π, making gated-oscillator CDR with half-rate clock recover possible.

**2.1 Gated oscillator details and problems with half rate clock recovery**

Another problem arises when you come to build half rate clock recovery with the gated oscillator. Shown as “ideal clock” in Figure 5, recovered half rate clock has to be shifted from the data transition edges exactly π/2 for optimum sampling, but gated oscillator always aligns the clock edge to data edges. Therefore you need delayed version of recovered clock, and it will be accounted later.

**3 Proposed half rate CDR**

With the new version of gated oscillators, we designed a half rate clock recovery circuit shown in Figure 8. It has two gated oscillators, each having ???, and they are switched by input data. This circuit differs from the conventional gated-oscillator CDR in the following points.

First, our new gated oscillators require the reset phase setting value R0 and R1. Since both rising and falling edges are required, it has to alternate the reset phase value supplied by the oscillators.
Second, the half portions of the recovered clock are combined using a MUX, not an OR gate, because even when the oscillator is not oscillating, the alternating R values come out to the output and may corrupt the combined clock. Data signals are also used as the MUX selecting signals so that the output path can be switched to the clock-generating gated oscillator resulting in complete half rate clock signals aligned with the data.

여기에 serializer 가 포함된 전체 회로 block diagram 필요?

4 Experimental results
The proposed half rate clock recovery circuit was designed with CMOS 0.25um parameter and verified by hspice simulation. A prototype chip was fabricated and directly attached on the test board. Figure 9 shows the micro-photograph of the chip.

Prototype chip includes 8-bit wide deserializer as well as half rate clock recovery, therefore we can observe 1/8 rate recovered clock instead of half rate clock. It was found that the fabricated chip can operate at up to 1Gbps. Figure 10 shows recovered clock from the PRBS11 data, and the measured clock jitter was 4.6ps[rms].

Figure 8. Recovered clock from PRBS11 and jitter measurement

Burst mode as well as continuous mode operation was verified by injecting the packet-like programmed bit patterns and into the test chip, and the recovered data and clock are shown in Figure 11. Table 2 shows the summary of chip performance.

Figure 9. Micro-photograph of prototype chip

(a) Burst mode data and recovered clock data
(b) Retimed and deserialized data
(c) Retimed and deserialized data from continuous mode data

Figure 11. Half rate clock recovery operations
Table 2. Starting phase and corresponding R0 and R1

<table>
<thead>
<tr>
<th>Process</th>
<th>CMOS 0.25um</th>
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<tbody>
<tr>
<td>Power supply</td>
<td>2.5V</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>1Gbps for PRBS15</td>
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<tr>
<td>Recovered clock jitter</td>
<td>4.6ps[rms] for PRBS11</td>
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<tr>
<td>Power consumption</td>
<td>100mW core, 375mW including deserializer and I/O</td>
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</tbody>
</table>

References


