

Introduction

❖ Topic

- Development of SerDes IP based on 65nm CMOS

❖ Team member

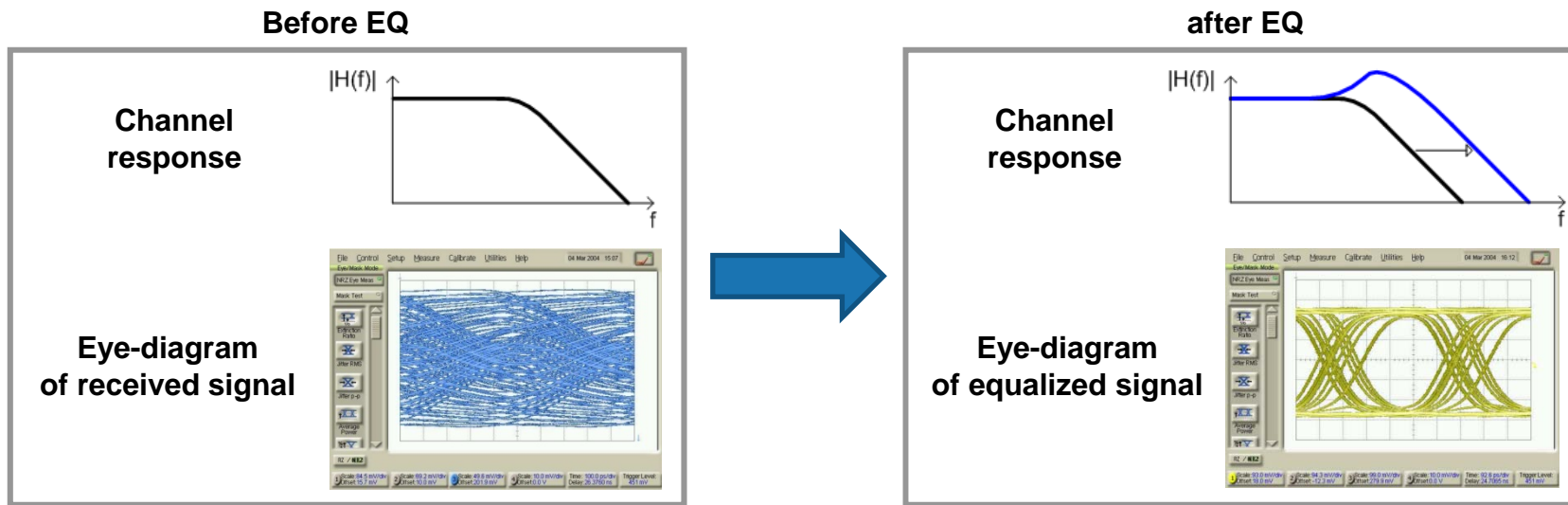
- Team member: K.C Choi, C.K Seong, Y.S Park and W.S Kim
 - CDR (Clock and Data Recovery) part: K.C Choi
 - PLL (Phase-Locked Loops) part: Y.S Park
 - Equalizer part: C.K Seong and W.S Kim

❖ Sponsor

- Samsung Electronics

Research explanation

❖ 5-Gb/s adaptive line equalizer (EQ)



❖ Focus of research

- New adaptation algorithm
- Mostly digital control

