

Introduction

❖ Topic

- Wireless Transceiver SOC for 60GHz WPAN

❖ Team member

- Team member: D.H Kim, J.Y Kim, M.S Ko
 - 60GHz LNA: D.H Kim
 - 60GHz Oscillator: J.Y Kim
 - 60GHz Mixer: M.S Ko
 - High Speed MODEM: D.H Kim

❖ Sponsor

- 한국과학재단 특정기초 연구 - CMOS 기반 60GHz 광대역 송수신기 구현

Introduction



- A network for interconnecting devices centered around an individual person's workspace
- **Typical WPAN range < 10m**
- IEEE 802.15.3 is one of WPAN standard
 - Data rate: 11, 22, 33, 44 and 55Mbps
 - Ad-hoc peer-to-peer networking
 - Security
 - Low power consumption
 - Low cost



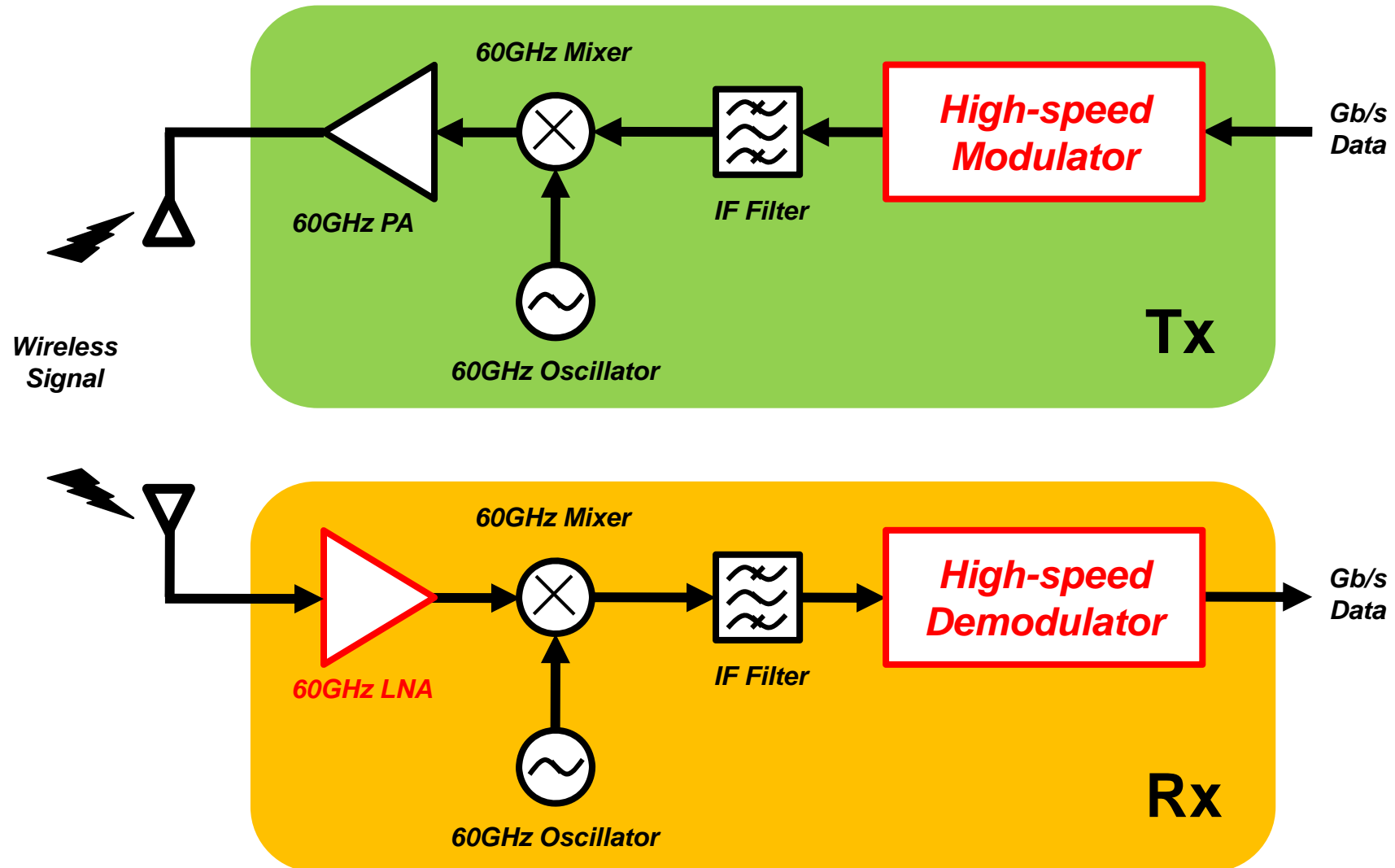
Demands for higher rate transmission (wireless HD video, wireless USB)



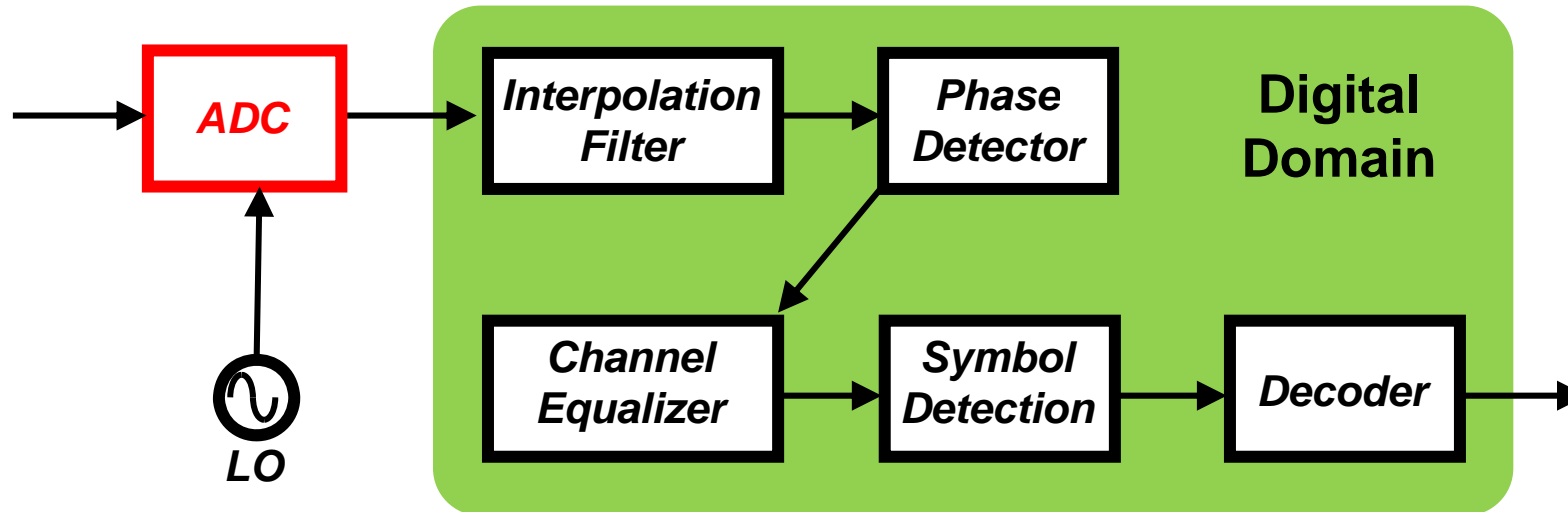
**Formation of IEEE 802.15.3c
Millimeter-wave WPAN for Gbps Tx**



Superheterodyne Receiver

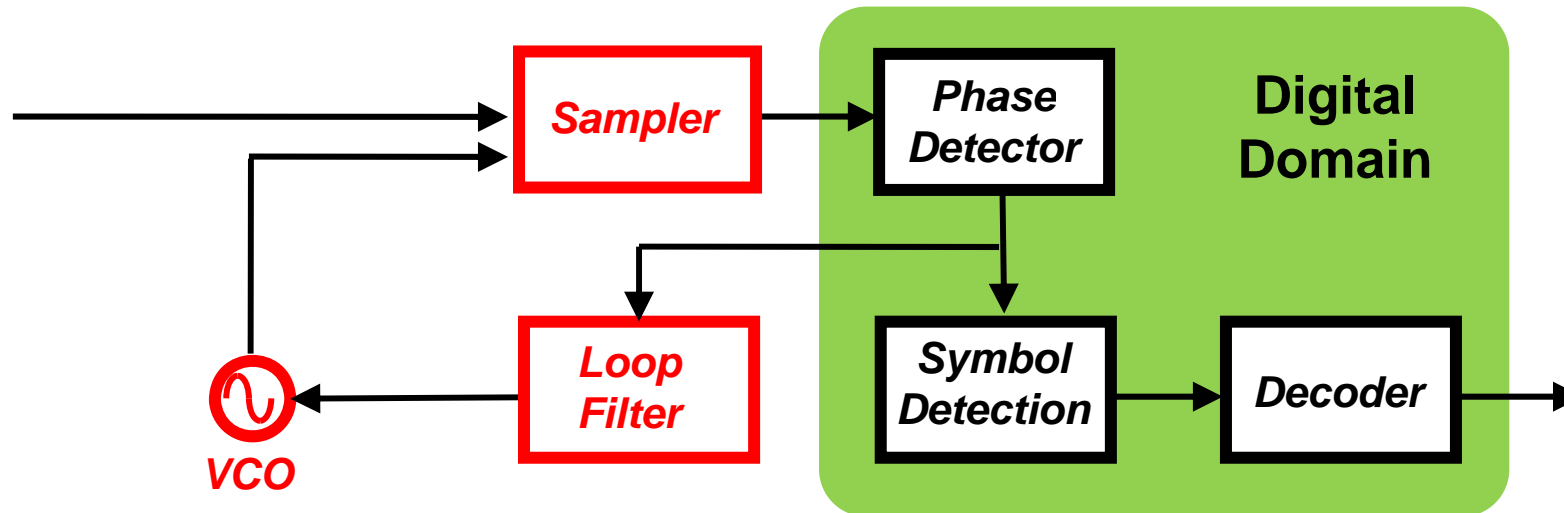


Classic Scheme of Demodulator



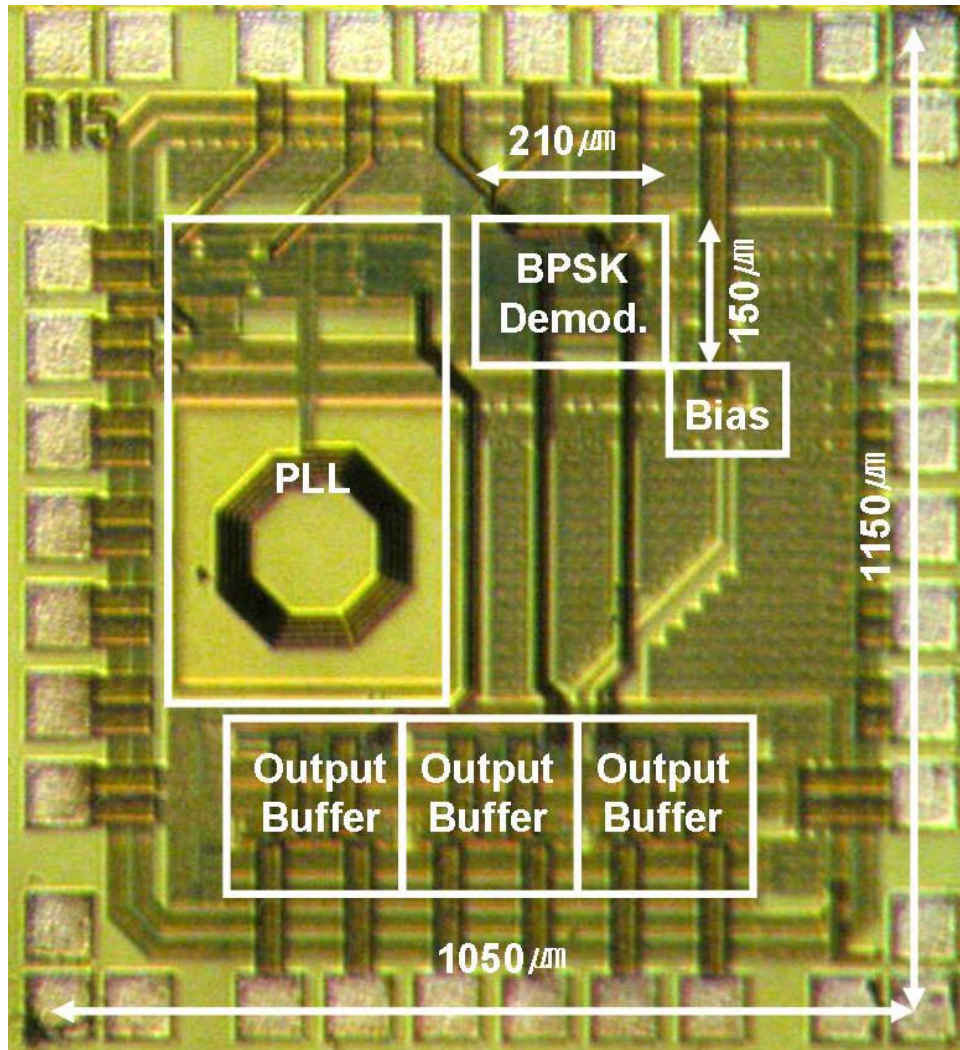
- ❖ QPSK demodulator usually requires at least 4-bit resolution.
- ❖ ADC speed > Nyquist frequency (2X symbol rate)
 - ➔ Gsymbol/s ADC is required!
- ❖ But Gsymbol/s ADC is difficult in CMOS process.
- ❖ High speed ADC consumes high power and large area.

Mixed-mode PSK Demodulator

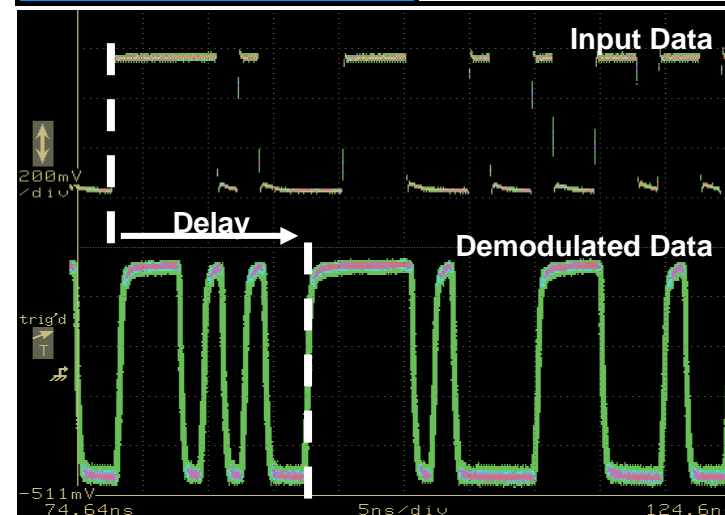


- ❖ Sampler is same as a 1-bit ADC.
- ❖ The speed of sampler has already reached 10 times of 4-bit ADC.
→ Mixed-mode demodulator has high-speed capability.
- ❖ Sampler occupies smaller size and consumes lower power.

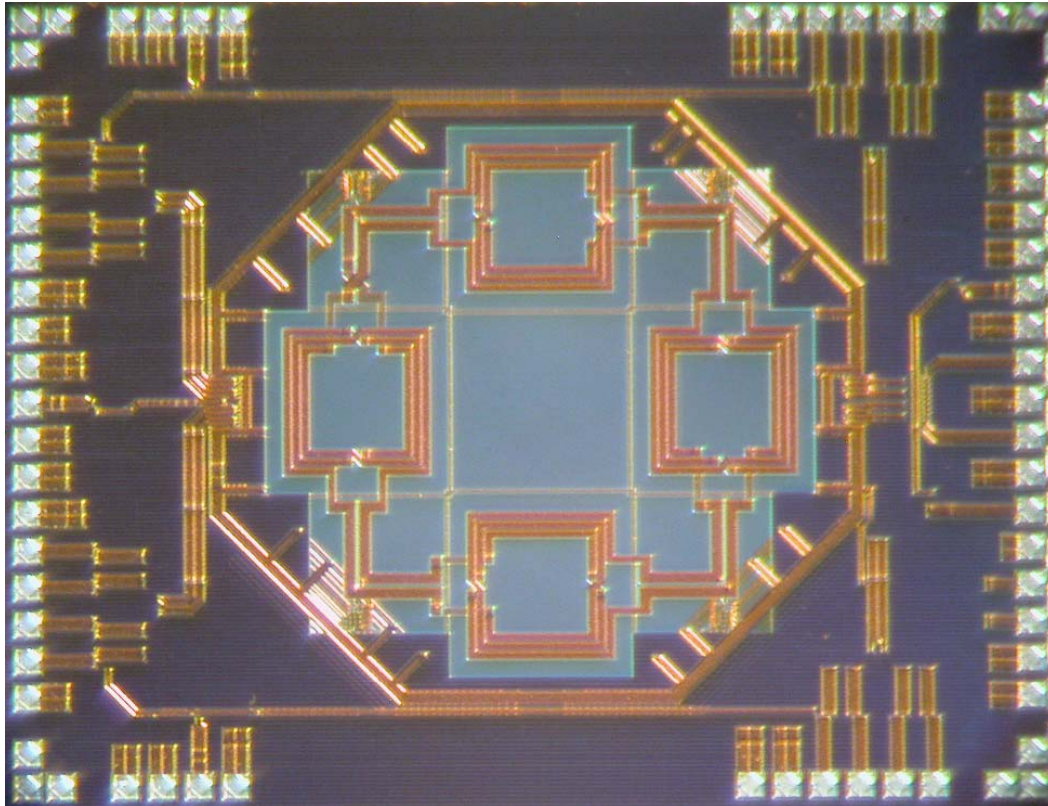
Chip#1 - BPSK Demodulator



Process	TSMC 0.18 μm
Max. data rate (PRBS 2 ⁷ -1)	622 Mb/s
Carrier frequency	1.4 GHz
Demodulator core area	210 × 150 μm^2
Supply voltage	1.8V
Power consumption	22mW (core) 288mW (w/ I/O & PLL)



Chip#2 – QPSK Demodulator



Process	Magnachip/Hynix 0.18 μm
Maximum data rate (PRBS 2 ⁷ -1)	500-Mb/s (each I/Q) 1-Gb/s (total)
Carrier frequency	1.7-GHz
Area	2.8 × 2.15 mm ² (including PAD)
	0.17 × 0.2 mm ² (core)
	1.7 × 1.7 mm ² (VCO)
Supply voltage	2.5 V
Power consumption	475-mW (including I/O)
	35-mW (core)
	67.5-mW (VCO)

❖ Journal

- Duho Kim, Kwang-chun Choi, Young-Kwang Seo, Hyunchin Kim, and Woo-young Choi, “A 622-Mb/s Mixed-mode BPSK Demodulator Using a Half-rate Bang-bang Phase Detector”, *IEEE Journal of Solid-State Circuits, in publication*

❖ Conference

- Duho Kim, Kwang-chun Choi, Young-Kwang Seo, Hyunchin Kim, and Woo-young Choi, “A 622Mb/s BPSK Demodulator with Mixed-mode Demodulation Scheme”, *IEEE Asian Solid-State Circuits Conference, pp. 288-291, 12-14 Nov. 2007*
- Duho Kim, Woo-young Choi, Young-kwang Seo and Hyunchin Kim, “A Novel BPSK Demodulating Scheme Using a Half-rate Bang-bang PD”, *SOCC 2006, COEX Conference Center, Seoul, Korea, 26~27 Oct., 2006*

❖ Awards

▪ **Chip Design Contest Second Prize**

Duho Kim, Kwang-chun Choi, Young-kwang Seo, Hyunchin Kim, and Woo-young Choi, “Mixed-mode BPSK Demodulator”, 2007 International SoC Design Conference, COEX Conference Center, Seoul, Korea, 15-16 Oct., 2007

❖ Patents

▪ “위상 검출을 이용한 복조 방법 및 그 장치”

김두호, 서영광, 최우영, 김현진

대한민국 특허 제 10-0826248, 미국, 중국, 일본, 유럽 출원 중

▪ “신호 복조 방법 및 그 장치”

김두호, 최우영

대한민국, PCT 출원 중