

# Introduction

## ❖ Topic

- Channel link analysis and design for Displayport 1.1 standard

## ❖ Team member

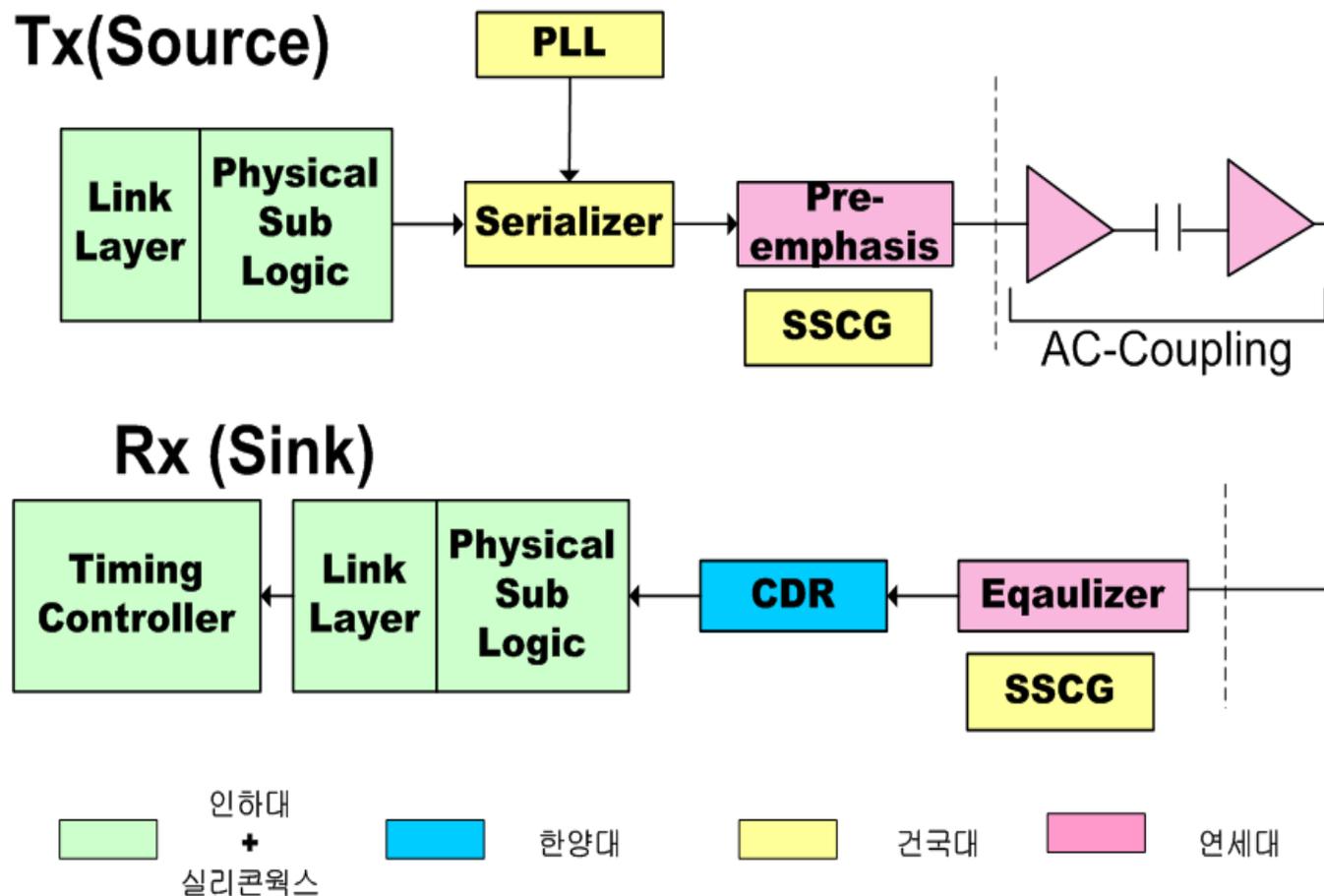
- Team member: D.H Kim, K.C Choi, and J.S Yoon
  - Channel analysis: K.C Choi
  - Circuit design: D.H Kim, J.S Yoon

## ❖ Sponsor

- "**System IC 2010**" project of Korea Ministry of Knowledge Economy

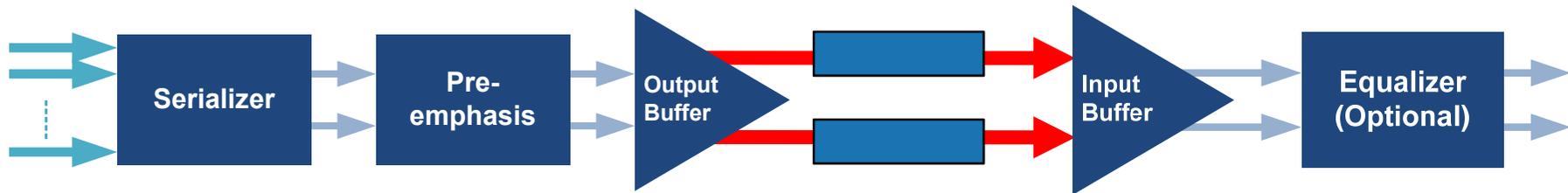
# DisplayPort 표준 핵심 IP 및 통합 칩 설계

❖ Joint research of 4 universities



# DisplayPort 표준 핵심 IP 및 통합 칩 설계

❖ Research topic of Yonsei university



**1**

**Serializer**

- CMOS logic level
- 162 / 250 Mbps
- 10 bit serializer

**2**

**I/O Buffer**

- Differential
- 0.4/0.6/0.8/1.2 Vdiff
- 1.62/ 2.7 Gbps

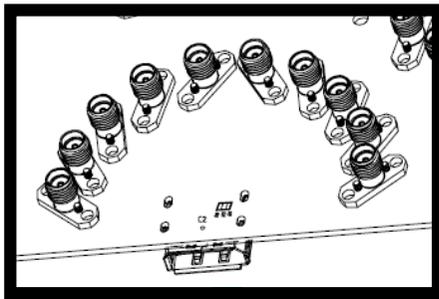
**3**

**Pre-emphasis**

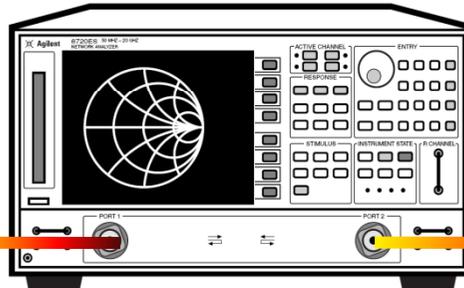
- 0/ 3.5/ 6/ 9.5 dB
- Channel modeling

# Channel Modeling

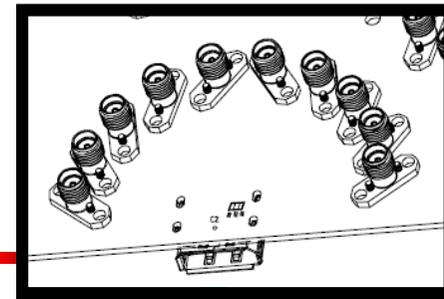
**Evaluation Board**  
MOLEX



**Network Analyzer**  
Agilent 8719ES

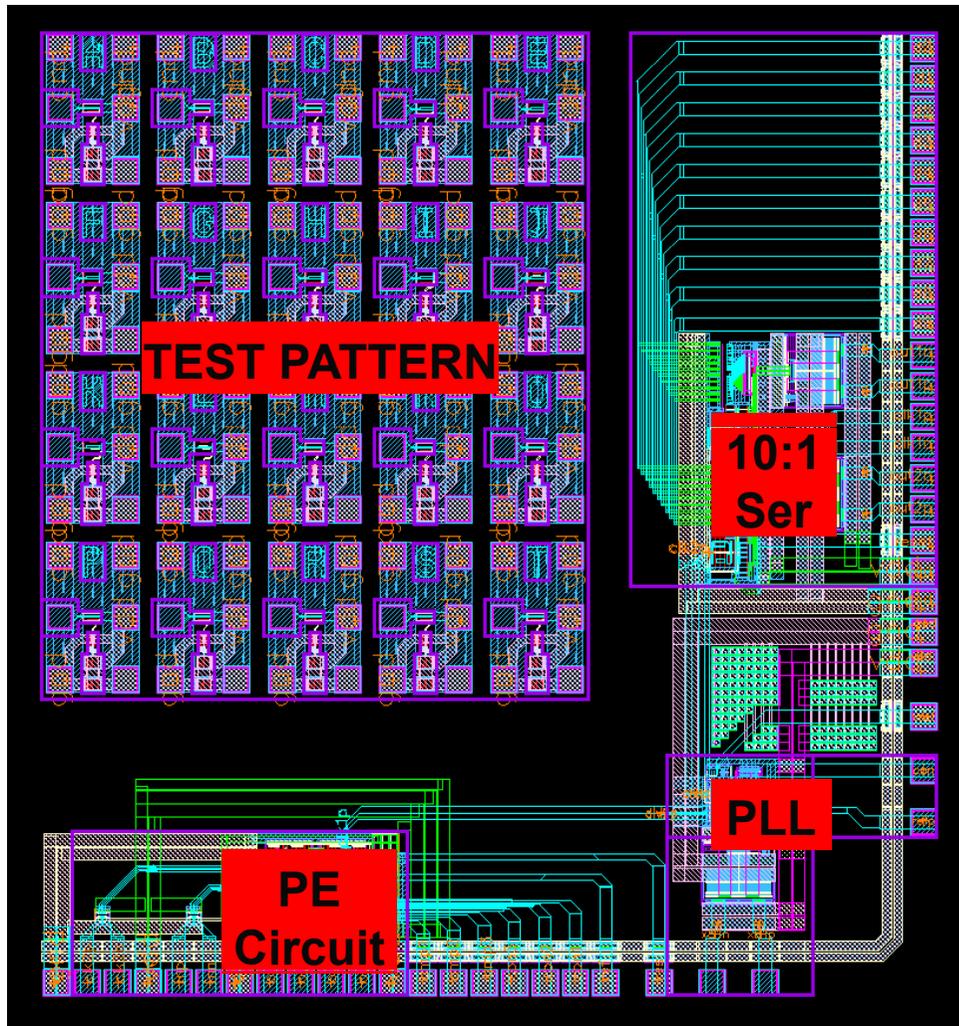


**Evaluation Board**  
MOLEX



**DisplayPort Cable**  
MOLEX

# Chip#1 – Dongbu 0.18 $\mu$ m



## Pre-Emphasis Circuit

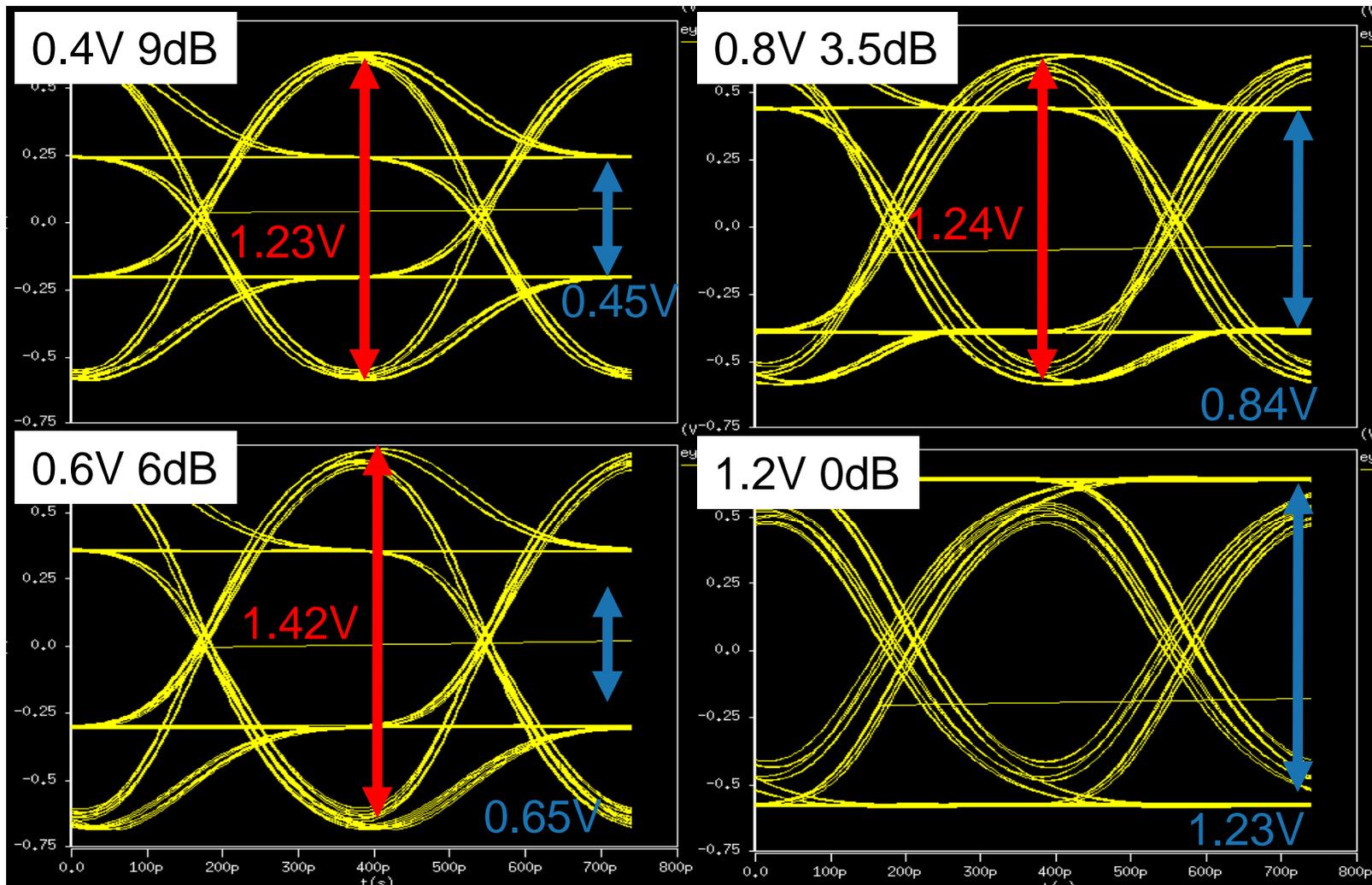
- 3.3V supply
- 220 X 250  $\mu$ m
- Maximum 45mA  
(@1.2V swing)

## 10:1 Serializer

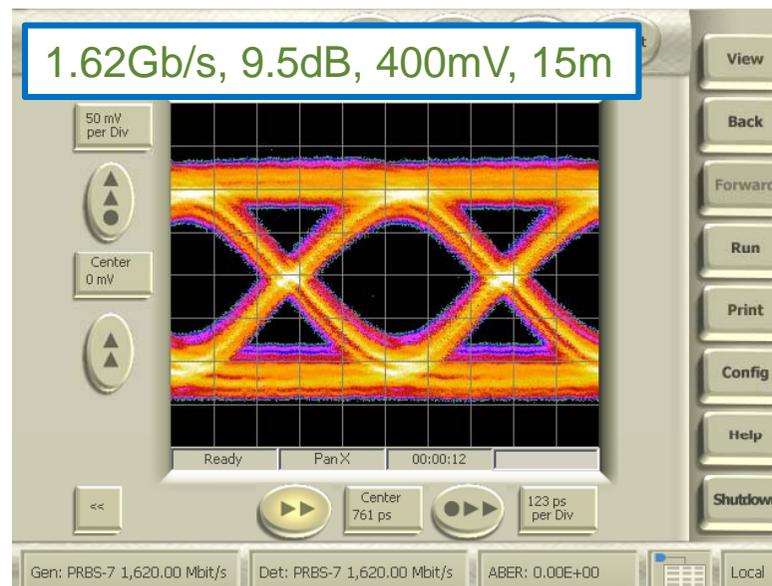
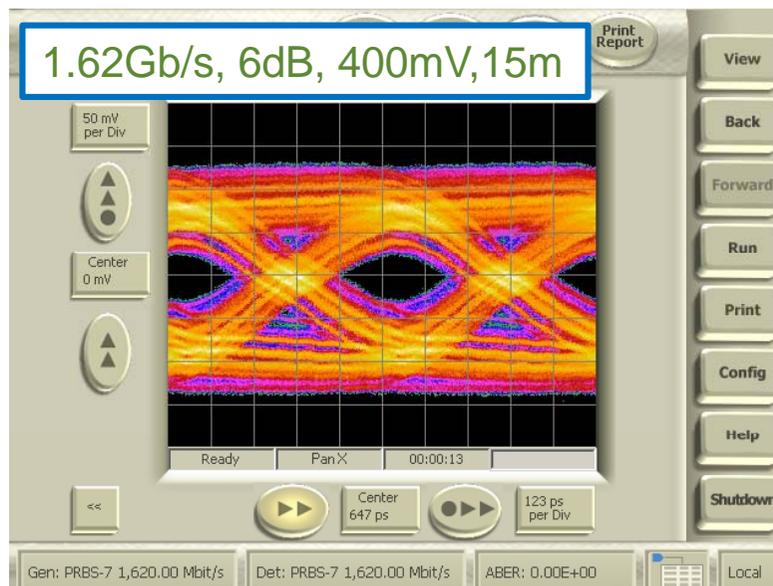
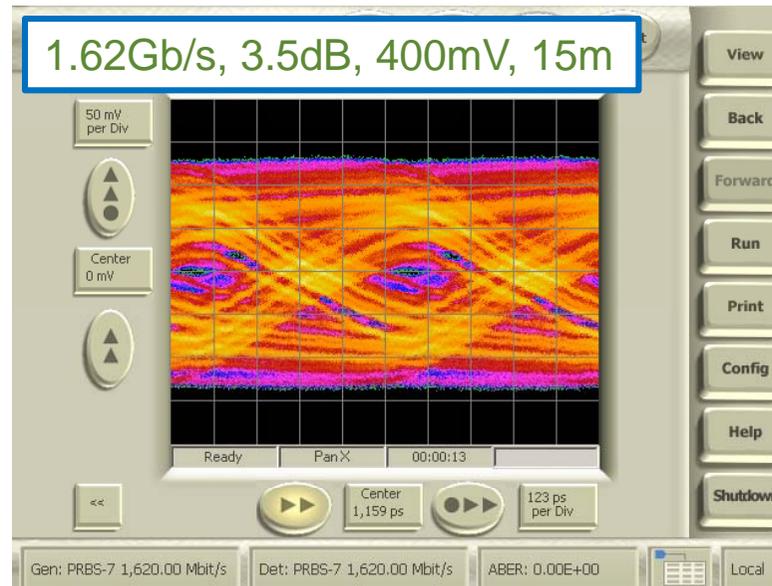
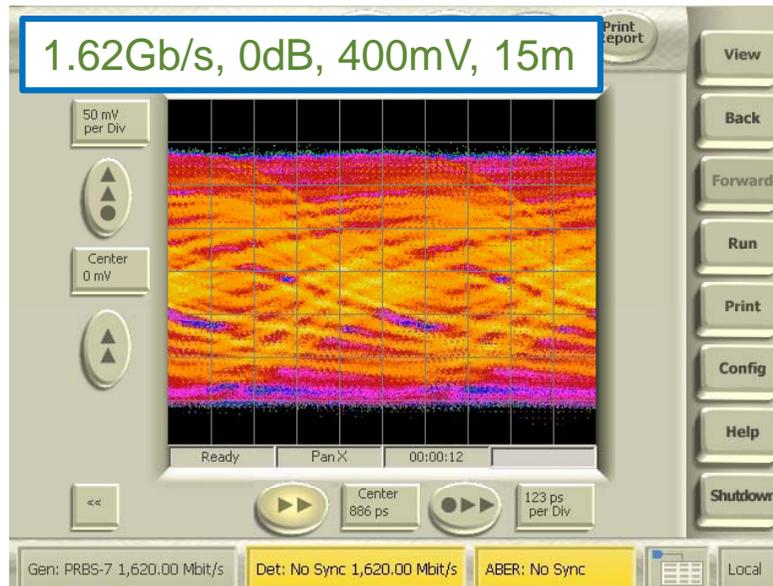
- 1.8V supply
- 120 X 290  $\mu$ m
- 2.5mA

2008. 6.30  
Chip out

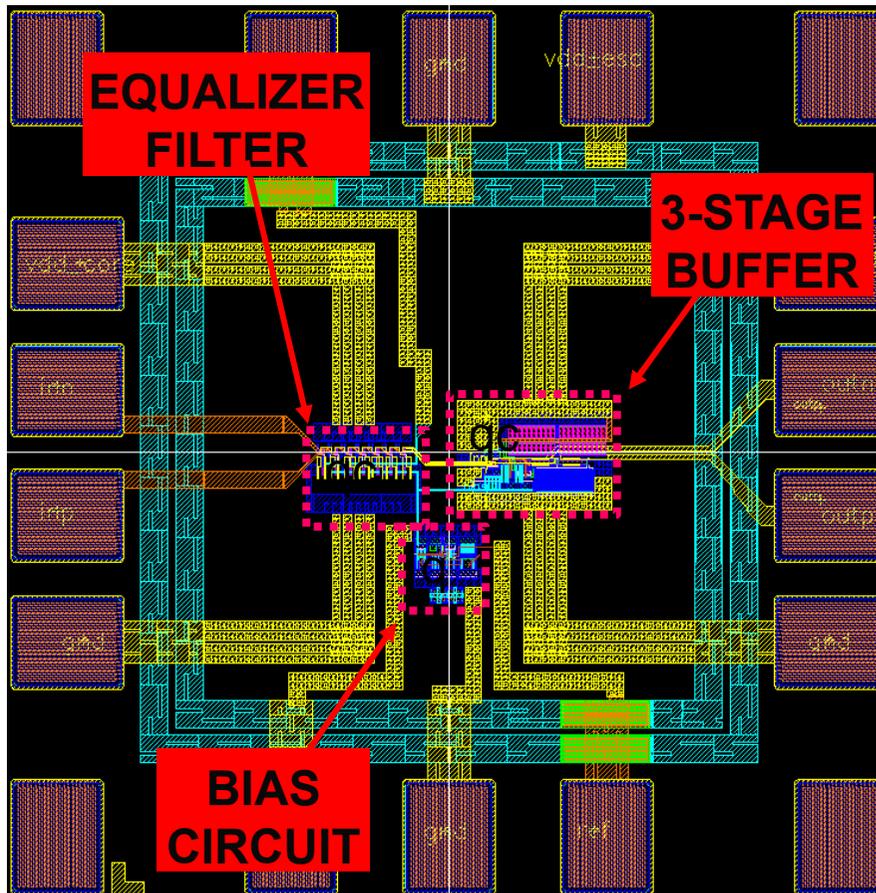
# Chip#1 – Simulation (@2.7Gb/s)



# Chip#1 – Measurements



# Chip#2 - Dongbu 0.13 $\mu$ m



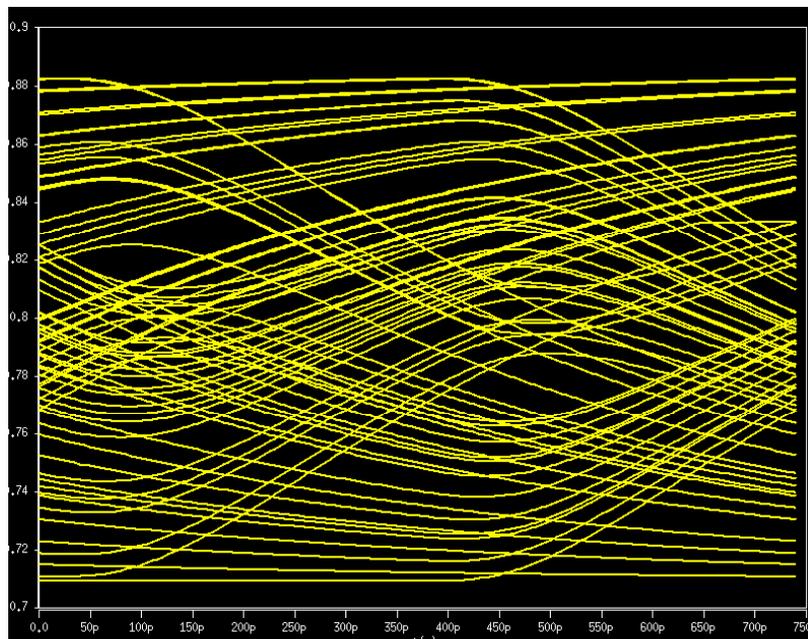
## EQUALZER Circuit

- 1.2V supply
- 55 X 70  $\mu$ m
- Maximum 1.26mW (@0.6V swing)

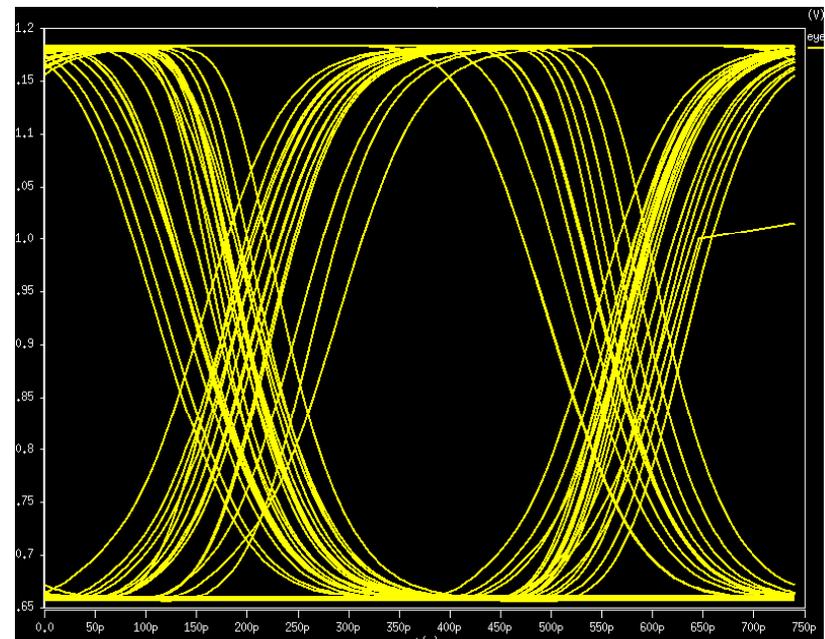
2008. 10.15  
Chip out

# Chip#2 – Simulation Results

❖ 2.7Gb/s, no pre-emphasis, 15m Cable

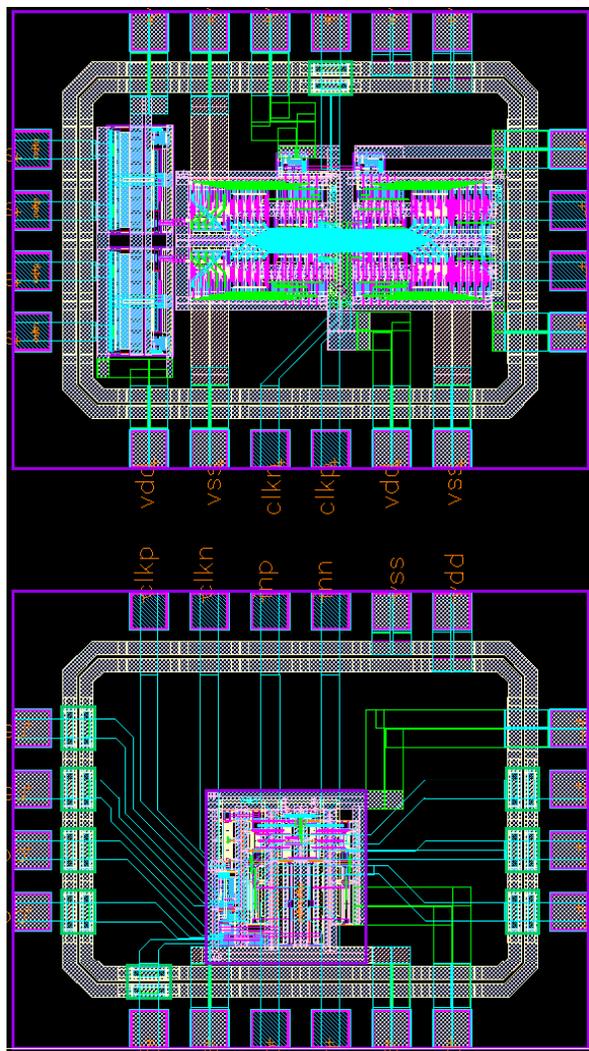


**After 15m Cable**



**After Equalizer**

# Chip#3 – Dongbu 0.18 $\mu\text{m}$



## Pre-Emphasis Circuit

- 3.3V supply
- 260 X 280  $\mu\text{m}$
- Maximum 60mA  
(@1.2V swing)

## 10:1 Serializer

- 1.8V supply
- 230 X 270  $\mu\text{m}$
- 30mA

2008. 12. 1  
Chip out