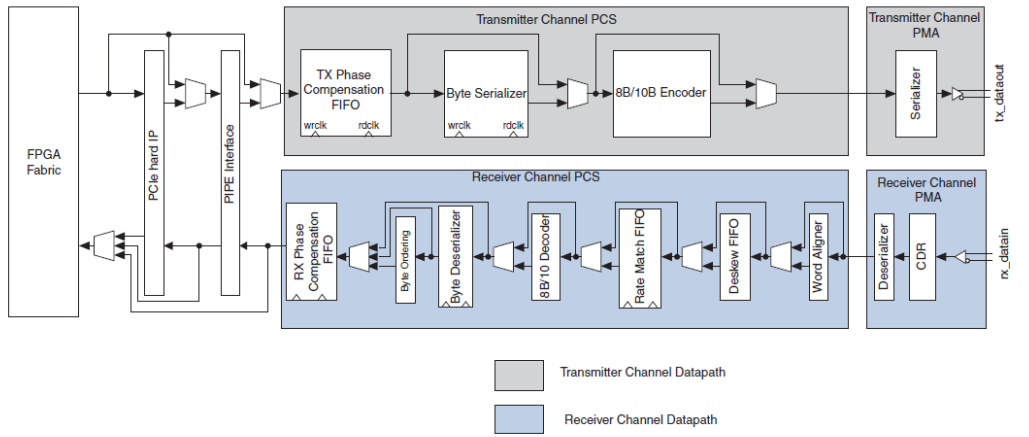
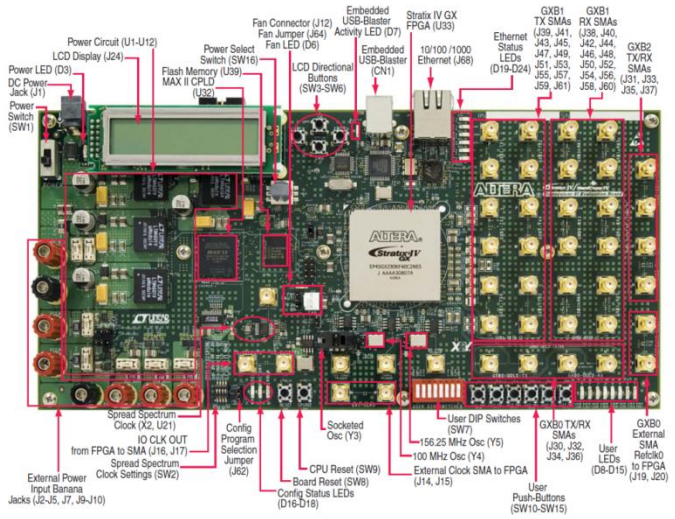
25-Gb/s Optical Transceiver System

- 4-channel BIST system using FPGA Transceiver Evaluation Kit
  - ❖ FPGA has a maximum 8.5Gbps speed Transceivers

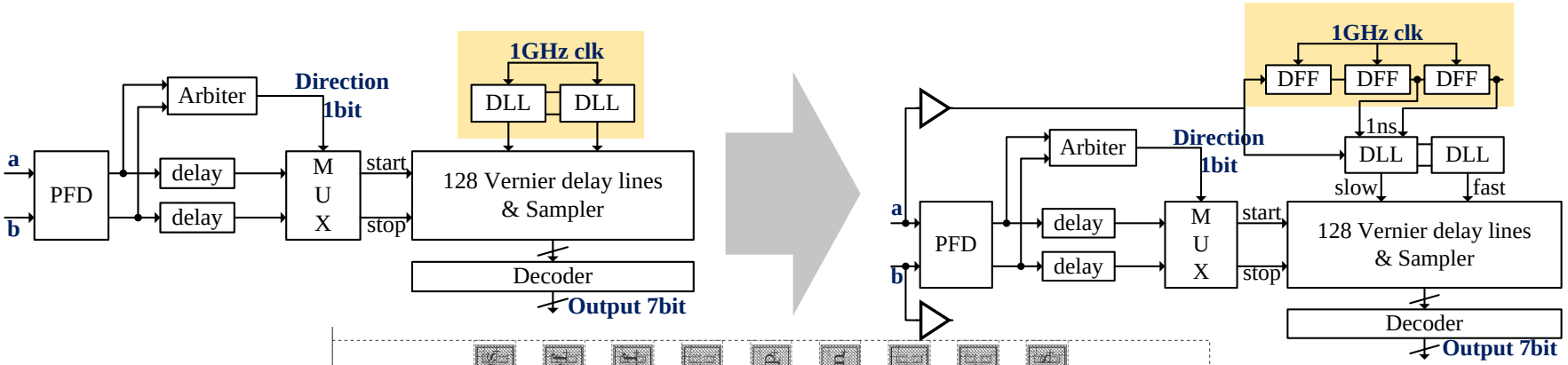
1. Design a **Transceiver block**
   - Using Quartus II to design 4 channel transceiver blocks (6.25Gbps x 4 = 25Gbps)
   - For 6.25Gbps, we should use 32:1 SerDes system.
2. Design a **Pattern Generator**
   - PRBS7,15,31 pattern generator and high-speed clock(10101010…)
   - Error injection function
3. Design a **Bit Error Checker**
   - Applying Error checker function
   - Error count summation

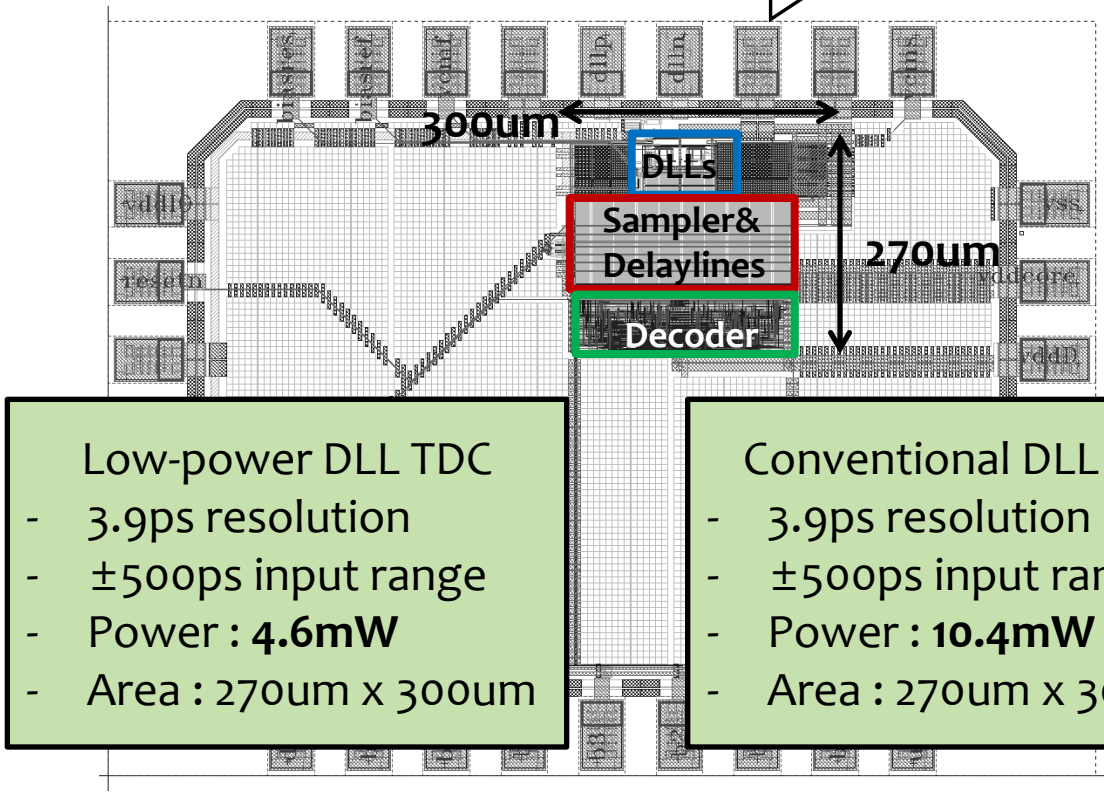
Figure 1–12. Stratix IV GX and GT Transceiver Datapath





Low-power TDC design





Low-power DLL TDC
- 3.9ps resolution
- ±500ps input range
- Power : **4.6mW**
- Area : 270um x 300um

Conventional DLL TDC
- 3.9ps resolution
- ±500ps input range
- Power : **10.4mW**
- Area : 270um x 300um