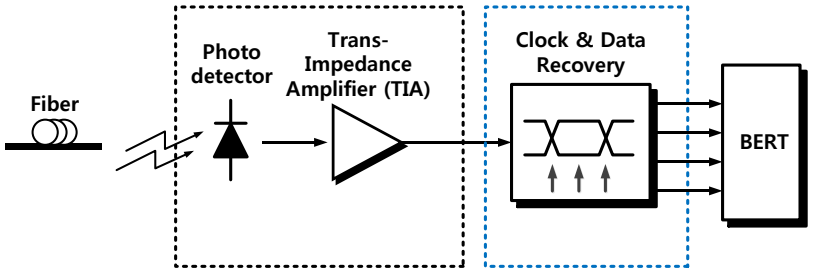
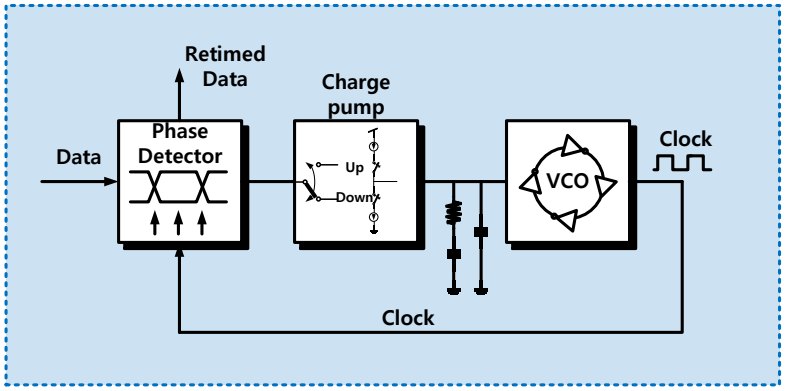
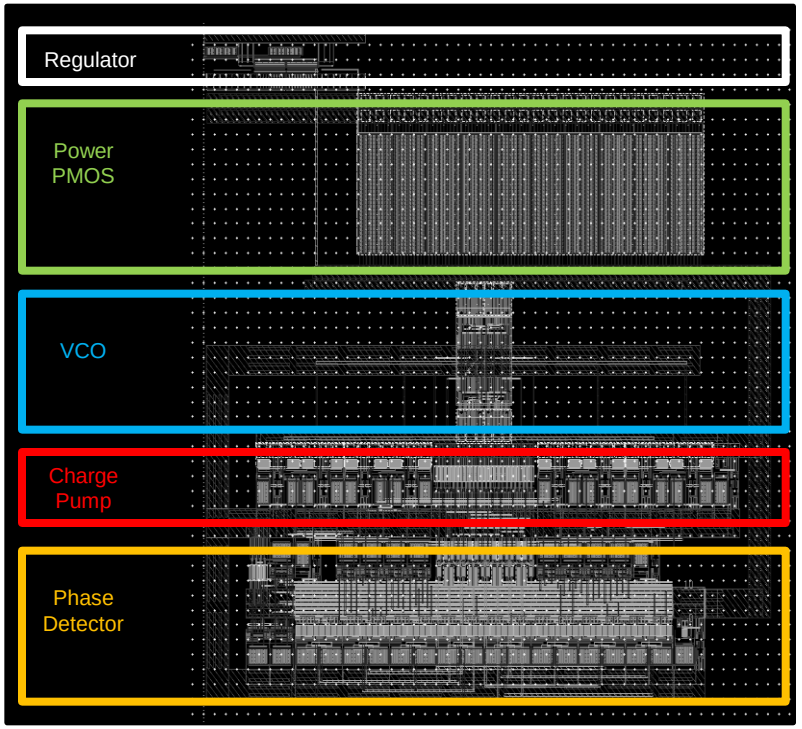
Designing high speed CDR for Optical Rx







- Noisy and Asynchronous data ➔ Clear & Synchronous data
- 20Gb/s quarter-rate CDR for optical Rx.
  - Inductorless
  - High input sensitivity
  - Clock align
  - Deserializer
  - Ideal modeling of CDR

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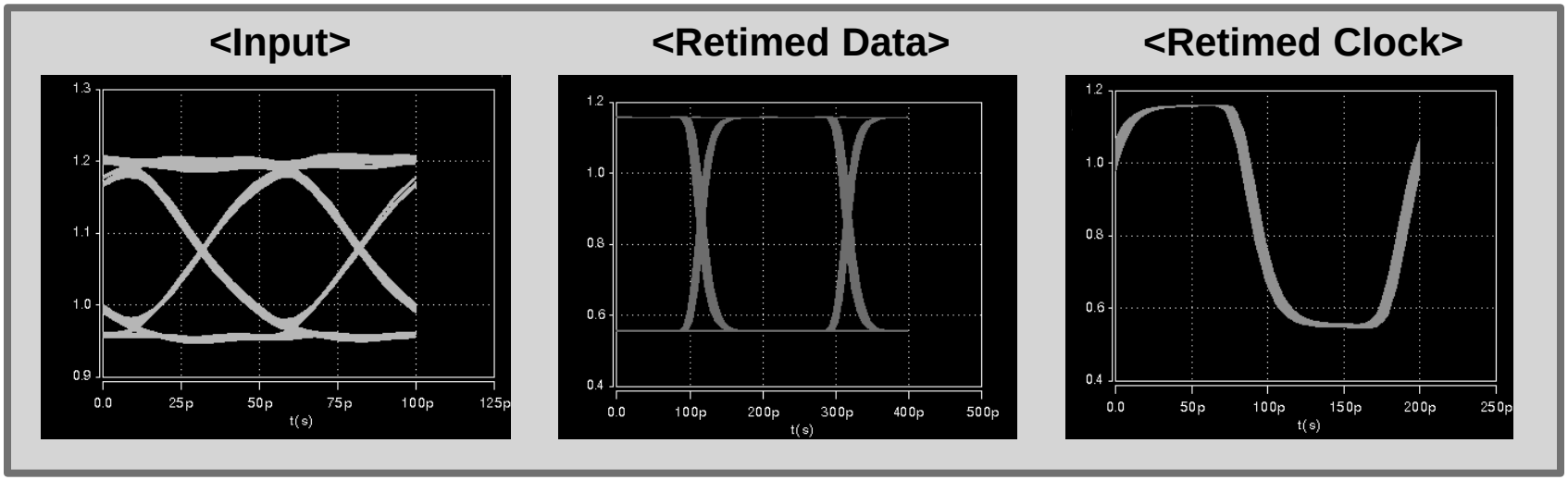
- Post-layout simulation



  - 20Gb/s CDR → Retimed Data & Clock
  - FF, NN, SS corner

- Future Work
  - 20Gb/s Board design
  - Monitoring circuit for sensing & reacting → Clock phase align
  - PLL based dual loop CDR
  - CDR with FD