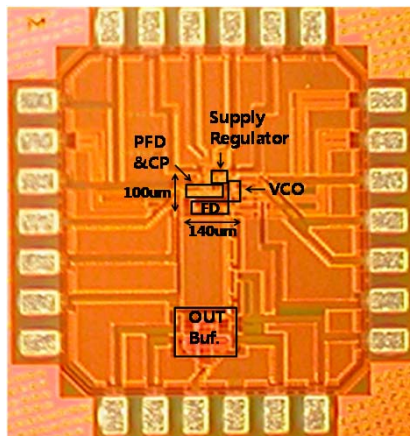


Ultra-Low Voltage Phase-Locked Loops

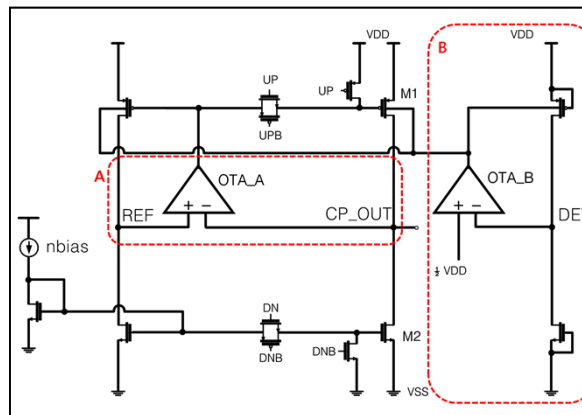
- Why ultra-low voltage?
 - Low power consumption
 - Enhance Power efficiency

Chip Photograph

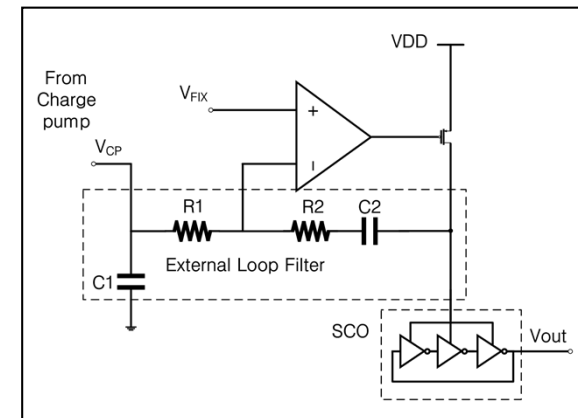


Samsung 130nm tech.

Spur-free CP structure



SRALF VCO structure

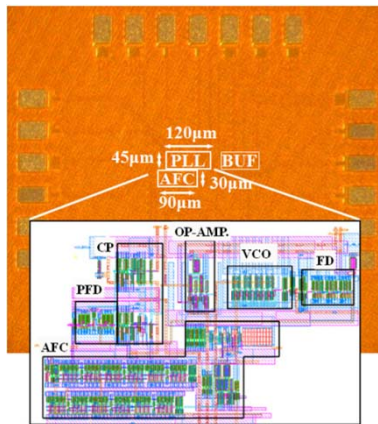


- Result :
ISOCC 2013 "A spur free 0.4-V 88-uW 200-MHz phase-locked loop "

Ultra-Low Voltage Phase-Locked Loops

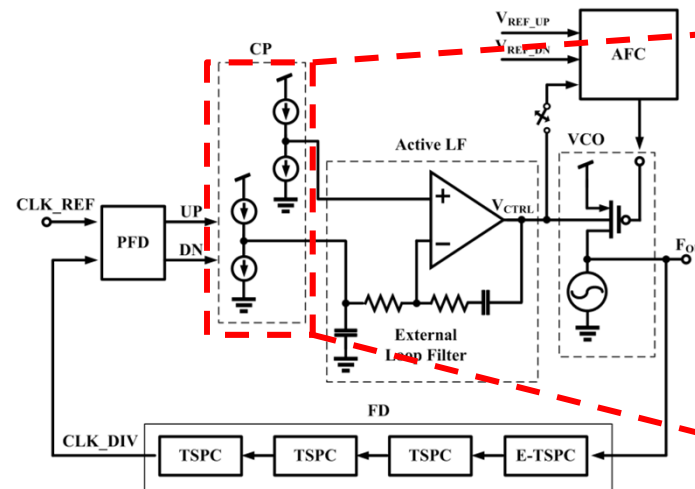
- **ULV PLL with enhanced power efficiency**
 - 0.31 mW/GHz of record low power efficiency
 - Mismatch compensation with an active loop-filter charge pump
 - Low power AFC (automatic frequency calibration) is implemented

Chip Photograph

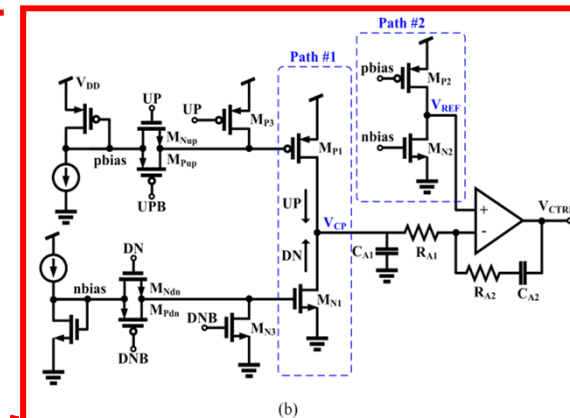


Samsung 65nm tech.

PLL architecture



ULV CP w/ matched char.



- **Result :**
TCAS2 "A 0.4-V 90~350-MHz PLL with an active loop-filter charge pump"