40 nm/40 nm 3D-Stacked SPAD Pixels With Sub-10 μm Pitch and 2 ns Dead Time

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***Abstract*—We present a comprehensive comparative study of passive quenching active recharge (PQAR) and active quenching active recharge (AQAR) analog front-ends (AFEs) designed for 64 × 64 pixel arrays of single-photon avalanche diode (SPAD) pixels. These AFEs were fabricated using a back-side illuminated (BSI) 3D-stacked 40 nm/40 nm CMOS image sensor process. While configured as an array, initial verification was conducted at the pixel level, comparing both AFE types. To enable a truly fair and direct performance evaluation, which was often difficult in prior independent studies due to the use of different devices, processes, architectures, or assumptions, both AFE types were fabricated under identical process, wafer, and layout conditions on the same die. The SPADs exhibit a breakdown voltage of 22.5 V, a low dark count rate (5.1 cps/μm^2 at 2 V excess voltage), and a high photon detection probability (25.1% at 850 nm at 2 V excess voltage). The AQAR pixel occupies a larger area (88.56 μm^2) compared to the PQAR pixel (55.75 μm^2), reflecting an area-performance trade-off. We analyzed methodologies for defining SPAD dead time, adopting inter-arrival time histogram analysis under intensive light. Experimental results demonstrate precise dead time control for both AFEs, achieving a minimum dead time of 2 ns and confirming maximum count rates up to near 500 Mcps. Moreover, this study experimentally verifies the effectiveness of active quenching in afterpulse suppression, leading to reduced noise and consequently contributing to an improved signal-to-noise ratio. The results of this study provide useful information on the design trade-offs and performance of PQAR and AQAR AFEs for various high-performance single-photon detection applications.**

***Index Terms*—3D photonics, 3D-stacked integration, active quenching active recharge (AQAR), afterpulse, analog front-end (AFE), back-side illumination (BSI), CMOS, dead time, light detection and ranging (LiDAR), maximum count rate, passive quenching active recharge (PQAR), photon-counting image sensor (PCIS), pixel, single-photon avalanche diode (SPAD).**

I. Introduction

SINGLE-PHOTON avalanche diodes (SPADs) have become essential in a wide range of imaging applications requiring high sensitivity and/or temporal resolution, such as photon-counting image sensors (PCIS) and light detection and ranging (LiDAR) systems [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44]. These devices have benefited from advances in CMOS technology [45], which enables scalable and low-cost fabrication, leading to their broad adoption across multiple domains.

LiDAR systems, which are widely used in autonomous vehicles, robotics, and augmented reality, prioritize fast and accurate depth sensing. In these systems, performance metrics such as temporal resolution and count rate linearity are more critical than pixel density. Accordingly, most SPAD-based LiDAR sensors adopt relatively large pixel pitches and show little trend toward miniaturization. In contrast, PCIS applications such as low-light-level imaging, biomedical imaging, quantum optics, and time-resolved spectroscopy require both high sensitivity and fine spatial resolution. These systems have aggressively scaled pixel pitches to improve resolution and integration density. This contrasting design trend between LiDAR and PCIS is clearly reflected in Fig. 1, which presents the pixel pitch trends of SPAD-based sensors from 2013 to 2025. While PCIS shows a steady decrease in pixel pitch, reaching sub-10 μm in recent years, LiDAR sensors maintain relatively large pixels.

The increasing circuit complexity poses significant challenges for PCIS systems aiming to scale toward smaller pixel pitches. In conventional 2D integration, shrinking pixel pitches leave little area for advanced analog front-end (AFE) circuits, while also worsening routing complexity, fill factor, and signal integrity. These constraints make further miniaturization increasingly difficult. To address these challenges, 3D-stacked integration has emerged as a key architectural solution. Using hybrid Cu-Cu bonding, SPAD arrays and AFE circuits can be fabricated on

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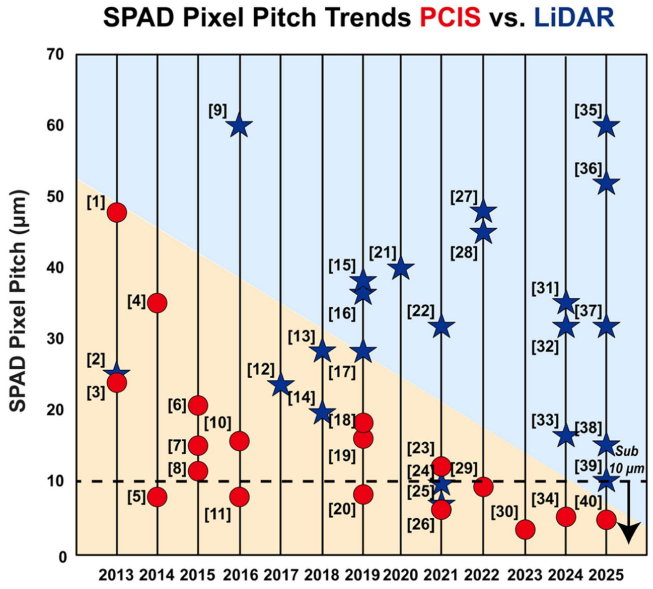

Fig. 1. Comparison of pixel-pitch scaling trends in SPAD-based PCIS and LiDAR sensors.

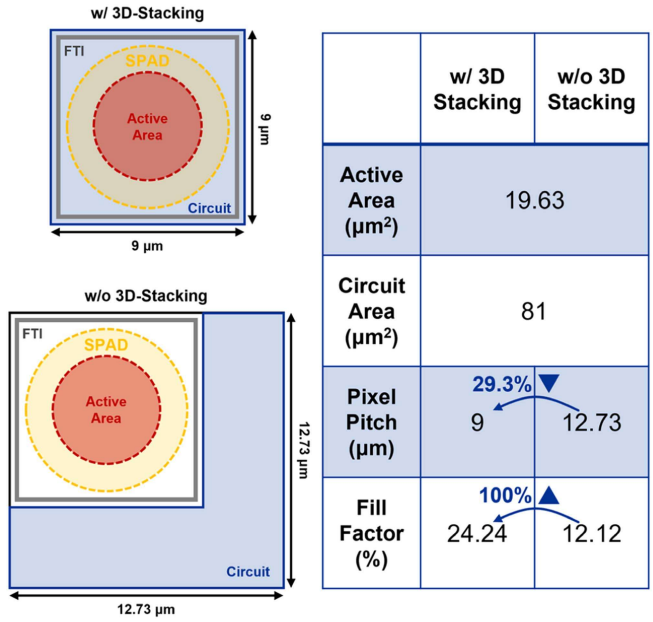

Fig. 2. Conceptual comparison of SPAD pixels with and without 3D-stacked integration.

separate silicon tiers and vertically integrated. This decouples pixel design from circuit complexity, enabling the implementation of advanced readout architectures without compromising pixel density [46].

Fig. 2 illustrates the fundamental advantage of 3D-stacked integration in terms of pixel pitch and fill factor, with fixed SPAD active area. Assuming a SPAD active area diameter of 5 μm, the resulting active area is identical (19.63 μm^2) regardless of whether 3D-stacking is employed when a full trench isolation (FTI) is implemented. When 3D-stacked integration is adopted, the SPAD and its associated readout circuit are placed on separate tiers, allowing the circuit area to be allocated independently beneath the SPAD area. In this case, the circuit occupies an area of 81 μm^2, resulting in a pixel pitch of 9 μm and a fill factor of 24.24% . In contrast, without 3D-stacking, the same SPAD active area and circuit area must be designed within a single tier. This constraint increases the required pixel pitch to approximately 12.73 μm, reducing the fill factor to 12.12% . As a result, the adoption of 3D-stacked integration enables a 29.3% reduction in pixel pitch while achieving a 100% increase in fill factor, clearly demonstrating its effectiveness as a key enabler for pixel miniaturization.

This architectural flexibility facilitates the integration of diverse AFE designs optimized for different applications: passive quenching passive recharge (PQPR), passive quenching active recharge (PQAR), and active quenching active recharge (AQAR). These architectures offer different trade-offs in complexity, area, and timing characteristics. Among them, active recharge approaches, i.e., PQAR and AQAR, have become increasingly important for reducing SPAD dead time and improving the maximum count rate (MCR) [47], which is essential for high-speed and high-illumination environments. The PQAR circuits utilize passive quenching with fast active recharge, which offers a relatively compact design with sufficient speed, making it suitable for PCIS applications where minimizing pixel area is a priority [33], [38], [44]. AQAR circuits, on the other hand, actively control both quenching and recharge phases, enabling better timing resolution and higher count rate linearity with minimal afterpulsing probability (APP) [48]. Although it consumes more area, the performance benefits make AQAR well-suited for LiDAR systems, where performance is prioritized over compactness. Time-gated circuits can be also regarded as a type of AQAR, where photon detection is enabled only within a clock-defined gate window to suppress background photons under high ambient illumination. While time-gated architectures enable compact pixel implementations and are highly effective in high-flux conditions, their clock-driven operation may lead to reduced power efficiency in low-flux conditions and increased sensitivity to clock skew [38].

Despite the widespread use of PQAR and AQAR across various applications, few studies have directly compared them under matched fabrication and layout conditions. Most prior works evaluate these circuits independently, using different processes, pixel architectures, or assumptions, making it difficult to fairly assess their architectural trade-offs. In this paper, we present a comprehensive comparative study of PQAR and AQAR circuits implemented in a 3D-stacked 40 nm/40 nm back-side illuminated (BSI) CMOS image sensor (CIS) technology. Both AFEs were designed with identical pixel layouts and fabricated in adjacent regions of the same die, ensuring that any differences in performance stem solely from the AFE architecture. The unified design and fabrication approach enables a fair and quantitative comparison of key performance metrics such as DCR, dead time, and APP. The insights obtained from this work provide practical design guidance for selecting the most suitable AFE architecture based on application-specific constraints such as pixel pitch.

II. BACK-SIDE ILLUMINATED 3D-STACKED SPAD PIXELS

This section presents the design and performance of the SPAD pixels developed in this work, particularly focusing on the two different AFE architectures vertically integrated with their SPADs. Unlike many prior studies, which often suffer from inconsistent fabrication conditions, SPAD pixels discussed in this work were fabricated on the same wafer using a matched 40 nm/40 nm BSI 3D-stacked process. Both AFE types share an identical SPAD layout, including junction and guard-ring structure, pixel dimensions, and back-end-of-line (BEOL) configuration, thereby eliminating non-architectural sources of performance variation. For direct evaluation of the impact of active quenching, both PQAR and AQAR AFE types are designed.

A. AFE Circuits

3D-stacked integration offers significant flexibility in SPAD AFE design. Fundamentally, AFEs are categorized by how they combine passive and active methods for quenching and recharge, resulting in configurations like PQPR, PQAR, and AQAR. Since most designs converge into these operating principles regardless of schematic variations, understanding the evolution from basic PQPR to advanced AQAR is essential for interpreting the comparative analysis presented in this paper.

The evolution of AFE architectures begins with the fundamental PQPR structure. In this configuration, both quenching and recharge operations rely on a resistive element, typically implemented using a MOSFET biased to operate as a resistor connected to the SPAD anode. Upon photon detection, the avalanche current creates a voltage drop across this transistor, passively quenching the SPAD. Subsequently, the anode potential recovers via passive recharge determined by the resistance of the MOSFET and stray capacitance. While PQPR offers distinct advantages in terms of circuit simplicity and compact area, it suffers from a critical trade-off between stability and speed. A large resistance is required to ensure reliable quenching, but this results in a prolonged RC recharge time, which severely limits the MCR. Conversely, reducing the resistance to shorten the dead time increases the risk of incomplete quenching. Furthermore, the slow, unregulated recharge phase leaves the SPAD vulnerable to re-triggering by afterpulses, leading to irregular output pulse widths.

To address the limitations of PQPR, active recharge is introduced. Instead of relying on the slow passive recharge, this configuration utilizes a delay cell to trigger a rapid recharge path after a predetermined time delay (T_{Delay}) following the quench event. This ensures a short and well-defined dead time (T_{Dead}), regardless of the quenching resistance value. Consequently, a high quenching resistance can be used for stability without compromising the count rate. However, PQAR presents a new drawback. While the prolonged dead time of PQPR naturally masked early-occurring afterpulses, the shortened dead time of PQAR exposes them. This increased detection of afterpulses leads to higher pixel noise, negatively impacting the signal-to-noise ratio (SNR) and dynamic range (DR).

To suppress these afterpulses, active quenching is implemented. The primary motivation for using active quenching lies in its effective afterpulse suppression, realized by implementing control mechanism optimized for the recharge phases. In PQAR, a passive recharge mechanism is active between the end of quenching and the activation of active recharge. During this period, the excess voltage across the SPAD gradually rises, creating a window for re-triggering. Active quenching resolves this by providing a hold-off time (T_{Hold}) to prevent the SPAD from exceeding its breakdown voltage until the active recharge process is initiated. Ultimately, the AQAR AFE integrates several useful functions. While it incurs a larger area overhead compared to PQAR structures, its advantages are significant: stable operation, reduced noise due to afterpulse suppression (leading to increased SNR), and the realization of a short, well-defined dead time, which significantly increases the MCR and, consequently, improves the DR.

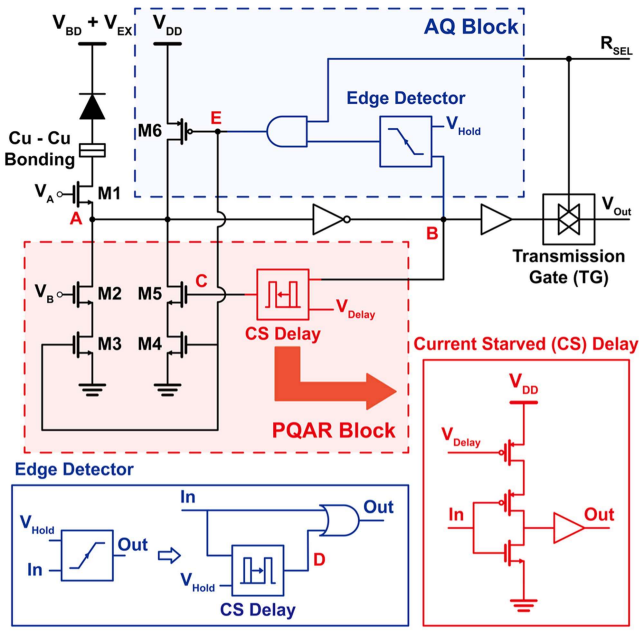

Fig. 3. Schematic of the designed AQAR AFE circuit. The design integrates the PQAR block (red dashed box) and the AQ block (blue dashed box) with the SPAD device. Detailed schematics for the CS delay and edge detector are shown in the bottom insets.

To experimentally analyze and compare the PQAR and AQAR architectures, we designed and fabricated both AFE types, with their detailed schematics presented in Fig. 3. As illustrated, the AQAR circuit integrates both the PQAR block (highlighted by the red dashed line) and the AQ block (highlighted by the blue dashed line). In contrast, the PQAR circuit is implemented without the AQ block, while all other circuit components remain identical to ensure a consistent comparison. In the PQAR circuit, the gates of transistors M3 and M4 are connected to the row select signal (R_{SEL}), enabling pixel selection control.

The operation of the PQAR block relies on the fundamental quenching and recharge mechanisms. The M2 operates in the linear region, functioning as a tunable quenching resistor controlled by the gate voltage (V_B). Specifically, V_B is adjusted to set a sufficiently high resistance value, which is essential for ensuring stable quenching. Upon photon detection, the avalanche

current flows through M2, inducing a voltage drop that passively quenches the SPAD. Subsequently, the active recharge loop is activated. In this configuration, the delay element is implemented using a current-starved (CS) inverter topology. By increasing the control voltage (V_{Delay}), the driving current is modulated to extend the output rise time of the CS delay inverter, thereby generating the desired delay (approximately 260 ps-150 ns). This mechanism enables the tunability of the reset timing, ensuring a short and well-defined dead time (T_{Dead}) down to about 600 ps in simulation.

In the AQAR configuration, the additional AQ block enables active quenching and a tunable hold-off capability. While the quenching process is primarily initiated by the passive resistor M2, the active loop serves to latch the quenched state. Specifically, the sensing inverter (0.46 V threshold) detects the rising edge of node A and activates M6 with a propagation delay of approximately 130 ps, forcibly pulling node A to VDD. Furthermore, the hold-off control is implemented by the edge detector circuit incorporating the CS delay cell. By adjusting the control voltage (V_{Hold}), the internal delay is modulated to define the hold-off time (T_{Hold}), maintaining the SPAD in a quenched state for this duration. This ensures that the SPAD remains quenched during the high probability window of carrier detrapping. Consequently, it effectively masks afterpulses and significantly improves signal reliability.

Our designed AFEs implement several advanced techniques to achieve further advantages. First, all transistors within the pixel are designed using 1.1 V low voltage transistors. This offers significant area benefits while implementing numerous features and simplifies the layout by requiring only a single power line. Second, the implementation of a cascode structure (M1) allows for an available excess voltage approximately double the driving voltage of the transistors, thereby enhancing photon detection efficiency of the SPAD pixel.

These AFEs are optimized considering various scenarios as illustrated in Fig. 4. First, for normal operation (Case 1), the dead time can be controlled via the T_{Delay} setting. Second, in instances of photon arrival within the dead time (Case 3), the T_{Hold} control ensures a sufficient hold-off time to effectively mask afterpulses, thereby preventing premature re-triggering during the recharge phase. Third, our design effectively handles photon arrival during active recharge (Case 2), even when a low-resistance current-sink path is formed. This is achieved by ensuring sufficient current driving capability from M4 and M5, and by designing the delay cell asymmetrically to minimize the active recharge duration to approximately 300-500 ps. This is crucial to reduce the probability of photon arrival during the active recharge phase, since avalanche quenching cannot occur because the resistance of the active recharge path is too low to induce the necessary voltage drop. By minimizing this duration, the design effectively narrows the time window where such signal conflicts could occur. Finally, for SPAD deactivation (Case 4), the SPAD can be turned off by controlling R_{SEL}. This feature is highly valuable for array applications, as it allows pixels to be selectively turned off during unnecessary periods, improving device reliability and reducing power consumption.

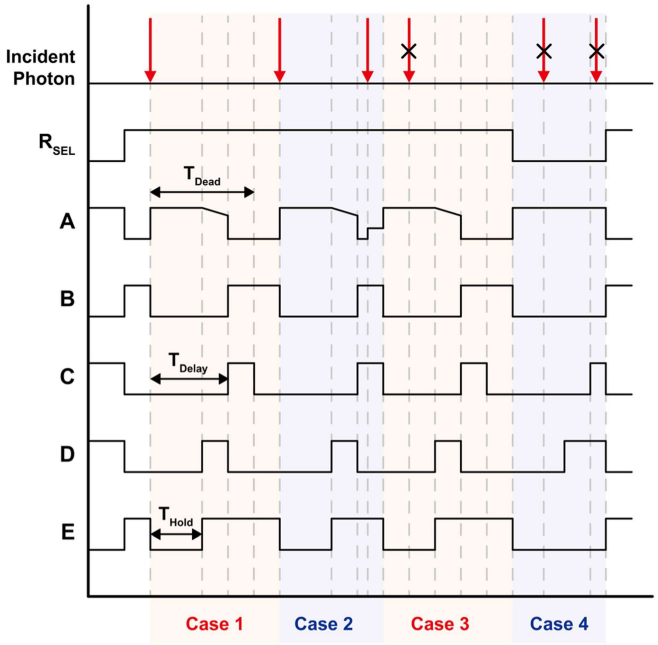

Fig. 4. Timing diagram depicting the behavior of the AQAR for four different photon arrival scenarios.

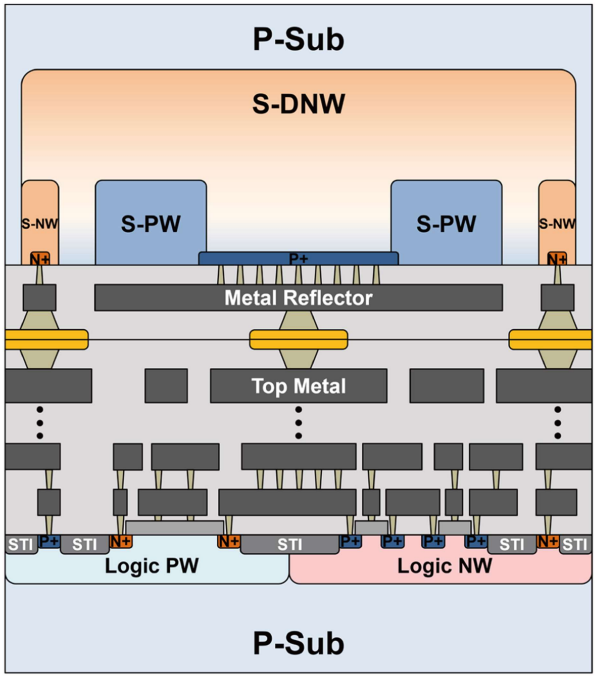

Fig. 5. Cross-section of the 3D-stacked SPAD structure.

B. SPAD Device Structure and Pixel Array Architecture

Fig. 5 illustrates the SPAD structure with the integrated circuits. As shown in Fig. 5, the SPAD is fabricated using 3D-stacked technology, where the SPAD is designed on the top tier and vertically integrated with the AFE circuit on the bottom tier through hybrid Cu-Cu bonding. The SPAD has a P+/S-DNW junction with an S-PW guard ring, where S-DNW stands for

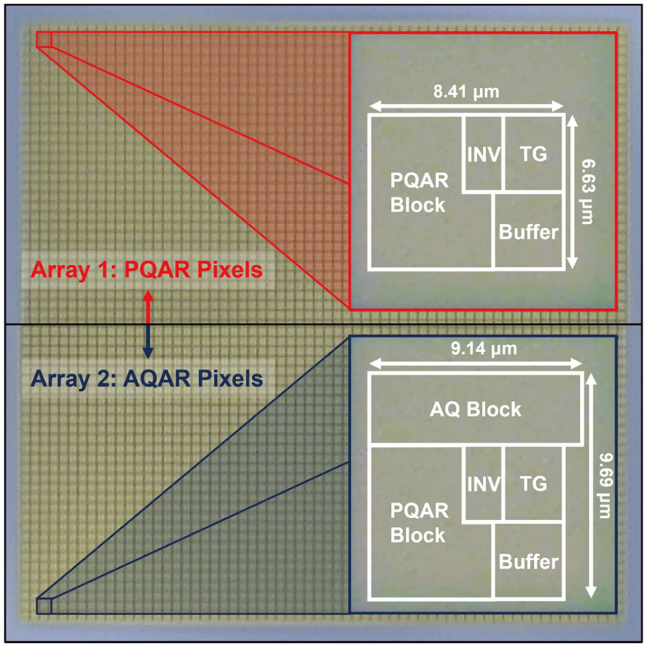

Fig. 6. Chip micrograph: PQAR 64×64 pixel array (top half) and AQAR 64×64 pixel array (bottom half).

SPAD Deep N-well and S-PW SPAD P-well, both are optimized for SPAD operation, which effectively prevents premature edge breakdown and ensures a uniform multiplication region. Fig. 6 shows the micrograph of the fabricated 3D-stacked chip. The top half corresponds to a portion of the 64 × 64 PQAR pixel array, while the bottom half shows a portion of the 64 × 64 AQAR pixel array. On the right side of the figure, a magnified view of a single pixel contains the block diagram of the designed layout. The PQAR pixel includes a passive quenching (PQ) block, an active recharge (AR) block, and signal processing logic. The AQAR pixel, in contrast, contains both active quenching (AQ) and AR blocks, along with an identical signal processing logic.

Due to the extra circuitry required for active quenching, the AQAR pixel occupies a larger area of 88.56 μm^2 compared to 55.75 μm^2 for the PQAR pixel. Although their pixel pitches are similar, 8.41 μm for PQAR and 9.69 μm for AQAR, the difference becomes critical when considering future integration of additional functions such as on-pixel counters. In this context, the PQAR architecture offers sufficient margin for further integration within a 10 μm pitch, making it more suitable for PCIS applications where pixel miniaturization is a key requirement. In contrast, the AQAR pixel, while larger, provides better performance, which is more desirable in LiDAR applications where performance is prioritized over pixel area. Furthermore, implementing more advanced CMOS technology nodes for AFE circuit could enable further reduction in the circuit area, which would allow even tighter pixel pitches.

III. Experimental Results

This chapter presents the measurement results of the fabricated 3D-stacked IC. First, the performance of the SPAD devices designed on the top wafer is evaluated to verify correct operation. Subsequently, the focus shifts to the AFEs implemented on the bottom wafer. These AFE measurements aim to enable a direct and fair comparison between the PQAR and AQAR architectures. Although these architectures form the respective arrays, the measurements were performed on standalone test pixels utilizing identical SPADs sized for the AQAR pixel. The measurements were conducted using a LeCroy WavePro 735Zi oscilloscope and a 4GHz active probe (ZS4000). The evaluation was performed in three stages. First, measurements were conducted to verify if each AFE operates as intended. Subsequently, measurements were performed to derive the MCR corresponding to the measured dead time. Finally, APP measurements were conducted to confirm whether active quenching is indeed effective in suppressing afterpulses. All AFE measurements were conducted at $V_{EX} = 2$ V.

A. SPAD Device Performance

The current-voltage (I-V) characteristics under both dark and illuminated conditions are shown in Fig. 7(a). The breakdown voltage is measured to be 22.5 V, and the dark current remains below 10 pA, indicating low leakage current. An abrupt increase in avalanche current at the breakdown voltage confirms proper avalanche multiplication. To empirically verify the uniformity of the multiplication region, the light emission test (LET) result is also presented in Fig. 7(a). The observed uniform light emission across the active area experimentally confirms that the electric field is uniformly distributed, demonstrating that premature edge breakdown is effectively suppressed. Fig. 7(b) illustrates the dark count rate (DCR) performance measured up to an excess voltage of 2 V, corresponding to the AFE's operating conditions. At this bias, the DCR is 100 cps, and the normalized DCR is 5.1 cps/μm^2, demonstrating low-noise operation. Fig. 7(c) shows the photon detection probability (PDP) across various wavelengths. Thanks to the BSI structure, the depletion region is formed deeper in the substrate, enhancing sensitivity at longer wavelengths. At the excess voltage of 2 V, the peak PDP reaches 32.4% at 750 nm. Notably, high PDP values of 19.5% at 900 nm and 17.3% at 950 nm are achieved, which are particularly beneficial for both PCIS and LiDAR applications. Considering the 3D-stacked configuration, where an optimized microlens can enable an effective fill factor approaching 100% , the effective photon detection efficiency (PDE) is also expected to be comparable to the measured PDP values.

B. Dead Time

The commonly used definition of dead time is the period during which a SPAD is unable to detect incoming photons. However, beyond a conceptual understanding, it is necessary to consider how dead time should be defined and measured in actual systems when integrated with an AFE, to obtain a value close to the actual dead time.

One approach defines dead time based on the output pulse width. However, this fixed-value output pulse, just signaling an event, often fails to accurately reflect the full unresponsive period of the SPAD and its internal recovery times; thus, the

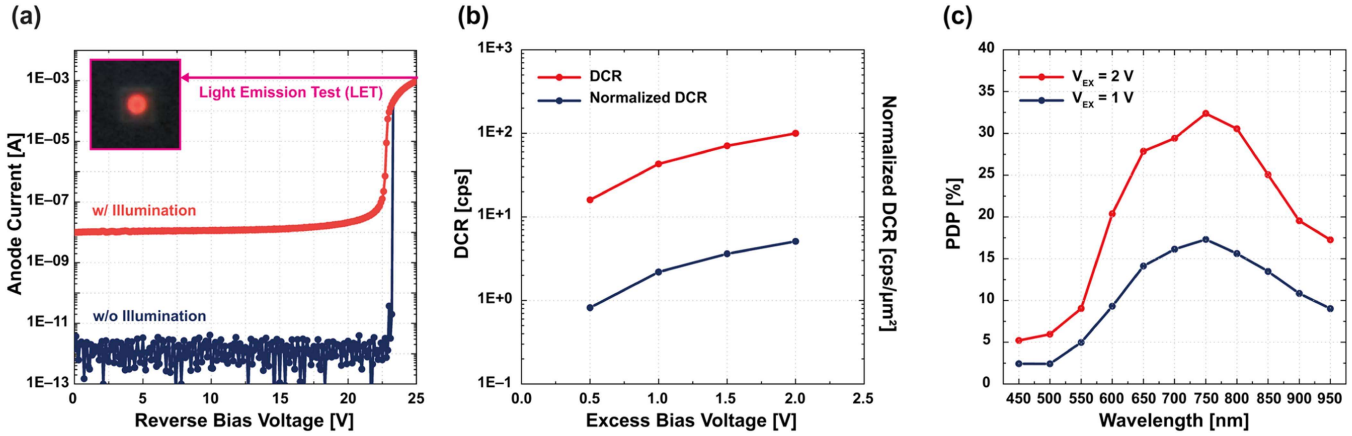

Fig. 7. (a) I-V, (b) DCR, and (c) PDP characteristics of the SPAD.

actual dead time of the system can be longer. This pulse width is also inconsistent, exhibiting larger standard deviations of output pulse width for noisier devices, affecting the reliability of the measured value. Furthermore, for active recharge systems (refer to Fig. 4), defining dead time just by output pulse width is challenged by the need to include the duration of the active recharge trigger signal, revealing inaccuracies from internal AFE processing.

The second perspective defines dead time as the minimum interval time between output pulses, a widely adopted and accurate method. However, accurately identifying dead time from an inter-arrival time (IAT) histogram can be challenging at very low count rates, as it becomes susceptible to statistical noise. This requires us to consider two distinct cases based on the light intensity condition. Under intensive light, the sharp rising edge at the minimum interval of the IAT histogram accurately defines dead time. In contrast, under low light, with very few photons, it is hard to reliably accumulate IAT histograms, though IAT can still indicate dead time. Pulse width may offer an approximate value. Therefore, the IAT-based dead time definition is most suitable for intensive light, whereas for low light, output pulse width may offer an approximate value (though not perfectly accurate). Based on this, we adopted the most reliable method, utilizing the IAT histogram under highly intensive light conditions. Specifically, to exclude noise-induced outliers, we defined the dead time as the minimum time bin where the accumulated count reaches 50% of the histogram's maximum peak. This threshold (essentially the leading edge of the FWHM) ensures data reliability by filtering out low-count noise while capturing the effective recovery time, rather than the peak arrival time. The validity of this approach is confirmed by our experimental observation. While the output pulse width (FWHM) indicated approximately 1.7 ns, the IAT-based dead time was determined to be 2 ns. This discrepancy caused by the active recharge window closing after the pulse output demonstrates that relying solely on pulse width leads to an underestimation of the true dead time.

Fig. 8(a) presents the measured IAT histogram under intensive light condition. The graph exhibits a steep slope characteristic of high photon flux, rising sharply as it approaches the dead time

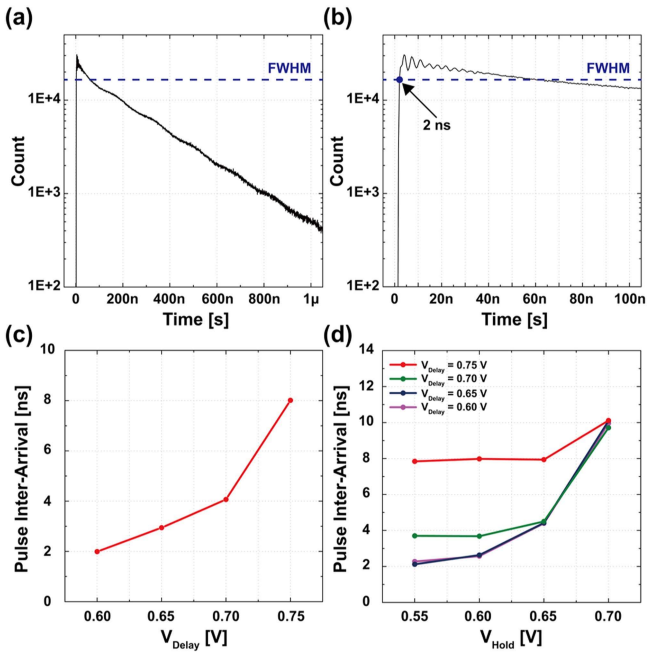

Fig. 8. (a) Measured IAT histogram result of the AQAR under intensive light conditions and (b) zoom-in view of the rising edge. (c) Variation of IAT with V_{Delay} in PQAR. (d) Variation of IAT with V_{Hold} at various V_{Delay} in AQAR.

limit. Fig. 8(b) provides a zoom-in view of the sub-100 ns region from Fig. 8(a). Here, the dead time is determined at the rising edge where the count exceeds 50% of the peak value, verifying our extraction method. Following this characterization, Fig. 8(c) and (d) present experimental verification of dead time control and proper operation. For the PQAR AFE (Fig. 8(c)), V_{Delay} adjustment controls active recharge trigger timing, confirming that the measured minimum IAT increases with longer delay, which indicates the extension of the dead time, thus verifying the proper operation. Similarly, Fig. 8(d) verifies the proper operation of the AQAR AFE. V_{Hold} control adjusts hold-off time, and as design prevents recharge during activation of hold-off, the minimum IAT changes accordingly even with a fast active recharge trigger if a longer hold-off time is set. Consequently,

the designed PQAR and AQAR AFEs exhibit a minimum dead time of 2 ns. Although data extraction was performed only up to a dead time of approximately 10 ns, the dead time can be extended to over 100 ns. However, we optimized the V_{Delay} operating range based on practical application requirements and measurement constraints. First, since dead times exceeding 10 ns are generally not preferred for our target applications, the focus was placed on the sub-10 ns regime. Second, verifying extremely short dead times presents challenges in the current setup. In the absence of an integrated counter, the characterization relies on driving the output pulse off-chip via I/O pads. This configuration inevitably introduces bandwidth limitations due to parasitic load. Therefore, the V_{Delay} range was adjusted to ensure reliable external measurement, while the design supports a minimum dead time of 600 ps in simulation.

C. MCR

MCR practically signifies the maximum detection capability of a SPAD AFE, and it is directly related to dead time. Photons cannot be detected within the dead time but can be counted thereafter. This implies that if triggers occur at the maximum frequency corresponding to the dead time, that would be the moment of maximum counting. Therefore, the maximum value obtained from the MCR measurement should be the same as the dead time measured through the IAT histogram. Consequently, MCR measurement was performed to confirm the correctness of the dead time values obtained from previous dead time measurements.

For the experiment, a PicoQuant PDL-800D laser driver and an LDH-D-C-670 laser head were used to align a continuous laser to the pixel, and light power was adjusted via the intensity control function of the laser driver. Fig. 9 shows the count rate measurement results based on the available laser power range with the equipment used. Regardless of AFE type, at an 8 ns dead time, saturation occurs near the theoretical maximum of 125 Mcps, and the count rate decreases with stronger incident light. This phenomenon is caused by pile-up, where photons continuously trigger the SPAD even before its recharge is fully complete due to excessively strong light. As light intensity increases, this phenomenon worsens, eventually causing the output voltage baseline of the AFE to become fixed, leading to a rapid decrease in counting. In contrast, operating with a dead time around 2 ns, counts can reach their theoretical maximum, which is typically around 450-500 Mcps. Therefore, the dead time value defined via the IAT histogram is consistent with the dead time value that can be defined through MCR measurement.

D. APP

An afterpulse occurs when a charge generated by an avalanche in a SPAD is captured in a defect within the SPAD. The trapped charge is then released after the initial avalanche process is quenched, re-triggering an avalanche in the high electric field of the SPAD.

The primary objective of this experiment is to demonstrate the effectiveness of the active quenching mechanism in suppressing afterpulses, thereby validating the design strategy discussed in Section II. To ensure a fair and reliable comparison, both PQAR and AQAR AFEs were fabricated by integrating identical SPAD devices on the same die under the same process conditions. Furthermore, since APP is inversely proportional to dead time, we controlled both PQAR and AQAR to operate with identical dead times for the measurement, as shown in Fig. 10.

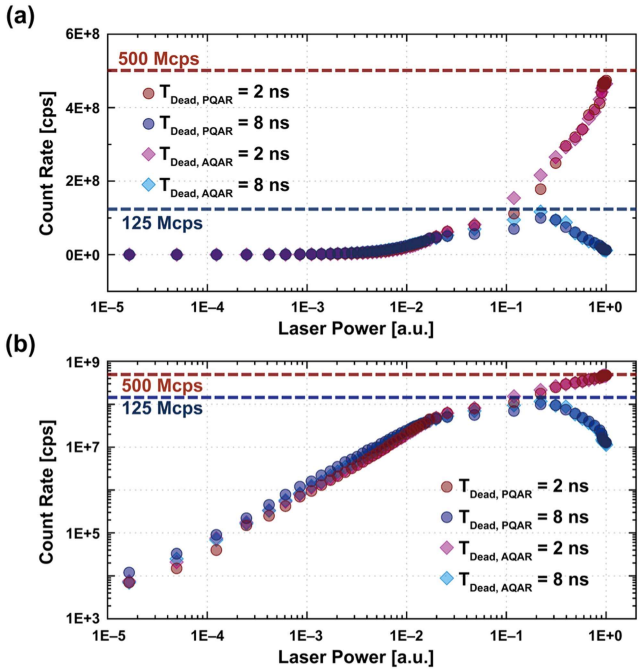

Fig. 9. Measured count rate versus laser power of PQAR and AQAR at 2 ns and 8 ns dead time with $V_{Hold} = 0.55$ V in (a) linear scale and (b) log scale.

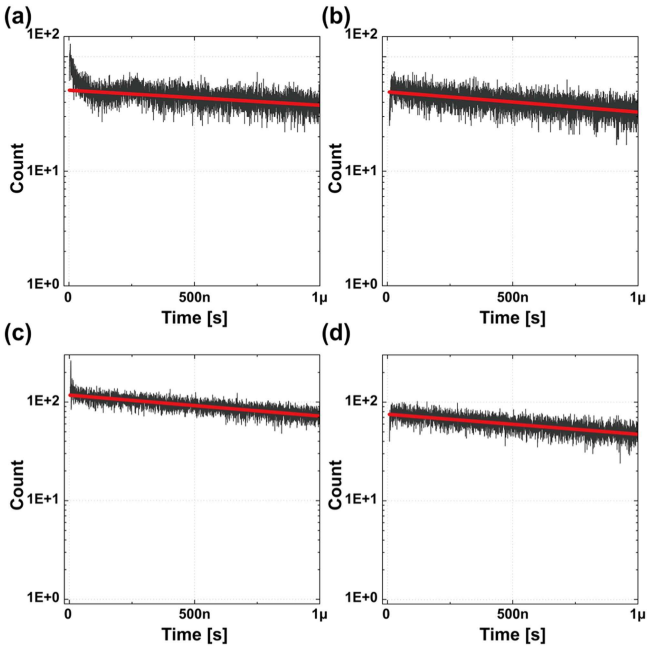

Fig. 10. APP measurement results where the red lines are the ideal fitting lines: (a) 2 ns dead time for PQAR, (b) 8 ns dead time for PQAR, (c) 2 ns dead time for AQAR, and (d) 8 ns dead time for AQAR.

TABLE I
COMPARISON WITH STATE-OF-THE-ART 3D-STACKED SPAD PIXELS FOR PCIS AND LIDAR

Parameters	Unit	This Work				VLSI'23 Takatsuka [34]	ISSCC'22 Ota [32]	IEDM'21 Morimoto [29]	ISSCC'21 Kumagai [27]	IEDM'21 Shimada [49]	JSSC'19 Ximenes [16]
Process	-	**40 nm/40 nm 3D-Stacked**				90 nm/22 nm 3D-Stacked	90 nm/40 nm 3D-Stacked	90 nm/40 nm 3D-Stacked	90 nm/40 nm 3D-Stacked	90 nm/22 nm 3D-Stacked	45 nm/65 nm 3D-Stacked
Application	-	**PCIS / LiDAR**				Photon Counting Image Sensor (PCIS)			Light Detection and Ranging (LiDAR)		
AFE Type	-	**PQAR**		**AQAR**		PQAR	PQAR	N/A	PQPR	PQPR	PQPR
Pixel Pitch	μm	**8.41**[a]		**9.69**[a]		3.36	9.585	6.39	10	6	19.8
V_{BD}	V	**22.5**				19	26.5[e]	30	16.7[f]	22	28.5[g]
V_{EX}	V	**2**				3	2.5	2.5	3.3[f]	3	2.5
PDP @ Wavelength	%	**25.1 @ 850 nm**				26.5[b, c] @ 940 nm	25[b, e] @ 850 nm	32.8[b] @ 850 nm	22[b] @ 905 nm	42[b] @ 850 nm	10[h] @ 850 nm
Normalized DCR	cps/μm²	**5.1**				0.19[d]	0.03[d]	0.044	20.1[d]	0.53[d]	55.4
Dead Time	ns	**2**	**8**	**2**	**8**	6[c]	N/A	N/A	6	6.3	< 2.4
APP	%	**2.9**	**0.2**	**0.6**	**0.1**	< 0.1[c]	N/A	N/A	0.1	< 0.1	2.2

(a) Effective pixel pitch based on AFE pitch (b) PDE value w/ μlens (c) Obtained value from [33] (d) Calculated as DCR divided by pixel area (e) Obtained value from [24] (f) Estimated value from the figures (g) Obtained value from [15] (h) Estimated value from PDP graph

Before introducing the actual measured IAT histogram results in Fig. 10, we will briefly mention the APP measurement method. APP is measured by conducting an IAT histogram under non-intensive or low-light conditions. From the accumulated waveform, a linear fitting line is created. The remaining area value, obtained by subtracting the integral value of the fitting line from the integral value of the actual waveform, is then divided by the integral value of the actual waveform and presented as a percentage, which represents the APP.

Note that the APP value can vary depending on the range of the x-axis (time axis) used in the calculation. This is because while the numerator (the area representing the number of afterpulses, defined as the difference between the integral of the afterpulse waveform and the integral of the fitting line) remains constant, the calculated APP value decreases as the denominator (the time axis range) widens. Given this, when interpreting APP results, it is important to focus on the raw data (waveform) and the trend of APP change with dead time, rather than just on the absolute value of the APP.

Fig. 10(b) and (d) respectively show the APP waveforms when PQAR and AQAR are operated with an 8 ns dead time. These results confirm that they have negligible afterpulse levels. In contrast, Fig. 10(a) and (c) show that when operated with a 2 ns dead time, PQAR visually exhibits a significant accumulation of low IAT values. Conversely, while AQAR shows some accumulation compared to Fig. 10(b) and (d), it remains at a negligible level.

The IAT histogram was performed over a 0-1 μs range with a 200 ps time resolution. The fitting curve used for calculations was set based on data from 0.5-1 μs. The time axis range used for APP calculation encompassed the full measurement range from the dead time up to 1 μs. Fig. 11 visualizes the calculated APP values to identify trends. Specifically, by presenting the pulse IAT in Fig. 11(a) and the APP in Fig. 11(b) with respect to the same control voltage (V_{Delay}), the correlation between APP and dead time is clearly visualized. This allows to intuitively observe that increasing the dead time effectively suppresses the APP. Consequently, the implementation of active quenching was experimentally proven to effectively suppress afterpulses.

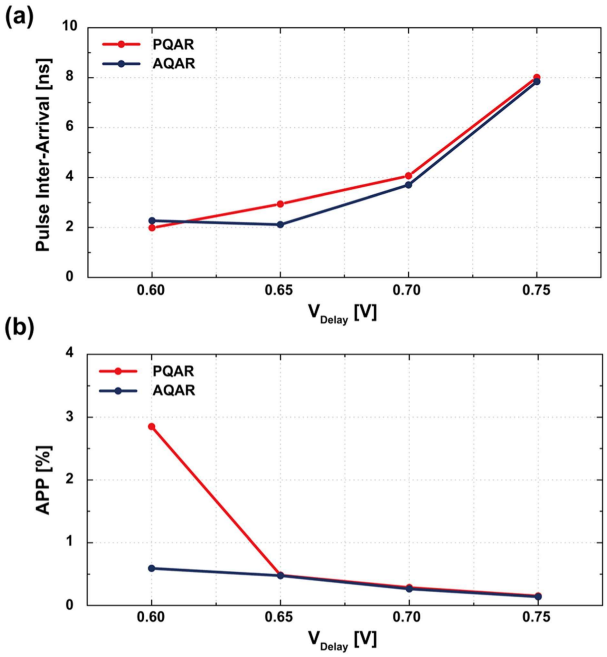

Fig. 11. (a) Comparison of IAT variation and (b) APP with V_{Delay} for PQAR and AQAR at $V_{Hold} = 0.55$ V.

E. Discussion

Table I summarizes and compares the state-of-the-art results utilizing 3D-stacked CMOS processes. While most recent studies commonly adopt passive quenching with active recharge, we chose a more complex active quenching approach to ensure robust afterpulse suppression. The fabricated SPADs achieve a

breakdown voltage of 22.5 V and a DCR of 5.1 cps/μm^2 at 2 V excess voltage, demonstrating low-noise operation. Notably, our design achieves a high PDP despite operating at a remarkably low excess voltage of 2 V. In terms of AFE performance, our design demonstrates highly competitive characteristics. Both architectures achieve a minimum dead time of 2 ns and a MCR reaching nearly 500 Mcps, demonstrating exceptional performance comparable to state-of-the-art 3D-stacked SPADs. Furthermore, despite the complexity of the AFE circuits, we achieved compact pixel pitches of 8.41 and 9.69 μm for PQAR and AQAR, respectively, demonstrating that high performance and advanced functionality can be realized within a small pixel area suitable for high-resolution arrays.

IV. Conclusion

In this paper, we presented the design and experimental verification of individual pixels incorporating both PQAR and AQAR AFEs, which form a 64 $\times$ 64 pixel array. These pixels were fabricated using a 40 nm/40 nm 3D-stacked CIS process. Our research involved integrating identical SPAD devices within these pixels under precisely matched process, wafer, and layout conditions on the same die, which allowed for a truly fair and direct performance evaluation.

Our experimental results confirmed precise dead time control for both AFEs, achieving a minimum dead time of 2 ns and MCR reaching nearly 500 Mcps. Our SPAD pixels achieved a highly competitive pixel pitch, 8.41 μm for PQAR and 9.69 μm for AQAR. The AQAR pixel (88.56 μm^2 with 9.69 μm pitch) occupies a larger area than the PQAR pixel (55.75 μm^2 with 8.41 μm pitch), which reflects an area-performance trade-off. However, this area overhead is compensated by its superior afterpulse performance, as experimentally proven by its significantly lower APP (0.6% at 2 ns dead time) compared to the PQAR AFE (2.9% at 2 ns dead time), thereby demonstrating the effectiveness of active quenching in afterpulse suppression. Additionally, further substantial reduction in pixel pitch and area could be achieved using advanced CMOS processes beyond 40 nm or through layout optimization.

The results provide clear insights into the design trade-offs and performance of PQAR and AQAR AFEs and offer valuable guidance for selecting the most appropriate AFE architecture based on specific application requirements, such as area-sensitive PCIS and performance-demanding LiDAR systems.

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